



# SI2321

## P-Channel Enhancement Mode Field Effect Transistor

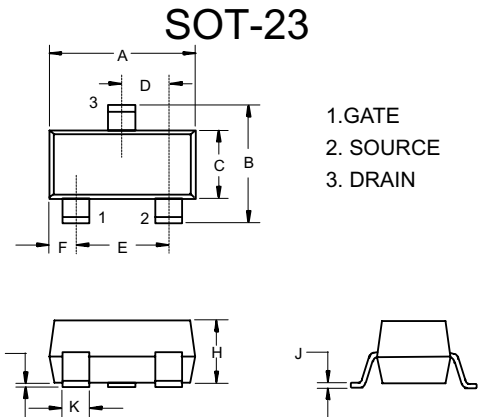
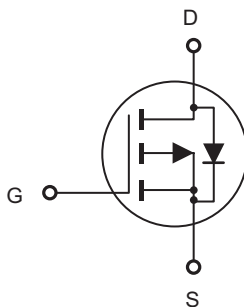
### Features

- Halogen free available upon request by adding suffix "-HF"
- -20V, -2.9A,  $R_{DS(ON)}=57m\Omega @ V_{GS}=-4.5V$   
 $R_{DS(ON)}=76m\Omega @ V_{GS}=-2.5V$
- High dense cell design for extremely low  $R_{DS(ON)}$
- Rugged and reliable
- High Speed Switching
- SOT-23 Package
- Marking Code: S21 K
- Epoxy meets UL 94 V-0 flammability rating
- Moisture Sensitivity Level 1

### Maximum Ratings @ 25°C Unless Otherwise Specified

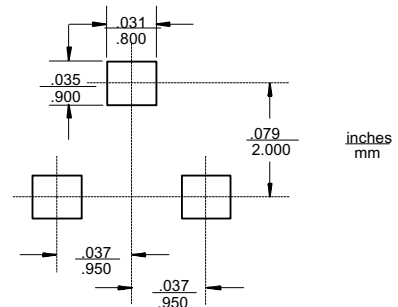
Symbol	Parameter	Rating	Unit
$V_{DS}$	Drain-source Voltage	-20	V
$I_D$	Drain Current-Continuous	-2.9	A
$I_{DM}$	Drain Current-Pulsed	-12	A
$I_S$	Continuous Source-Drain Diode Current	-0.59	A
$V_{GS}$	Gate-source Voltage	$\pm 12$	V
$P_D$	Total Power Dissipation	0.35	W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient	357	$^{\circ}C/W$
$T_J$	Operating Junction Temperature	-55 to +150	$^{\circ}C$
$T_{STG}$	Storage Temperature	-55 to +150	$^{\circ}C$

### Internal Block Diagram



DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.110	.120	2.80	3.04	
B	.083	.104	2.10	2.64	
C	.047	.055	1.20	1.40	
D	.035	.041	.89	1.03	
E	.070	.081	1.78	2.05	
F	.018	.024	.45	.60	
G	.0005	.0039	.013	.100	
H	.035	.044	.89	1.12	
J	.003	.007	.085	.180	
K	.015	.020	.37	.51	

### Suggested Solder Pad Layout



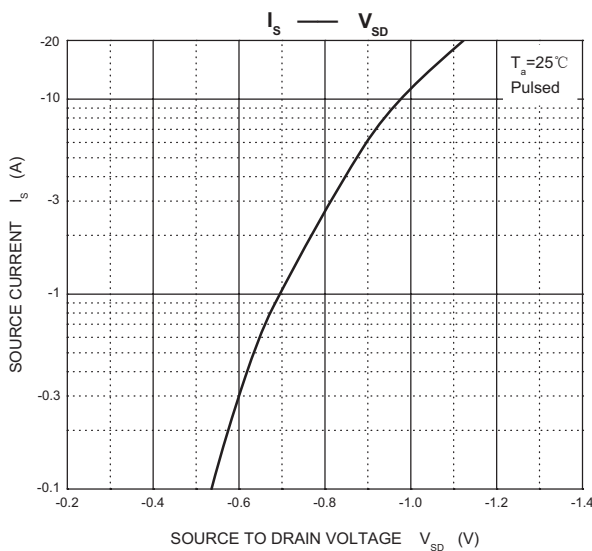
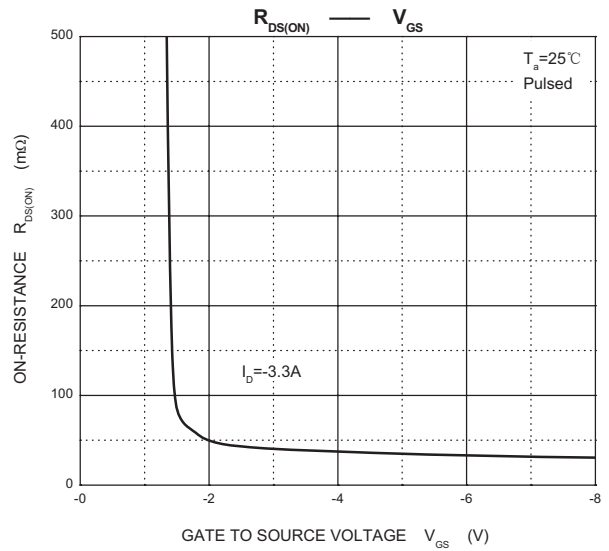
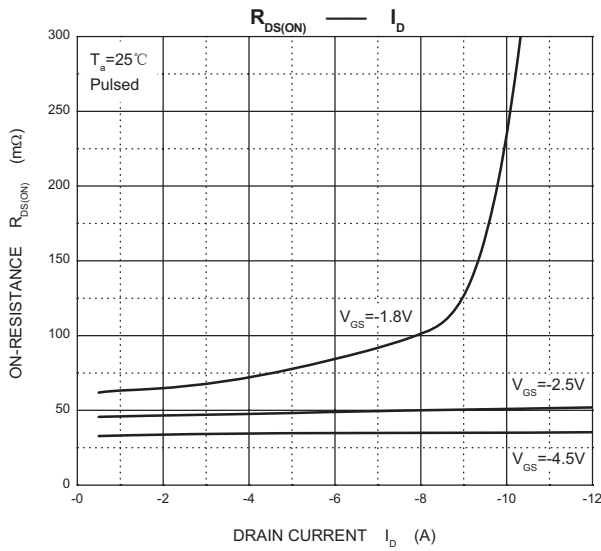
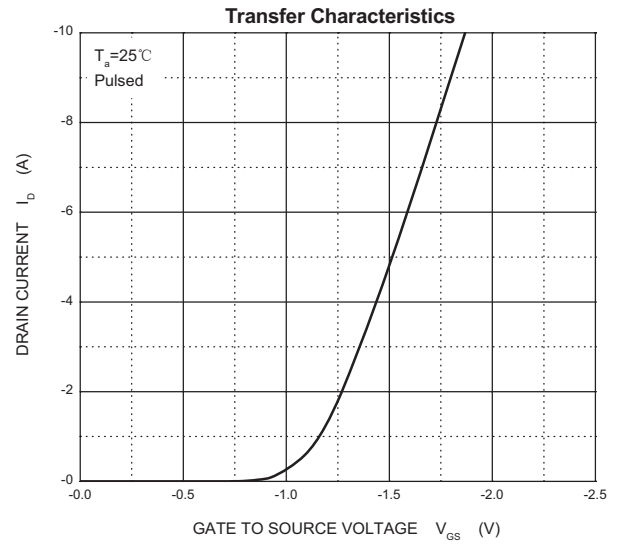
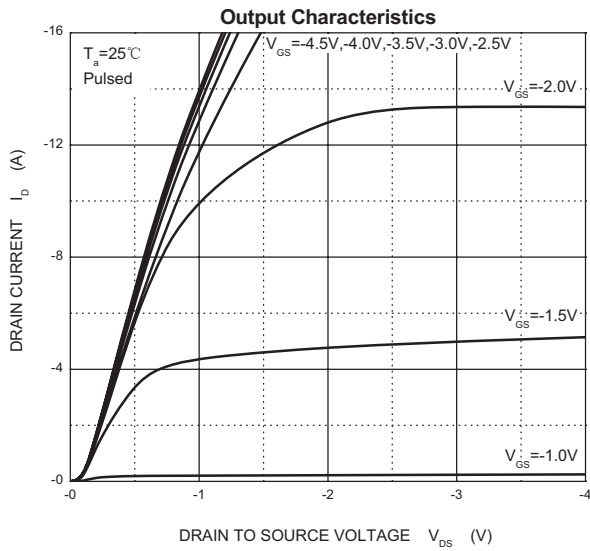
**Electrical characteristics (T<sub>a</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-source breakdown voltage	V <sub>(BR) DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = -10μA	-20			V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±12V			±100	nA
Zero Gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -16V, V <sub>GS</sub> = 0V			-1.0	μA
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA	-0.4		-0.9	V
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3.3A			0.057	Ω
		V <sub>GS</sub> = -2.5V, I <sub>D</sub> = -2.8A			0.076	
		V <sub>GS</sub> = -1.8V, I <sub>D</sub> = -2.3A			0.110	
Forward tranconductance	g <sub>fs</sub>	V <sub>DS</sub> = -5V, I <sub>D</sub> = -3.3A	3			S
Forward diode voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.6A			-1.2	V
<b>Dynamic</b>						
Input capacitance <sup>a,b</sup>	C <sub>iss</sub>	V <sub>DS</sub> = -6V, V <sub>GS</sub> = 0V, f = 1MHz		715		pF
Output capacitance <sup>a,b</sup>	C <sub>oss</sub>			170		
Reverse transfer capacitance <sup>a,b</sup>	C <sub>rss</sub>			120		
Total Gate charge <sup>a</sup>	Q <sub>g</sub>	V <sub>DS</sub> = -6V, V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -3.3A			13	nc
Gate-Source charge <sup>a</sup>	Q <sub>gs</sub>			1.2		nc
Gate-Drain charge <sup>a</sup>	Q <sub>gd</sub>			2.2		nc
<b>Switching<sup>a,b</sup></b>						
Turn-on delay Time	t <sub>d(on)</sub>	V <sub>GEN</sub> = -4.5V, V <sub>DD</sub> = -6V, I <sub>D</sub> = -1.0A, R <sub>G</sub> = 6Ω, R <sub>L</sub> = 6Ω			25	ns
Rise time	t <sub>r</sub>				55	
Turn-off delay time	t <sub>d(off)</sub>				90	
Fall time	t <sub>f</sub>				60	

**Notes :**

a. Pulse Test : pulse width ≤300μs, duty cycle ≤2%.

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Micro Commercial Components

### Ordering Information :

Device	Packing
Part Number-TP	Tape&Reel: 3Kpcs/Reel

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