SILICON LABORATORIES

Si306x

GLOBAL LINE-SIDE DAA FOR EMBEDDED SYSTEM-SIDE MODULE

Features

Complete DAA includes the following:

- 80 dB dynamic range TX/RX paths to support up to V.92 modem speeds
- Programmable line interface
  - AC termination
  - DC termination
  - Ring detect threshold
  - Ringer impedance
- Integrated codec and 2- to 4-wire analog hybrid
- Integrated ring detector
- Pulse dialing support
- Billing tone detection
- Overload detection
- > 5000 V isolation
- Proprietary isolation interface to integrated DAA module
- Line voltage monitor
- Loop current monitor
- Caller ID support
- Low-profile SOIC available in lead-free/ROHS-compliant packages

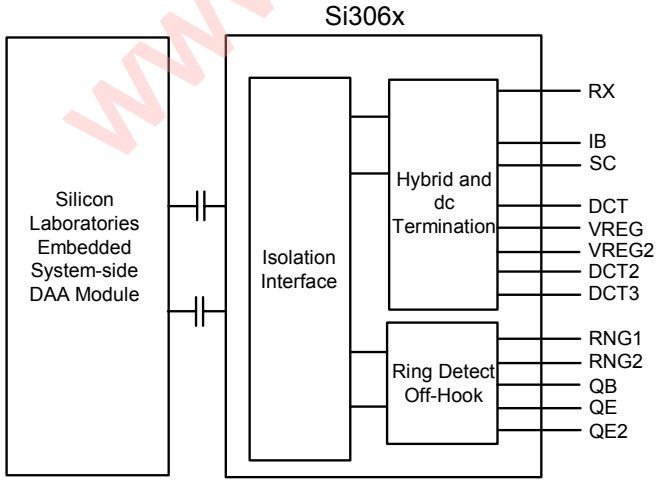
Applications

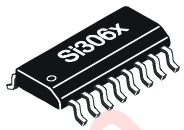
- V.92 soft modems
- PDAs
- Set-top boxes
- Fax machines
- POS terminals
- Multi-function Printers

Description

The Si306x is an integrated direct access arrangement (DAA) with a programmable line interface to meet global telephone line interface requirements. Available in a 16-pin small outline package, it eliminates the need for an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid. The Si306x dramatically reduces the number of discrete components and cost required to achieve compliance with global regulatory requirements. The Si306x interfaces directly to a Silicon Laboratories integrated DAA system-side module.

Functional Block Diagram



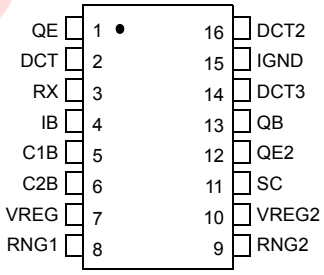


Ordering Information

See page 59.

Pin Assignments

Si306x



US Patent # 5,870,046
US Patent # 6,061,009
Other Patents Pending

1. Si306x Selection Guide

System-Side Requirement	Part Number	Description	Region	AC Terminations	Line Voltage Monitoring
For use with integrated system-side module only	Si3060-X-FS	FCC Line-side	FCC	1	No
	Si3061-X-FS	Global Line-side	Global	4	No
	Si3062-X-FS	Enhanced FCC Line-side	FCC	1	Yes
	Si3063-X-FS	Enhanced Global Line-side	Global	4	Yes
	Si3065-X-FS	Enhanced FCC/TBR21 Line-side	FCC/ TBR21	2	Yes

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2. Electrical Specifications

Table 1. Recommended Operating Conditions

Parameter[1]	Symbol	Test Condition	Min[2]	Typ	Max[2]	Unit
Ambient Temperature	T_A	F/K-Grade	0	25	70	°C

Notes:

1. The Si306x specifications are guaranteed when the typical application circuit (including component tolerance) and any system-side module and any Si306x are used. See "3. Typical Application Schematic" on page 9.
2. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise stated.

Table 2. Loop Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F/K-Grade, see Figure 1)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 11, ILIM = 0, DCV = 00, DCR = 0	—	—	6.0	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, MINI = 11, ILIM = 0, DCV = 00, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 00, ILIM = 0, DCV = 11, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 120 mA, MINI = 00, ILIM = 0, DCV = 11, DCR = 0	9	—	—	V
DC Termination Voltage	V_{TR}	I_L = 20 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	—	—	7.5	V
DC Termination Voltage	V_{TR}	I_L = 60 mA, MINI = 00, ILIM = 1, DCV = 11, DCR = 0	40	—	—	V
On Hook Leakage Current	I_{LK}	V_{TR} = –48 V	—	—	3	µA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 0	10	—	120	mA
Operating Loop Current	I_{LP}	MINI = 00, ILIM = 1	10	—	60	mA
DC Ring Current			—	1.5	3	µA
Ring Detect Voltage*	V_{RD}	RT = 0	13.5	15	16.5	V_{rms}
Ring Detect Voltage*	V_{RD}	RT = 1	19.35	21.5	23.65	V_{rms}
Ring Frequency	F_R		15	—	68	Hz
Ringer Equivalence Number	REN		—	—	0.2	

***Note:** The ring signal is guaranteed to not be detected below the minimum. The ring signal is guaranteed to be detected above the maximum.

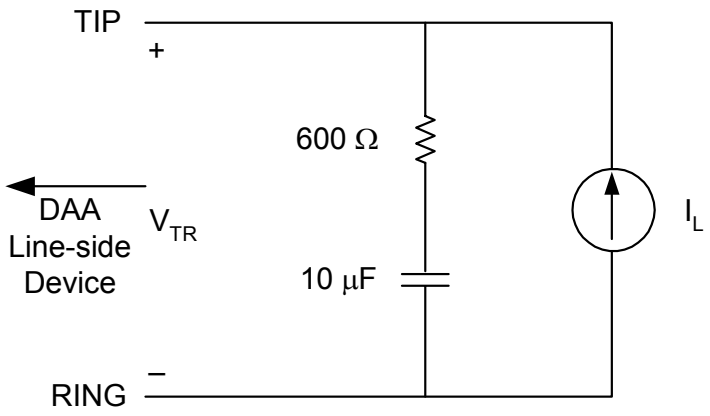


Figure 1. Test Circuit for Loop Characteristics

Table 3. DC Characteristics, V_D = 3.3 V

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	I_L		–10	—	10	µA
Power Supply Current, Analog*	I_D	V_A pin	—	9	12	mA

***Note:** This current is required from the integrated system-side interface to communicate with the Si306x through the proprietary isolation interface.

Table 4. AC Characteristics

(V_D = 3.0 to 3.6 V, T_A = 0 to 70 °C for F/K-Grade, see "3. Typical Application Schematic" on page 9)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Sample Rate	Fs		7.2	—	16[1]	kHz
Transmit Frequency Response		Low –3 dBFS Corner	—	0	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 0	—	5	—	Hz
Receive Frequency Response		Low –3 dBFS Corner, FILT = 1	—	200	—	Hz
Transmit Full Scale Level[2]	V_{FS}	FULL = 0 (0 dBM)	—	1.1	—	V_{PEAK}
Receive Full Scale Level[2,3]	V_{FS}	FULL = 0 (0 dBM)		1.1		V_{PEAK}
Dynamic Range[4,5]	DR	ILIM = 0, DCV = 11, DCR = 0, I_L = 120 mA, MINI = 00	—	80	—	dB
Dynamic Range[4,5]	DR	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	80	—	dB
Dynamic Range[4,5]	DR	ILIM = 1, DCV = 11, DCR = 0, I_L = 60 mA, MINI = 00	—	80	—	dB
Transmit Total Harmonic Distortion[6]	THD	ILIM = 0, DCV = 11, DCR = 0, I_L = 100 mA, MINI = 00	—	–72	—	dB
Transmit Total Harmonic Distortion[6]	THD	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	–78	—	dB
Receive Total Harmonic Distortion[6]	THD	ILIM = 0, DCV = 00, DCR = 0, I_L = 20 mA, MINI = 11	—	–78	—	dB
Receive Total Harmonic Distortion[6]	THD	ILIM = 1, DCV = 11, DCR = 0, I_L = 50 mA, MINI = 00	—	–78	—	dB
Dynamic Range (caller ID mode)[7]	DR_{CID}	VIN = 1 kHz, –13 dBFS	—	50	—	dB
Caller ID Full Scale Level[8]	V_{CID}		—	1.6	—	V_{PEAK}
AOUT Low Level Current			—	—	10	mA
AOUT High Level Current			—	—	10	mA

Notes:

1. The 32.768 MHz system-side module supports sample rates up to 16 kHz. The 32.4 MHz system-side module supports sample rates up to a maximum of 10.286 MHz.
2. Measured at TIP and RING with 600 Ω termination at 1 kHz, as shown in Figure 1.
3. Receive full scale level produces –0.9 dBFS at SDO.
4. DR = 20 x log (RMS V_{FS}/RMS V_{IN}) + 20 x log (RMS V_{IN}/RMS noise). V_{FS} is the 0 dBm full-scale level. RMS noise measurement excludes harmonics. V_{FS} is the 0 dBm full-scale level.
5. Measurement is 300 to 3400 Hz. Applies to both transmit and receive paths. Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
6. THD = 20 x log (RMS distortion/RMS signal). Vin = 1 kHz, –3 dBFS, Fs = 10300 Hz.
7. DR_{CID} = 20 x log (RMS V_{CID}/RMS V_{IN}) + 20 x log (RMS V_{IN}/RMS noise). V_{CID} is the 1.5 V full-scale level for the typical application circuit in Figure 2.
8. With the enhanced CID circuit (refer to "4. Bill of Materials" on page 10), V_{CID} = 1.5 V_{PEAK} and DR_{CID} = 62 dB.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Operating Temperature Range	T_A	–40 to 100	°C
Storage Temperature Range	T_{STG}	–65 to 150	°C

Note: Permanent device damage can occur if the above Absolute Maximum Ratings are exceeded. Restrict functional operation to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods might affect device reliability.

3. Typical Application Schematic

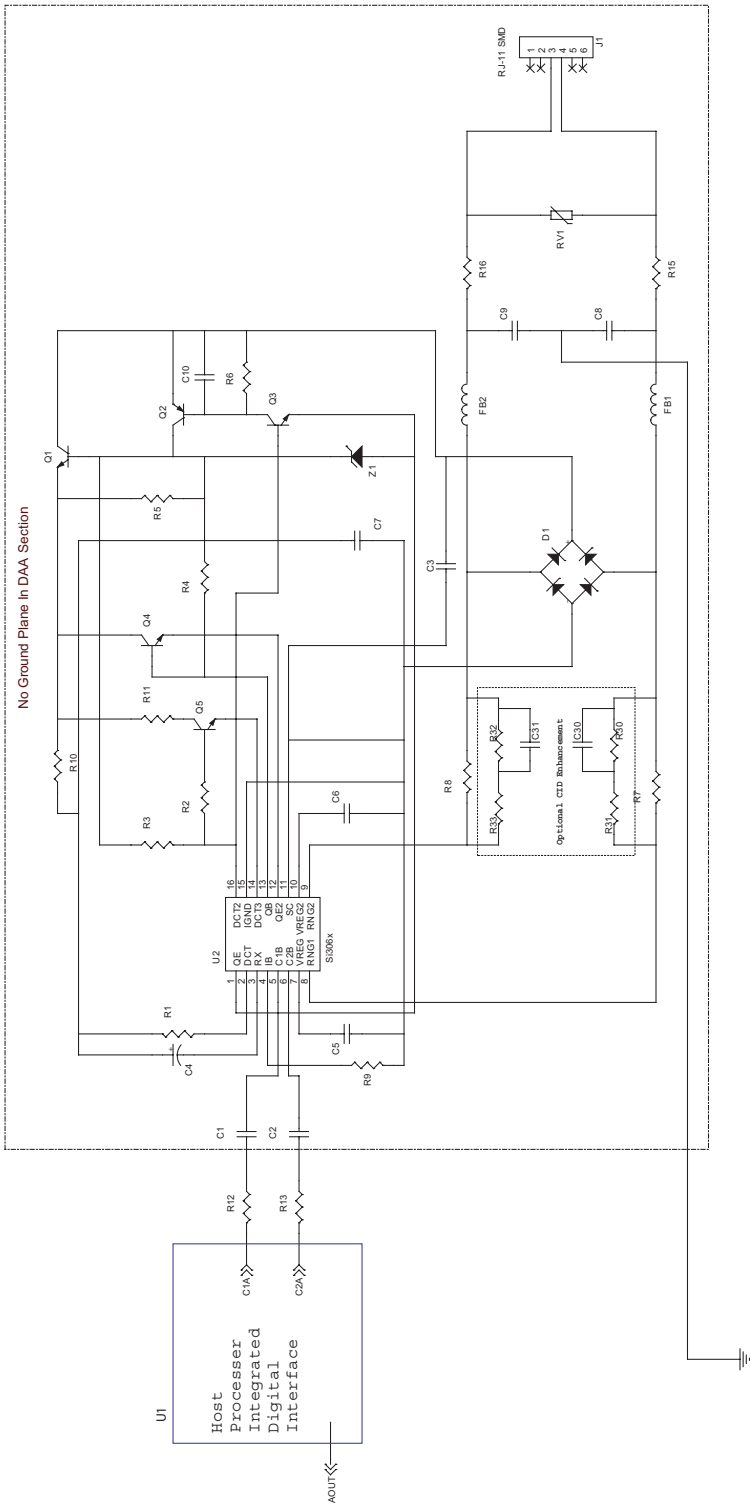


Figure 2. Typical Application Circuit for the Si306x Line-side device (Refer to "AN67: Si3050/52/54/56 Layout Guidelines" for recommended layout guidelines)

4. Bill of Materials

Component(s)	Value	Supplier(s)
C1, C2[1]	33 pF, Y2, X7R, ±20%	Panasonic, Murata, Vishay
C3	10 nF, 250 V, X7R, ±20%	Venkel, SMEC
C4	1.0 µF, 50 V, Elec/Tant, ±20%	Panasonic
C5, C6	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
C7	2.7 nF, 50 V, X7R, ±20%	Venkel, SMEC
C8, C9	680 pF, Y2, X7R, ±10%	Panasonic, Murata, Vishay
C10	0.01 µF, 16 V, X7R, ±20%	Venkel, SMEC
C30, C31[5]	Not installed, 120 pF, 250 V, X7R, ±10%	Venkel, SMEC
D1, D2[2]	Dual Diode, 225 mA, 300 V, CMPD2004	Central Semiconductor
FB1, FB2	Ferrite Bead, BLM18AG601SN1	Murata
Q1, Q3	NPN, 300 V, MMBTA42	Central Semiconductor, OnSemi, Fairchild
Q2	PNP, 300 V, MMBTA92	Central Semiconductor, OnSemi, Fairchild
Q4, Q5	NPN, 60 V, 330 mW, MMBTA06	Central Semiconductor, OnSemi, Fairchild
RV1	Sidactor, 275 V, 100 A	Teccor, ST Micro, Diodes Inc., Shindengen
R1	1.07 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R2	150 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R3	3.65 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R4	2.49 kΩ, 1/2 W, 1%	Venkel, SMEC, Panasonic
R5, R6	100 kΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R7, R8	20 MΩ, 1/16 W, 5%	Venkel, SMEC, Panasonic
R9	1 MΩ, 1/16 W, 1%	Venkel, SMEC, Panasonic
R10	536 Ω, 1/4 W, 1%	Venkel, SMEC, Panasonic
R11	73.2 Ω, 1/2 W, 1%	Venkel, SMEC, Panasonic
R12, R13[3]	56.2 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R15, R16[4]	0 Ω, 1/16 W, 5%	Venkel, SMEC, Panasonic
R30, R32[5]	Not installed, 15 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
R31, R33[5]	Not installed, 5.1 MΩ, 1/8 W, 5%	Venkel, SMEC, Panasonic
U1	SiLabs Integrated System-Side Interface	Silicon Labs
U2	Si306x line-side device	Silicon Labs
Z1	Zener Diode, 43 V, 1/2 W	General Semi, Diodes Inc.,OnSemi

Notes:

1. X2/Y3 or Y2 rated capacitors can be used to comply with Nordic supplemental insulation requirements. Additional vendors for these safety-rated capacitors include Novacap, Syfer, and Kyocera.
2. Several diode bridge configurations are acceptable. Parts, such as a single DF-04S or four 1N4004 diodes, may be used.
3. 56 Ω, 1/16 W, 1% resistors may be substituted for R12-R13 (0 Ω) to decrease emissions.
4. Murata BLM18AG601SN1 may be substituted for R15-R16 (0 Ω) to decrease emissions.
5. C30-C31 and R30-R33 can be substituted for R7-R8 to implement the enhanced caller ID circuit.

5. AOUT PWM Output

Figure 3 illustrates an optional circuit to support the pulse width modulation (PWM) output capability of the Si306x for call progress monitoring purposes. To enable this mode, the INTE bit (Register 2) should be set to 0, the PWME bit (Register 1) set to 1, and the PWMM bits (Register 1) set to 00.

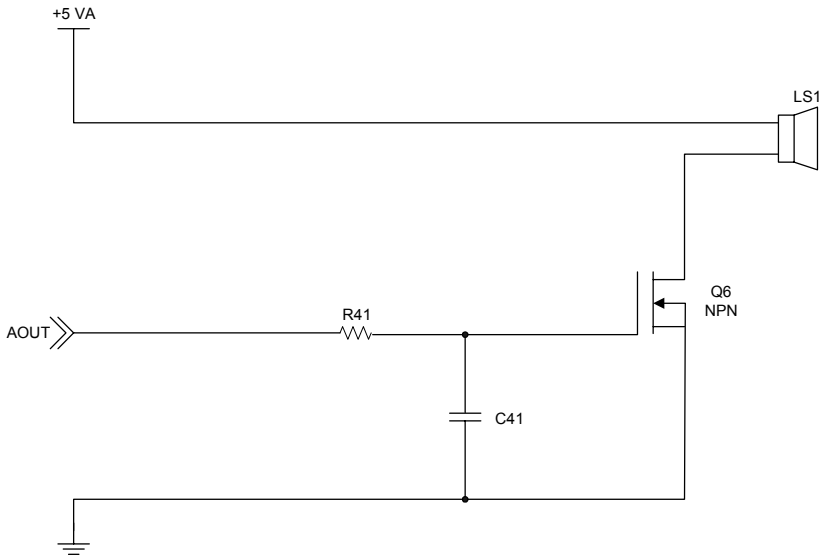


Figure 3. AOUT PWM Circuit for Call Progress

Table 6. Component Values—AOUT PWM

Component	Value	Supplier
LS1	Speaker BRT1209PF-06	Intervox
Q6	NPN KSP13	Fairchild
C41	0.1 µF, 16 V, X7R, ±20%	Venkel, SMEC
R41	150 Ω, 1/16 W, ±5%	Venkel, SMEC, Panasonic

Registers 20 and 21 allow the receive and transmit paths to be attenuated linearly. When these registers are set to all 0s, the receive and transmit paths are muted. These registers affect the call progress output only and do not affect transmit and receive operations on the telephone line.

The PWMM[1:0] bits (Register 1, bits 5:4) select one of the three different PWM output modes for the AOUT signal, including a delta-sigma data stream, a 32 kHz return to zero PWM output, and balanced 32 kHz PWM output.

6. Functional Description

The Si306x is an integrated direct access arrangement (DAA) that provides a programmable line interface to meet global telephone line interface requirements. The Si306x implements Silicon Laboratories' proprietary capacitive isolation technology and offers the highest level of integration by replacing an analog front end (AFE), an isolation transformer, relays, opto-isolators, and a 2- to 4-wire hybrid with a single 16-pin packages (SOIC).

The Si306x DAA can be programmed with software to meet global requirements and is compliant with FCC, TBR21, JATE, and other country-specific PTT specifications as shown in Table 9 on page 20. In addition, the Si306x meets the most stringent worldwide requirements for out-of-band energy, emissions, immunity, high-voltage surges, and safety, including FCC Part 15 and 68, EN55022, EN55024, and many other standards.

6.1. Line-Side Device Support

Silicon Labs offers five different line-side devices in the Si306x family that can be used with the SiLabs integrated system-side module. All five Si306x line-side devices are capable of supporting modem speeds of V.22 through V.92.

- The Si306x line-side device family includes solutions to meet regional PTT specifications or global devices to meet worldwide DAA requirements.
  - Si3060 and Si3062: Single ac termination to meet FCC PTT specifications.
  - Si3065: Two ac termination settings to meet FCC and TBR21 PTT specifications.
  - Si3061 and Si3063: Four ac termination settings to meet global PTT specifications.
- The Si3062, Si3063, and Si3065 enhanced line-side devices additionally provide line voltage monitoring and finer resolution loop current monitoring capabilities.
  - Line voltage monitoring in on-hook and off-hook modes enables non-intrusive line-in-use/parallel handset detection.
  - Polarity reversal interrupt simplifies support of Type II Caller ID.
  - Line current/voltage interrupts improve line monitoring capability.

Table 7. Country Specific Register Settings

Register	16	31	16	16	26	26	26	16[3]	
Country	OHS	OHS2	RZ	RT	ILIM	DCV[1:0]	MINI[1:0]	ACT	ACT2
Argentina	0	0	0	0	0	11	00	0	0
Australia[4]	1	0	0	0	0	01	01	0	1
Austria	0	1	0	0	1	11	00	0	1
Bahrain	0	1	0	0	1	11	00	0	1
Belgium	0	1	0	0	1	11	00	0	1
Brazil	0	0	0	0	0	11	00	0	0
Bulgaria	0	1	0	0	1	11	00	0	1
Canada	0	0	0	0	0	11	00	0	0
Chile	0	0	0	0	0	11	00	0	0
China	0	0	0	0	0	11	00	0	0
Colombia	0	0	0	0	0	11	00	0	0
Croatia	0	1	0	0	1	11	00	0	1
Cyprus	0	1	0	0	1	11	00	0	1
Czech Republic	0	1	0	0	1	11	00	0	1
Denmark	0	1	0	0	1	11	00	0	1
Ecuador	0	0	0	0	0	11	00	0	0
Egypt	0	1	0	0	1	11	00	0	1
El Salvador	0	0	0	0	0	11	00	0	0
Finland	0	1	0	0	1	11	00	0	1
France	0	1	0	0	1	11	00	0	1
Germany	0	1	0	0	1	11	00	0	1
Greece	0	1	0	0	1	11	00	0	1
Guam	0	0	0	0	0	11	00	0	0
Hong Kong	0	0	0	0	0	11	00	0	0
Hungary	0	1	0	0	1	11	00	0	1
Iceland	0	1	0	0	1	11	00	0	1
India	0	0	0	0	0	11	00	0	0

Note:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop current ≥ 20 mA.
3. Available with Si3061, Si3063, and Si3065 line-sides only. See "6.15. AC Termination" on page 21.
4. See "6.14. DC Termination" on page 20 for DCV and MINI settings.

Table 7. Country Specific Register Settings (Continued)

Register	16	31	16	16	26	26	26	16[3]	
Country	OHS	OHS2	RZ	RT	ILIM	DCV[1:0]	MINI[1:0]	ACT	ACT2
Indonesia	0	0	0	0	0	11	00	0	0
Ireland	0	1	0	0	1	11	00	0	1
Israel	0	1	0	0	1	11	00	0	1
Italy	0	1	0	0	1	11	00	0	1
Japan	0	0	0	0	0	01	01	0	0
Jordan	0	0	0	0	0	01	01	0	0
Kazakhstan	0	0	0	0	0	11	00	0	0
Kuwait	0	0	0	0	0	11	00	0	0
Latvia	0	1	0	0	1	11	00	0	1
Lebanon	0	1	0	0	1	11	00	0	1
Luxembourg	0	1	0	0	1	11	00	0	1
Macao	0	0	0	0	0	11	00	0	0
Malaysia[2]	0	0	0	0	0	01	01	0	0
Malta	0	1	0	0	1	11	00	0	1
Mexico	0	0	0	0	0	11	00	0	0
Morocco	0	1	0	0	1	11	00	0	1
Netherlands	0	1	0	0	1	11	00	0	1
New Zealand	0	0	0	0	0	11	00	1	1
Nigeria	0	1	0	0	1	11	00	0	1
Norway	0	1	0	0	1	11	00	0	1
Oman	0	0	0	0	0	01	01	0	0
Pakistan	0	0	0	0	0	01	01	0	0
Peru	0	0	0	0	0	11	00	0	0
Philippines	0	0	0	0	0	01	01	0	0
Poland	0	1	0	0	1	11	00	0	1
Portugal	0	1	0	0	1	11	00	0	1
Romania	0	1	0	0	1	11	00	0	1
Russia	0	0	0	0	0	11	00	0	0

Note:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop current ≥ 20 mA.
3. Available with Si3061, Si3063, and Si3065 line-sides only. See "6.15. AC Termination" on page 21.
4. See "6.14. DC Termination" on page 20 for DCV and MINI settings.

Table 7. Country Specific Register Settings (Continued)

Register	16	31	16	16	26	26	26	16[3]	
Country	**OHS**	**OHS2**	**RZ**	**RT**	**ILIM**	**DCV[1:0]**	**MINI[1:0]**	**ACT**	**ACT2**
Saudi Arabia	0	0	0	0	0	11	00	0	0
Singapore	0	0	0	0	0	11	00	0	0
Slovakia	0	1	0	0	1	11	00	0	1
Slovenia	0	1	0	0	1	11	00	0	1
South Africa	0	0	1	0	0	11	00	1	0
South Korea	0	0	1	0	0	11	00	0	0
Spain	0	1	0	0	1	11	00	0	1
Sweden	0	1	0	0	1	11	00	0	1
Switzerland	0	1	0	0	1	11	00	0	1
Taiwan	0	0	0	0	0	11	00	0	0
TBR21[1]	0	1	0	0	1	11	00	0	1
Thailand	0	0	0	0	0	01	01	0	0
UAE	0	0	0	0	0	11	00	0	0
United Kingdom	0	1	0	0	1	11	00	0	1
USA	0	0	0	0	0	11	00	0	0
Yemen	0	0	0	0	0	11	00	0	0

Note:

1. TBR21 includes the following countries: Austria, Belgium, Denmark, Finland, France, Germany, Greece, Iceland, Ireland, Italy, Luxembourg, Netherlands, Norway, Portugal, Spain, Sweden, Switzerland, and the United Kingdom.
2. Supported for loop current ≥ 20 mA.
3. Available with Si3061, Si3063, and Si3065 line-sides only. See "6.15. AC Termination" on page 21.
4. See "6.14. DC Termination" on page 20 for DCV and MINI settings.

6.2. Power Supplies

The Si306x line-side device derives its power from two sources: The system-side module and the telephone line. The integrated system-side module supplies power over the patented capacitive isolation link between the two devices, allowing the line-side device to communicate with the system-side module while on-hook and perform other on-hook functions such as line voltage monitoring. When off-hook, the line-side device also derives power from the line current supplied from the telephone line. This feature is exclusive to DAAs from Silicon Laboratories and allows the most cost effective implementation for a DAA while still maintaining robust performance over all line conditions.

6.3. Initialization

When the integrated system-side module is powered up, assert the $\overline{\text{RESET}}$ pin. When the $\overline{\text{RESET}}$ pin is deasserted, the registers have default values. This reset condition guarantees the line-side device is powered down without the possibility of loading the line (i.e., off-hook). An example initialization procedure is outlined in the following list:

1. Program the desired sample rate with the Sample Rate Control Register (Register 7).
2. Wait until the line-side PLL is locked. This time is normally between 100 µs and 1 ms from the application of MCLK.
3. Write a 00H into the DAA Control Register (Register 6) to power up the line-side device.
4. Set the required line interface parameters MINI[1:0], ILIM, DCR, ACT and ACT2, OHS, RT, RZ, ATX[2:0] and ARX[2:0] as defined by “Country Specific Register Settings” shown in Table 7.

When this procedure is complete, the Si306x is ready for ring detection and off-hook.

6.4. Isolation Barrier

The Si306x achieves an isolation barrier through low-cost, high-voltage capacitors in conjunction with Silicon Laboratories’ proprietary signal processing techniques. These techniques eliminate signal degradation from capacitor mismatches, common mode interference, or noise coupling. As shown in "3. Typical Application Schematic" on page 9, the C1, C2, C8, and C9 capacitors isolate the integrated system-side module from the line-side device. Transmit, receive, control, ring detect, and caller ID data are passed across this barrier. Y2 class capacitors can be used to achieve surge performance of 5 kV or greater.

The proprietary capacitive communications link is disabled by default. To enable it, the PDL bit (Register 6, bit 4) must be cleared. No communication between the system-side and line-side can occur until this bit is cleared.

6.5. Power Management

The DAA supports four basic power management operation modes. The modes are normal operation, reset operation, sleep mode, and full powerdown mode. PDN and PDL bits (Register 6) control the power management modes.

On powerup, or following a reset, the DAA is in reset operation. The PDL bit is set, and the PDN bit is cleared. The system-side module is operational, except for the communications link. No communication between the system-side module and the Si306x line-side device can occur during reset operation. Bits associated with the line-side device are not valid in this mode.

The most common mode of operation is the normal operation. In this mode, the PDL and PDN bits are cleared. The DAA is operational and the communications link is passing information between the Si306x and the line-side device.

The Si306x supports a low-power sleep mode that supports the wake-up-on-ring feature of many modems. The clock generator registers 7, 8, and 9 must be programmed with valid, non-zero values before enabling sleep mode. The PDN bit must be set and the PDL bit cleared. When the Si306x is in sleep mode, the host processor clock signal must remain active to support ring validation and wake-on-ring features. In low power sleep mode, the system-side module is non-functional except for the communications link and the RGDT signal. To take the Si306x out of sleep mode, the system-side module should be reset.

In summary, the powerdown/up sequence for sleep mode is as follows:

1. Ensure that Registers 7, 8, and 9 must have valid non-zero values.
2. Set the PDN bit (Register 6, bit 3) and clear the PDL bit (Register 6, bit 4).
3. The system-side module clock must stay active.
4. Reset the system-side module.
5. Program registers to the desired settings.

The Si306x also supports an additional powerdown mode. When both the PDN (Register 6, bit 3) and PDL (Register 6, bit 4) bits are set, the chipset enters a complete powerdown mode and draws negligible current (deep sleep mode). In this mode, the ring detect function does not operate. Normal operation is restored by the same process for taking the DAA out of sleep mode.

6.6. Calibration

The DAA initiates two auto-calibrations by default when the device goes off-hook or experiences a loss in line power. A 17 ms resistor calibration is performed to allow circuitry internal to the DAA to adjust to the exact line conditions present at that time. This resistor calibration can be disabled by setting the RCALD bit (Register 25, bit 5). A 256 ms ADC calibration is also performed to remove offsets that might be present in the on-chip A/D converter which could affect the A/D dynamic range. The ADC auto-calibration is initiated after the DAA dc termination stabilizes, and the resistor calibration completes**.** Because large variations in line conditions and line card behavior exist, it could be beneficial to use manual calibration instead of auto-calibration.

Execute manual ADC calibration as close as possible to 256 ms before valid transmit/receive data is expected.

Take the following steps to implement manual ADC calibration:

1. The CALD (auto-calibration disable—Register 17) bit must be set to 1.
2. The MCAL (manual calibration) bit must be toggled to 1 and then 0 to begin and complete the calibration.
3. The calibration is completed in 256 ms.

6.7. In-Circuit Testing

With the Si306x's advanced design the designer can determine system functionality during production line tests, and during support for end-user diagnostics. Two loopback modes allow increased coverage of system components. Four of the test modes require a line-side power source. Although a standard phone line can be used, the test circuit in Figure 1 on page 5 is adequate. In addition, an off-hook sequence must be performed to connect the power source to the line-side device.

For the start-up test mode, line-side power is not necessary and no off-hook sequence is required. The start-up test mode is enabled by default. When the PDL bit (Register 6, bit 4) is set (the default case), the line-side is in a powerdown mode and the DSP-side is in a digital loop-back mode. Data received on SDI passes through the internal filters and transmitted on SDO which introduces approximately 0.9 dB of attenuation on the SDI signal received. The group delay of both transmit and receive filters exists between SDI and SDO. Clearing the PDL bit disables this mode and the SDO data is switched to the receive data from the line-side. When the PDL bit is cleared, the FDT bit (Register 12, bit 6) becomes active, indicating the successful communication between the line-side and DSP-side. This can be used to verify that the communications link is operational.

The digital data loop-back mode offers a way to input data on the SDI pin and have the identical data output on the SDO pin (but bypassing the transmit and receive filters). Setting the DDL bit (Register 10, bit 0) enables this mode. No line-side power or off-hook sequence is required for this mode, which provides an easy way to verify communication between the host processor and the DAA.

The remaining test modes require an off-hook sequence to operate. The following sequence defines the off-hook requirements:

1. Powerup or reset.
2. Program the clock generator to the chosen sample rate.
3. Enable line-side by clearing the PDL bit.
4. Issue an off-hook command.
5. Delay 402.75 ms to allow calibration to occur.
6. Set the test mode.

In the isolation digital loopback mode, the host sends a digital input test pattern on SDI and receives that digital test pattern back on SDO. To enable this mode, set the IDL bit (Register 1, bit 1). In this mode, the isolation barrier is tested. The digital stream is delivered across the isolation capacitors, C1 and C2 of the "3. Typical Application Schematic" on page 9, to the line-side device and returned across the same barrier. In this mode, the 0.9 dB attenuation and filter group delays also exist.

The analog loopback mode allows an external device to drive a signal on the telephone line into the line-side device and returns the signal on to the line. This mode allows testing of external components connecting the RJ-11 jack (TIP and RING) to the line-side device. To enable this mode, set the AL bit (Register 2).

The PCM analog loopback mode extends the signal path of the analog loopback mode. In this mode, an analog signal can be driven from the line into the Si3019 line-side device. This analog signal is converted to digital data and then passed across the isolation barrier capacitors to the system-side device. The data passes through the receive filter, is routed back through the transmit filter, and is then passed back across the isolation barrier and sent back out onto the line as an analog signal. Set the PCML bit (Register 33, bit 7) to enable this mode.

The final testing mode, internal analog loopback, allows the system to test the basic operation of the transmit and receive paths on the line-side device and the external components shown in the "3. Typical Application Schematic" on page 9. In this test mode, the

host provides a digital test waveform on SDI. This data passes across the isolation barrier, is transmitted to and received from the line, passes back across the isolation barrier, and is presented to the host on SDO. To enable this mode, clear the HBE bit (Register 2, bit 1).

When the HBE bit is cleared, this causes a dc offset that affects the signal swing of the transmit signal. Silicon Labs recommends that the transmit signal be 12 dB lower than normal transmit levels. A lower level eliminates clipping from the dc offset that results from disabling the hybrid. It is assumed in this test that the line ac impedance is nominally 600 Ω.

Note: All test modes are mutually exclusive. If more than one test mode is enabled concurrently, the results are unpredictable.

6.8. Exception Handling

The Si306x provides several mechanisms to determine if an error occurs during operation. Through the secondary frames of the serial link, the controlling systems can read several status bits. The bit of highest importance is the frame detect bit (FDT, Register 12, bit 6), which indicates that the system-side (Si306x) and line-side devices are communicating. During normal operation, the FDT bit can be checked before reading bits for information about the line-side. If FDT is not set, the following bits related to the line-side are invalid—RDT, RDTN, RDTP, LCS[4:0], LSID[1:0], REVB[3:0], LCS2[7:0], LVS[7:0], ROV, BTD, DOD, and OVL; the $\overline{\text{RGDT}}$ operation is also non-functional.

Following Powerup and reset, the FDT bit is not set because the PDL bit (Register 6 bit 4) defaults to 1. The communications link does not operate and no information about the line-side can be determined. The user must program the clock generator to a valid configuration for the system and clear the PDL bit to activate the communications link. As the system- and line-side devices are establishing communication, the system-side device does not generate $\overline{\text{FSYNC}}$ signals. Establishing communication takes less than 10 ms. Therefore, if the controlling DSP serial interface is interrupt driven based on the $\overline{\text{FSYNC}}$ signal, the controlling DSP does not require a special delay loop to wait for this event to complete.

The FDT bit also can indicate if the line-side device executes an off-hook request successfully. If the line-side device is not connected to a phone line, the FDT bit remains cleared. The controlling DSP must provide sufficient time for the line-side to execute the off-hook request. The maximum time for FDT to be valid following an off-hook request is 10 ms. If the FDT bit is high, the LCS[4:0] bits indicate the amount of loop current flowing. If the FDT fails to be set following an off-hook request, the PDL bit (Register 6) must be set high for at least 1 ms to reset the line-side.

6.9. Revision Identification

With the Si306x the system designer can determine the revision of the system-side module and/or the line-side device. The REVA[3:0] bits (Register 11, bits 3:0) identify the revision of the system-side module. The REVB[3:0] bits (Register 13, bits 3:0) identify the revision of the line-side device. Table 8 lists revision values for all devices and might contain future revisions not yet in existence.

Table 8. Revision Values

Revision	Si306x
C	0011
D	0100
E	0101
F	0110

6.10. Parallel Handset Detection

The Si306x can detect a parallel handset going off-hook. When the Si306x is off-hook, the loop current can be monitored with the LCS or LCS2 bits. A significant drop in loop current signals a parallel handset going off-hook. If a parallel handset going off-hook causes the loop current to drop to 0, the LCS and LCS2 bits will read all 0s. Additionally, the Drop-Out Detect (DOD) bit will fire (and generate an interrupt if the DODM bit is set) indicating that the line-derived power supply has collapsed.

If the Si3062 or Si3063 line-side device is used, the LVS bits also can be read when on- or off-hook to determine the line voltage. Significant drops in line voltage can signal a parallel handset. For the Si306x to operate in parallel with another handset, the parallel handset must have a sufficiently high dc termination to support two off-hook DAAs on the same line. Improved parallel handset operation can be achieved by changing the dc impedance from 50 Ω to 800 Ω and reducing the DCT pin voltage with the DCV[1:0] bits.

6.11. Line Voltage/Loop Current Sensing

The Si306x line-side devices can measure loop current. The 5-bit LCS[4:0] register reports loop current measurements when off-hook. The Si3062, Si3063, and Si3065 offer an additional register to report loop current to a finer resolution (LCS2[7:0]). The Si3062, Si3063, and Si3065 also offer the capability to measure line voltage. The LVS[7:0] register monitors voltage both on

and off-hook.

These registers can help determine the following:

- When on-hook, detect if a line is connected.
- When on-hook, detect if a parallel phone is off-hook.
- When off-hook, detect if a parallel phone goes on or off-hook.
- Detect if enough loop current is available to operate.
- When used in conjunction with the OPD bit, detect if an overload condition exists (See "6.25. Overload Detection" on page 26).

6.11.1. Line Voltage Measurement (Si3062, Si3063, and Si3065 Only)

The Si3062, Si3063, and Si3065 devices report line voltage with the LVS[7:0] bits (Register 29) in both on- and off-hook states with a resolution of 1 V per bit. The accuracy of these bits is approximately ±10%. Bits 0 through 6 of this register indicate the value of the line voltage in 2s compliment format. Bit 7 of this register indicates the polarity of the tip/ring voltage.

If the INTE bit (Register 2) and the POLM bit (Register 3) are set, a hardware interrupt is generated on the AOUT/$\overline{\text{INT}}$ pin when bit 7 of the LVS register changes state. The edge-triggered interrupt is cleared by writing 0 to the POLI bit (Register 4). The POLI bit is set each time bit 7 of the LVS register changes state and must be written to 0 to clear it.

The default state of the LVS register forces the LVS bits to 0 when the line voltage is 3 V or less. The LVFD bit (Register 31, bit 0) disables the force-to-zero function and allows the LVS register to display non-zero values of 3 V and below. This register might display unpredictable values at line voltages between 0 to 2 V. At 0 V, the LVS register displays all 0s.

6.11.2. Loop Current Measurement

When the DAA is off-hook, the LCS[4:0] bits measure loop current in 3.3 mA/bit resolution. These bits enable detection of another phone going off-hook by monitoring the dc loop current. The line current sense transfer function is shown in Figure 4 and detailed in Table 9. The LCS and LCS2 bits report loop current down to the minimum operating loop current for the DAA. Below this threshold, the reported value of loop current is unpredictable.

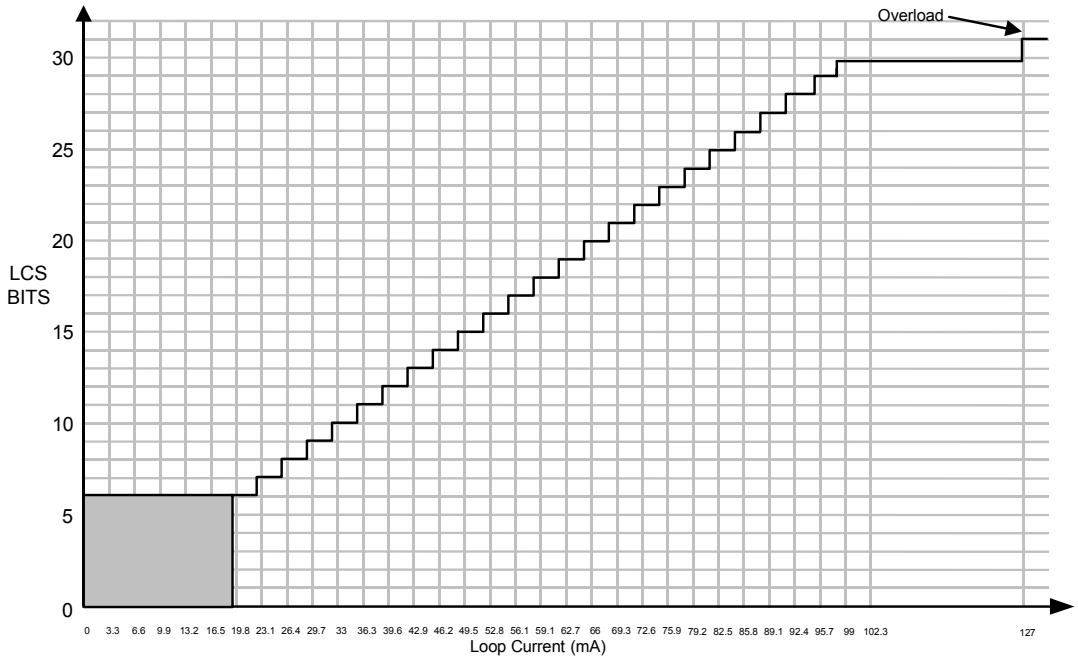


Figure 4. Typical Loop Current LCS Transfer Function

Table 9. Loop Current Transfer Function

LCS[4:0]	Condition
00000	Insufficient line current for normal operation. Use the DOD bit (Register 19, bit 1) to determine if a line is connected.
00100	Minimum line current for normal operation.
11111	Loop current may be excessive. Use the OPD bit to determine if an overload condition exists.

The 8-bit LCS2 register also reports loop current in the off-hook state. This register has resolution of 1.1 mA/bit.

6.12. Off-Hook

The system generates an off-hook command by setting the OH bit (Register 5, bit 0). With the OH bit set, the system is in an off-hook state. The off-hook state seizes the line for incoming/outgoing calls and also can be used for pulse dialing. When the DAA is on-hook, negligible dc current flows through the hookswitch. When the DAA is placed in the off-hook state, the hookswitch transistor pair, Q1 and Q2, turn on. A termination impedance across TIP and RING is applied and causes dc loop current to flow. The termination impedance has an ac and dc component.

Several events occur in the DAA when the OH bit is set. There is a 250 μs latency to allow the off-hook command to be communicated to the line-side device. Once the line-side device goes off-hook, an off-hook counter forces a delay before transmission or reception occurs for line transients to settle. This off-hook counter time is controlled by the FOH[1:0] bits (Register 31, bits 6:5). The default setting for the off-hook counter time is 128 ms, but can be adjusted up to 512 ms or down to either 64 or 8 ms.

After the off-hook counter has expired, a resistor calibration is performed for 17 ms. This allows circuitry internal to the DAA to adjust to the exact conditions present at the time of going off-hook. This resistor calibration can be disabled by setting the RCALD bit (Register 25, bit 5).

After the resistor calibration is performed, an ADC calibration is performed for 256 ms. This calibration helps to remove offset in the A/D sampling the telephone line. This ADC calibration can be disabled by setting the CALD bit (Register 17, bit 5). See “6.6. Calibration” on page 17. for more information on automatic and manual calibration.

Silicon Labs recommends that the resistor and the ADC calibrations not be disabled except when a fast response is needed after going off-hook, such as when responding to a Type II caller-ID signal. See “6.24. Caller ID” on page 25.

To calculate the total time required to go off-hook and start transmission or reception, the digital filter delay should be included in the calculation. (Refer to Table 4 in the appropriate embedded system-side DAA module specification to calculate the digital FIR filter group delay.)

6.13. Interrupts

The $\overline{\text{INT}}$ port in the system-side module can be used by setting the INTE bit (Register 2, bit 7). The default state of this interrupt output port is active low, but active high operation can be enabled by setting the INTP bit (Register 2, bit 6). Bits 7–2, and 0 in Register 3 and bit 1 in Register 44 can be set to enable hardware interrupt sources. When one or more of these bits are set, the $\overline{\text{INT}}$ port becomes active and stays active until the interrupts are serviced. If more than one hardware interrupt is enabled in Register 3, software polling determines the cause of the interrupts. Register 4 and bit 3 of Register 44 contain sticky interrupt flag bits. Clear these bits after servicing the interrupt.

Registers 43 and 44 contain the line current/voltage threshold interrupt. These line current/voltage registers and interrupts are only available with the Si3063 and Si3064 line-side devices. This interrupt will trigger when either the measured line voltage or current in the LVS or LCS2 registers, as selected by the CVS bit (Register 44, bit 2), crosses the threshold programmed into the CVT[7:0] bits. An interrupt can be programmed to occur when the measured value rises above or falls below the threshold. Only the magnitude of the measured value is used to compare to the threshold programmed into the CVT[7:0] bits, and thus only positive numbers should be used as a threshold. This line current/voltage threshold interrupt is only available with the Si3063 and Si3064 line-side devices.

6.14. DC Termination

The DAA has programmable settings for dc impedance, minimum operational loop current, and TIP/RING voltage. The dc impedance of the DAA is normally represented with a 50 Ω slope as shown in Figure 5, but can be changed to an 800 Ω slope by setting the DCR bit. This higher dc termination presents a higher resistance to the line as loop current increases.

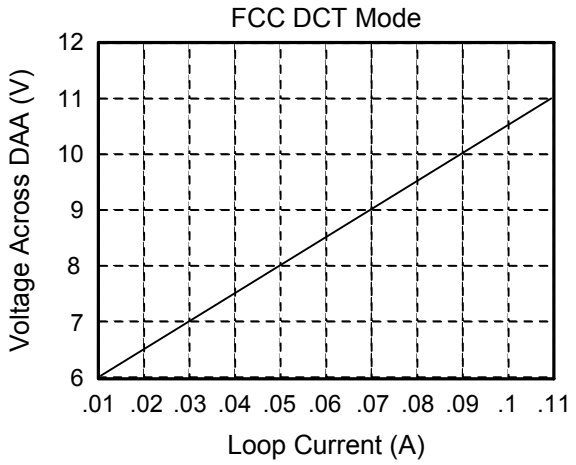


Figure 5. FCC Mode I/V Characteristics, DCV[1:0] = 00, MINI[1:0] = 00, ILIM = 0

For applications that require current limiting per the TBR21 standard, the ILIM bit can be set to select this mode. In the current limiting mode, the dc I/V curve is changed to a 2000 Ω slope above 40 mA, as shown in Figure 6. The DAA operates with a 50 V, 230 Ω feed, which is the maximum line feed specified in the TBR21 standard.

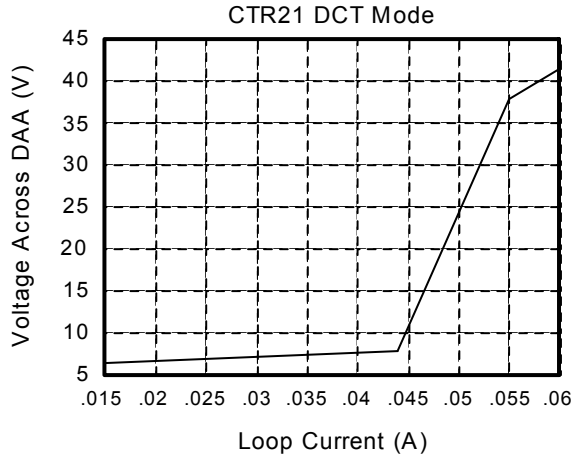


Figure 6. TBR21 Mode I/V Characteristics, DCV[1:0] = 11, MINI[1:0] = 00, ILIM = 1

The MINI[1:0] bits select the minimum operational loop current for the DAA, and the DCV[1:0] bits adjust the DCT pin voltage, which affects the TIP/RING voltage of the DAA. These bits permit important trade-offs to be made between signal headroom and minimum operational loop current. Increasing the TIP/RING voltage provides more signal headroom, while decreasing the TIP/RING voltage allows compliance to PTT standards in low-voltage countries such as Japan. Increasing the minimum operational loop current above 10 mA also increases signal headroom and prevents degradation of the signal level in low-voltage countries.

Finally, Australia has separate dc termination requirements for line seizure versus line hold. Japan mode may be used to satisfy both requirements. However, if a higher transmit level for modem operation is desired, switch to FCC mode 500 ms after the initial off-hook. This satisfies the Australian dc termination requirements.

6.15. AC Termination

The DAA provides one ac termination impedance with the Si3060 and Si3062 line-side devices, two ac terminations with the Si3065, and four ac termination impedances with the Si3061 and Si3063 line-side devices. With the Si3060 and Si3062 line-side devices, the ACT bits (Register 16) are forced to zero to provide the necessary 600 Ω termination to satisfy FCC Part 68. With the Si3061 and Si3063, The ACT and ACT2 bits can be programmed to provide three ac impedance selections in addition to the real, nominal 600 Ω termination. The available ac termination settings are listed for the line-side devices in Tables 10 and 11.

With the Si3065 line side device, only the ACT2 bit is available to enable either the 600 Ω ac termination to meet FCC Part 68 (ACT2 = 0) or a complex impedance to meet TBR21 (ACT2 = 1).

Table 10. AC Termination Settings for the Si3061 and Si3063 Line-Side Devices

ACT	ACT2	AC Termination
0	0	Real, nominal 600 Ω termination that satisfies the impedance requirements of FCC part 68, JATE, and other countries.
1	0	Complex impedance that satisfies global impedance requirements.
0	1	Complex impedance that satisfies global impedance requirements EXCEPT New Zealand. May achieve higher return loss for countries requiring complex ac termination.
1	1	Complex impedance for use in New Zealand.

There are two selections that are useful for satisfying non-standard ac termination requirements. The 350 Ω + (1000 Ω || 210 nF) impedance selection is the ANSI/EIA/TIA 464 compromise impedance network for trunks. The last ac termination selection, ACIM[3:0] = 1111, is

designed to satisfy minimum return loss requirements for every country in the world that requires a complex termination. For any of the ac termination settings, the programmable digital hybrid can be used to further reduce near-end echo. See the following “6.16. Transhybrid Balance” section for more details.

6.16. Transhybrid Balance

The DAA contains an on-chip analog hybrid that performs the 2- to 4-wire conversion and near-end echo cancellation. This hybrid circuit is adjusted for each ac termination setting selected.

6.17. Ring Detection

The ring signal is resistively coupled from TIP and RING to the RNG1 and RNG2 pins. The DAA supports either full- or half-wave ring detection. With full-wave ring detection, the designer can detect a polarity reversal of the ring signal. See “6.24. Caller ID” on page 25. The ring detection threshold is programmable with the RT bit (Register 16, bit 0).

The ring detector mode is controlled by the RFWE bit (Register 18). When the RFWE bit is 0 (default mode), the ring detector operates in half-wave rectifier mode. In this mode, only positive ring signals are detected. A positive ring signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. Conversely, a negative ring signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2. When the RFWE bit is 1, the ring detector operates in full-wave rectifier mode. In this mode, both positive and negative ring signals are detected.

The ring detector output can be monitored in one of two ways. The first method uses the register bits RDTP, RDTN, and RDT (Register 5). The second method uses the SDO output internal to the integrated system-side module.

The ring detector mode is controlled by the RFWE bit (Register 18). When the RFWE bit is 0 (default mode), the ring detector operates in half-wave rectifier mode. In this mode, only positive ring signals are detected. A positive ring signal is defined as a voltage greater than the ring threshold across RNG1-RNG2. Conversely, a negative ring signal is defined as a voltage less than the negative ring threshold across RNG1-RNG2. When the RFWE bit is 1, the ring detector operates in full-wave rectifier mode. In this mode, both positive and negative ring signals are detected.

The first ring detect method uses the ring detect bits (RDTP, RDTN, and RDT). The RDTP and RDTN behavior is based on the RNG1-RNG2 voltage. When the signal on RNG1-RNG2 is above the positive ring threshold the RDTP bit is set. When the signal on RNG1-RNG2 is below the negative ring threshold the RDTN bit is set. When the signal on RNG1-RNG2 is between these thresholds, neither bit is set.

The RDT behavior is also based on the RNG1-RNG2 voltage. When the RFWE bit is 0, a positive ring signal sets the RFWE bit for a period of time. When the RFWE bit is 1, a positive or negative ring signal sets the RDT bit.

The RDT bit acts like a one shot. When a new ring signal is detected, the one shot is reset. If no new ring signals are detected prior to the one shot counter reaching 0, then the RDT bit clears. The length of this count is approximately 5 seconds. The RDT bit is reset to 0 by an off-hook event. If the RDTM bit (Register 3, bit 7) is set, a hardware interrupt occurs on the $\overline{\text{INT}}$ port when RDT is triggered. This interrupt can be cleared by writing to the RDTI bit (Register 4, bit 7). When the RDI bit (Register 2, bit 2) is set, an interrupt occurs on both the beginning and end of the ring pulse as defined by the RTO bits (Register 23, bits 6:3). Ring validation may be enabled when using the RDI bit.

The second ring detect method uses the serial communication interface to transmit ring data. If the communications link is active (PDL=0) and the device is not off-hook or not in on-hook line monitor mode, the ring data is presented on SDO. The waveform on SDO depends on the state of the RFWE bit.

When the RFWE bit is 0, SDO is –32768 (8000h) when the RNG1-RNG2 voltage is between the thresholds. On ring detection, SDO transitions to +32767 when the ring signal is positive, then goes back to –32768 when the ring is near 0 and negative. Therefore, a near square wave is presented on SDO that swings from –32768 to +32767 in cadence with the ring signal.

When the RFWE bit is 1, SDO sits at approximately +1228 when the RNG1-RNG2 voltage is between the thresholds. When the ring becomes positive, SDO transitions to +32767. When the ring signal is near 0, SDO remains near 1228. As the ring signal becomes negative, the SDO transitions to –32768. This repeats in cadence with the ring signal.

To observe the ring signal on SDO, observe the MSB of the data. The MSB toggles at the same frequency as the ring signal independent of the ring detector mode. This method is adequate for determining the ring frequency.

6.18. Ring Validation

This feature prevents false triggering of a ring detection by validating the ring parameters. Invalid signals, such as a line voltage change when a parallel handset goes off-hook, pulse dialing, or a high-voltage line test are

ignored. Ring validation can be enabled during normal operation and in low power sleep mode. The external MCLK signal is required in low power sleep mode for ring validation.

The ring validation circuit operates by calculating the time between alternating crossings of positive and negative ring thresholds to validate that the ring frequency is within tolerance. High and low frequency tolerances are programmable in the RAS[5:0] and RMX[5:0] fields. The RCC[2:0] bits define how long the ring signal must be within tolerance.

Once the duration of the ring frequency is validated by the RCC bits, the circuitry stops checking for frequency tolerance and begins checking for the end of the ring signal, which is defined by a lack of additional threshold crossings for a period of time configured by the RTO[3:0] bits. When the ring frequency is first validated, a timer defined by the RDLY[2:0] bits is started. If the RDLY[2:0] timer expires before the ring timeout, then the ring is validated and a valid ring is indicated. If the ring timeout expires before the RDLY[2:0] timer, a valid ring is not indicated.

Ring validation requires five parameters:

- Timeout parameter to place a lower limit on the frequency of the ring signal on the RAS[5:0] bits (Register 24). The frequency is measured by calculating the time between crossings of positive and negative ring thresholds.
- Minimum count to place an upper limit on the frequency on the RMX[5:0] bits (Register 22).
- Time interval over which the ring signal must be the correct frequency on the RCC[2:0] bits (Register 23).
- Timeout period that defines when the ring pulse has ended based on the most recent ring threshold crossing.
- Delay period between when the ring signal is validated and when a valid ring signal is indicated to accommodate distinctive ringing.

The RNGV bit (Register 24, bit 7) enables or disables the ring validation feature in normal operating mode and low-power sleep mode.

6.19. Ringer Impedance and Threshold

The ring detector in many DAAs is ac coupled to the line with a large 1 µF, 250 V decoupling capacitor. The ring detector on the Si306x DAA is resistively coupled to the line. This coupling produces a high ringer impedance to the line of approximately 20 MΩ to meet the majority of country PTT specifications, including FCC and TBR21.

Several countries including Poland, South Africa, and Slovenia, require a maximum ringer impedance that can be met with an internally synthesized impedance by setting the RZ bit (Register 16, bit 1).

Some countries also specify ringer thresholds differently. The RT bit (Register 16, bit 0) selects between two different ringer thresholds: 15 V ±10% and 21.5 V ±10%. These two settings satisfy ringer threshold requirements worldwide. The thresholds are set so that a ring signal is guaranteed to not be detected below the minimum, and a ring signal is guaranteed to be detected above the maximum.

6.20. Pulse Dialing and Spark Quenching

Pulse dialing results from going off- and on-hook to generate make and break pulses. The nominal rate is 10 pulses per second. Some countries have strict specifications for pulse fidelity that include make and break times, make resistance, and rise and fall times. In a traditional solid-state dc holding circuit, there are many problems in meeting these requirements.

The Si306x dc holding circuit actively controls the on-hook and off-hook transients to maintain pulse dialing fidelity.

Spark quenching requirements in countries such as Italy, the Netherlands, South Africa, and Australia deal with the on-hook transition during pulse dialing. These tests provide an inductive dc feed resulting in a large voltage spike. This spike is caused by the line inductance and the sudden decrease in current through the loop when going on-hook. The traditional solution to the problem is to put a parallel resistive capacitor (RC) shunt across the hookswitch relay. However, the capacitor required is large (~1 µF, 250 V) and relatively expensive. In the Si306x, loop current can be controlled to achieve three distinct on-hook speeds to pass spark quenching tests without additional BOM components. Through the settings of four bits in three registers, OHS (Register 16), OHS2 (Register 31), SQ1 and SQ0 (Register 59), a slow ramp down of loop current can be achieved which induces a delay between the time OH bit is cleared and the time the DAA actually goes on-hook.

To ensure proper operation of the DAA during pulse dialing, disable the automatic resistor calibration that is performed each time the DAA enters the off-hook state by setting the RCALD bit (Register 25, bit 5).

6.21. Billing Tone Detection and Receive Overload

“Billing tones” or “metering pulses” generated by the Central Office can cause modem connection difficulties. The billing tone is typically either a 12 or 16 kHz signal and is sometimes used in Germany, Switzerland, and South Africa. Depending on line conditions, the billing tone might be large enough to cause major errors in the

line data. The DAA can provide feedback indicating the beginning and end of a billing tone.

Billing tone detection is enabled with the BTE bit (Register 17, bit 2). Billing tones less than 1.1 V_{PK} on the line are filtered out by the low pass digital filter of the DAA. The ROV bit is set when a line signal is greater than 1.1 V_{PK}, indicating a receive overload condition. The BTD bit is set when a billing tone is large enough to excessively reduce the line-derived power supply of the line-side device.

The OVL bit (Register 19) can be polled following a billing tone detection. The OVL bit indicates that the billing tone has passed when it returns to 0. The ROV bit is sticky and must be written to 0 to be reset. After the billing tone passes, the DAA initiates an auto-calibration sequence that must complete before data can be transmitted or received.

Certain line events, such as an off-hook event on a parallel phone or a polarity reversal, can trigger the ROV or the BTD bits. Look for multiple events before qualifying if billing tones are present. After the billing tone passes, the DAA initiates an auto-calibration sequence that must complete before data can be transmitted or received.

Although the DAA remains off-hook during a billing tone event, the received data from the line is corrupted when a large billing tone occurs. If the user wishes to receive data through a billing tone, an external LC filter must be added. A manufacturer can provide this filter to users in the form of a dongle that connects on the phone line before the DAA. This prevents the manufacturer from having to include a costly LC filter to support multiple countries and customers.

Alternatively, when a billing tone is detected, the system software notifies the user that a billing tone has occurred. Notification prompts the user to contact the telephone company to disable billing tones or to purchase an external LC filter.

Disturbances on the line other than billing tones can also cause a receive overload. Some conditions may result in a loop current collapse to a level below the minimum required operating current of the DAA. When this occurs, the dropout detect bit (DOD) is set, and an interrupt will be generated if the dropout detect interrupt mask bit (DODM) is set.

6.22. Billing Tone Filter (Optional)

To operate without degradation during billing tones in Germany, Switzerland, and South Africa, requires an external LC notch filter. The Si306x can remain off-hook during a billing tone event, but line data is lost in the presence of large billing tone signals. The notch filter design requires two notches, one at 12 kHz and one at 16 kHz. Because these components are expensive and few countries utilize billing tones, this filter is typically placed in an external dongle or added as a population option for these countries. Figure 7 shows an example billing tone filter.

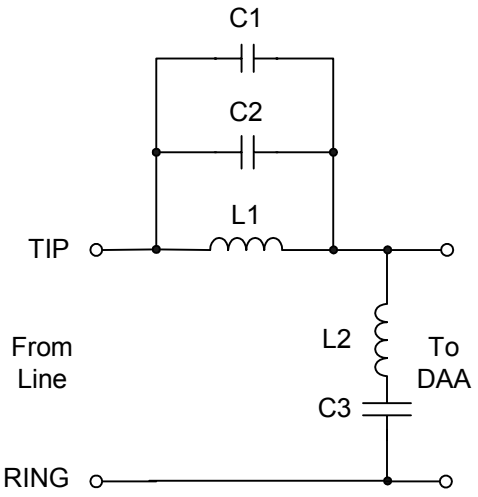


Figure 7. Billing Tone Filter

L1 must carry the entire loop current. The series resistance of the inductors is important to achieve a narrow and deep notch. This design has more than 25 dB of attenuation at both 12 kHz and 16 kHz.

Table 11. Component Values—Optional Billing Tone Filters

Symbol	Value
C1,C2	0.027 μF, 50 V, ±10%
C3	0.01 μF, 250 V, ±10%
L1	3.3 mH, >120 mA, <10 Ω, ±10%
L2	10 mH, >40 mA, <10 Ω, ±10%

The billing tone filter affects the DAA's ac termination and return loss. The global complex ac termination (ACIM = 1111) passes global return loss specifications with and without the billing tone filter by at least 3 dB. This ac termination is optimized for frequency response and hybrid cancellation and has greater than 4 dB of margin with or without the dongle for South Africa, Australia, TBR21, Germany, and Switzerland country specifications.

6.23. On-Hook Line Monitor

The on-hook line monitor mode allows the Si306x to receive line activity when in an on-hook state. This

mode is typically used to detect caller ID data and is enabled by setting the ONHM bit (Register 5, bit 3). Caller ID data can be gained up or attenuated using the receive gain control bits in Register 15.

6.24. Caller ID

With the Si306x, caller ID data can be passed from the phone line to a caller ID decoder connected to the serial port.

6.24.1. Type I Caller ID

Type I Caller ID sends the CID data while the phone is on-hook.

In systems where the caller ID data is passed on the phone line between the first and second rings, utilize the following method to capture the caller ID data:

1. After identifying a ring signal using one of the methods described in "6.17. Ring Detection" on page 22, determine when the first ring is complete.
2. Assert the ONHM bit (Register 5, bit 3) to enable caller ID data detection. The caller ID data passed across the RNG 1/2 pins is presented to the host via the SDO pin.
3. Clear the ONHM bit after the caller ID data is received.

In systems where the caller ID data is preceded by a line polarity (battery) reversal, use the following method to capture the caller ID data:

1. Enable full wave rectified ring detection (RFWE, Register 18, bit 1).
2. Monitor the RDTP and RDTN register bits to identify if a polarity reversal or a ring signal has occurred. A polarity reversal trips either the RDTP or RDTN ring detection bits, and thus the full-wave ring detector must be used to distinguish a polarity reversal from a ring. The lowest specified ring frequency is 15 Hz; therefore, if a battery reversal occurs, the DSP should wait a minimum of 40 ms to verify that the event observed is a battery reversal and not a ring signal. This time is greater than half the period of the longest ring signal. If another edge is detected during this 40 ms pause, this event is characterized as a ring signal and not a battery reversal.
3. Assert the ONHM bit (Register 5, bit 3) to enable caller ID data detection. The caller ID data passed across the RNG 1/2 pins is presented to the data to the host via the SDO pin.
4. Clear the ONHM bit after the caller ID data is received.

6.24.2. Type II Caller ID (Si3063 and Si3064 Line-Side Devices Only)

Type II Caller ID sends the CID data while the phone is off-hook and is often referred to as caller ID/call waiting (CID/CW). To receive the CID data while off-hook, use the following procedure (see Figure 8):

1. The Caller Alert Signal (CAS) tone is sent from the Central Office (CO) and is digitized along with the line data. The host processor must detect the presence of this tone.
2. The DAA must then check for another parallel device on the same line. This is accomplished by briefly going on-hook, measuring the line voltage, and then returning to an off-hook state.
   a. Set the CALD bit (Register 17, bit 5) to disable the calibration that automatically occurs when going off-hook.
   b. Set the RCALD bit (Register 25, bit 5) to disable the resistor calibration from occurring when going off-hook.
   c. Set the FOH[1:0] bits (Register 31, bits 6:5) to 11 to reduce the off-hook counter time to 8 ms.
   d. Clear the OH bit to put the DAA in an on-hook state. The RXM bit (Register 19, bit 3) may also be set to mute the receive path.
   e. Read the LVS bits to determine the state of the line.
      If the LVS bits read the typical on-hook line voltage, then no parallel devices are active on the line and CID data reception can be continued.
      If the LVS bits read well below the typical on-hook line voltage, then one or more devices are present and active on the same line that are not compliant with Type II CID. Do not continue CID data reception.
   f. Set the OH bit to 1 to return to an off-hook state. After returning to an off-hook state and waiting 8 ms for the off-hook counter, normal data transmission and reception can proceed. If a non-compliant parallel device is present, then a reply tone is not sent by the host tone generator and the CO does not proceed with sending the CID data. If all devices on the line are Type II CID compliant, then the host must mute its upstream data output to avoid propagation of its reply tone and the subsequent CID data. After muting its upstream data output, the host processor should then return an acknowledgement (ACK) tone to the CO to request the transmission of the CID data.

3. The CO then responds with the CID data. After receiving the CID data, the host processor unmutes the upstream data output and continues with normal operation.
4. The muting of the upstream data path by the host processor mutes the handset in a telephone application so the user cannot hear the acknowledgement tone and CID data being sent.
5. The CALD and RCALD bits can be cleared to re-enable the automatic calibration when going off-hook. The FOH[1:0] bits also can be programmed to 01 to restore the default off-hook counter time.

Because of the nature of the low-power ADC, the data presented on SDO could have up to a 10% dc offset. The caller ID decoder must either use a high pass or a band pass filter to accurately retrieve the caller ID data.

6.25. Overload Detection

The Si306x can be programmed to detect an overload condition that exceeds the normal operating power range of the DAA circuit. To use the overload detection feature, the following steps should be followed:

1. Set the OH bit (Register 5, bit 0) to go off-hook, and wait 25 ms to allow line transients to settle.
2. Enable overload detection by then setting the OPE bit (Register 17, bit 3).

If the DAA senses an overload situation, it automatically presents an 800 Ω impedance to the line to reduce the hookswitch current. At this time, the DAA also sets the OPD bit (Register 19, bit 0) to indicate that an overload condition exists. The line current detector within the DAA has a threshold that is dependant upon the ILIM bit (Register 26). When ILIM = 0, the overload detection threshold equals 160 mA. When ILIM = 1, the overload detection threshold equals 60 mA. The OPE bit should always be cleared before going off-hook.

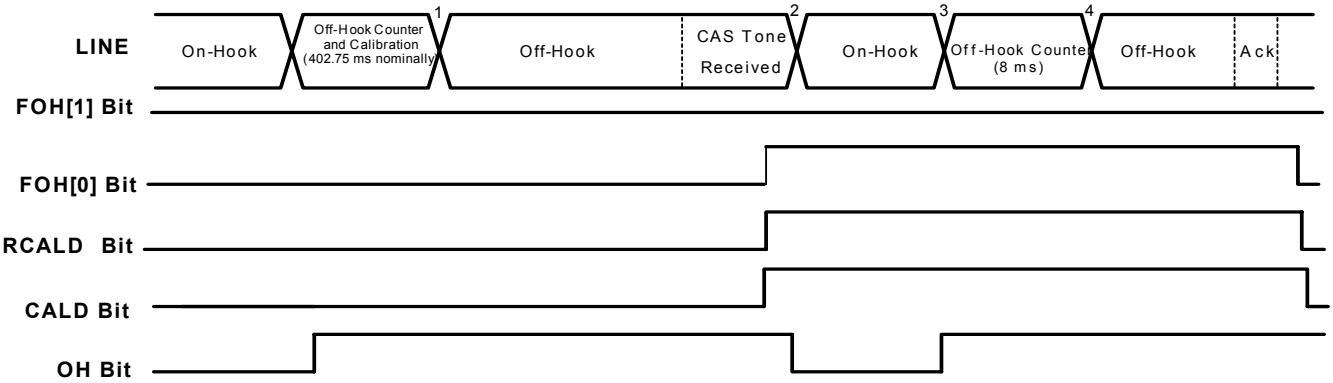
6.26. Gain Control

The DAA supports different gain and attenuation settings depending on the line-side device being used. For all line-side devices, gains of 0, 3, 6, 9, and 12 dB can be selected for the receive path with the ARX[2:0] bits. The receive path can also be muted with the RXM bit. Attenuations of 0, 3, 6, 9, and 12 dB can also be selected for the transmit path with the ATX[2:0] bits. The transmit path also can be muted with the TXM bit.

The signal flow through the DAA line-side and integrated module is shown in Figures 9 and 10.

6.27. Clock Generation

The Si306x line-side device connects to a system-side module that is in turn integrated into a host processor. The Si306x line-side receives all clocking from this module and does not need any other clock inputs. The sample rate for the Si306x is controlled by the Sample Rate Control Register.



Notes:

1. The off-hook counter and calibrations prevent transmission or reception of data for 402.75 ms (default) for the line voltage to settle.
2. The caller alert signal (CAS) tone transmits from the CO to signal an incoming call.
3. The device is taken on-hook to read the line voltage in the LVS bits to detect parallel handsets. In this mode, no data is transmitted on the SDO pin.
4. When the device returns off-hook, the normal off-hook counter is reduced to 8 ms. If the CALD and RCALD bits are set, then the automatic calibrations are not performed.
5. After allowing the off-hook counter to expire (8 ms), normal transmission and reception can continue. If CID data reception is required, send the appropriate signal to the CO at this time.

Figure 8. Implementing Type II Caller ID on the Si306x

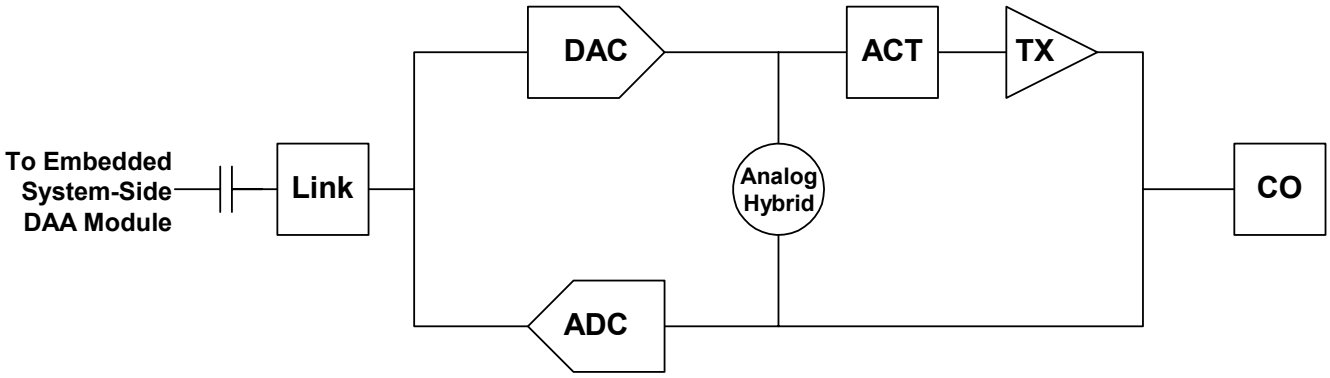
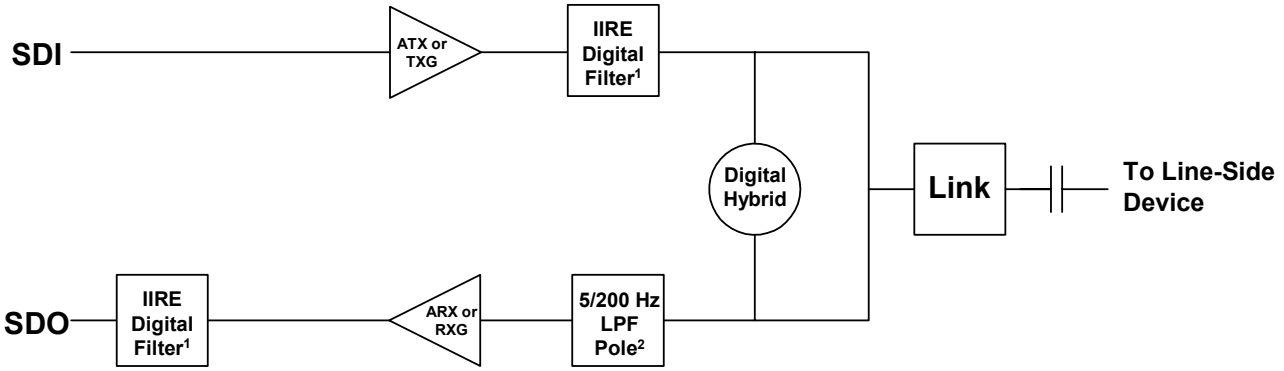


Figure 9. Si306x Signal Flow Diagram



Notes:
1. Available with 32.768 MHz embedded system-side DAA module only.
2. Available with Si3064 line-side device.

Figure 10. Embedded System-Side DAA Module Signal Flow Diagram

7. Control Registers

Table 12. Register Summary

Register	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	Control 1	SR		PWMM[1:0]				IDL	
2	Control 2	INTE	INTP		WDTEN		RDI	HBE	RXE
3	Interrupt Mask	RDTM	ROVM	FDTM	BTDM	DODM	LCSOM		POLM[1]
4	Interrupt Source	RDTI	ROVI	FDTI	BTDI	DODI	LCSOI		POLI[1]
5	DAA Control 1		RDTN	RDTP		ONHM	RDT	OHE	OH
6	DAA Control 2				PDL	PDN			
7	Sample Rate Control					SRC[3:0]			
8	Reserved								
9	Reserved								
10	DAA Control 3								DDL
11	System-Side and Line-Side	LSID[3:0]				REVA[3:0]			
12	Line-Side Device Status		FDT		LCS[4:0]				
13	Line-Side Device Revision		1	REVB[3:0]					
14	Reserved								
15	TX/RX Gain Control 1	TXM	ATX[2:0]			RXM	ARX[2:0]		
16	International Control 1	ACT2[2]	OHS	ACT[2]	IIRE[3]			RZ	RT
17	International Control 2	CALZ	MCAL	CALD		OPE	BTE	ROV	BTD
18	International Control 3							RFWE	
19	International Control 4						OVL	DOD	OPD
20	Call Progress RX Attenuation	ARM[7:0]							
21	Call Progress TX Attenuation	ATM[7:0]							
22	Ring Validation Control 1	RDLY[1:0]		RMX[5:0]					
23	Ring Validation Control 2	RDLY[2]	RTO[3:0]				RCC[2:0]		
24	Ring Validation Control 3	RNGV		RAS[5:0]					
25	Resistor Calibration	RCALS	RCALM	RCALD		RCAL[3:0]			
26	DC Termination Control	DCV[1:0]		MINI[1:0]		Reserved		ILIM	DCR
27	Reserved								
28	Loop Current Status	LCS2[7:0][1]							
29	Line Voltage Status	LVS[7:0][1]							
30	Reserved								
31	DAA Control 4		FOH[1:0]			OHS2		FILT	LVFD[1]
32–42	Reserved								
43	Line Current/Voltage Threshold Interrupt	CVT[7:0][1]							
44	Line Current/Voltage Threshold Interrupt Control					CVI[1]	CVS[1]	CVM[1]	CVP[1]
45–58	Reserved								
59	Spark Quenching Control		SQ1		SQ0		RG1	GCE	

Notes:
1. Bit is available for Si3062, Si3063, and Si3064 line-side devices only.
2. Bit is available for Si3061 and Si3063 line-side devices only.
3. Bit is available with 32.768 MHz system-side module only.

Register 1. Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	SR		PWMM[1:0]				IDL	
Type	R/W		R/W				R/W	

Reset settings = 0000_0000

Bit	Name	Function
7	SR	**Software Reset.** 0 = Enables the DAA for normal operation. 1 = Sets all registers to their reset value. **Note:** Bit automatically clears after being set.
6	Reserved	Read returns zero.
5:4	PWMM[1:0]	**Pulse Width Modulation Mode.** Refer to PWMM bit description in the embedded system-side module specification for operation of these bits. The PWM output signals depends on the input clock frequency provided to the SiLabs system-side module.
3:2	Reserved	Read returns zero.
1	IDL	**Isolation Digital Loopback.** 0 = Digital loopback across the isolation barrier is disabled. 1 = Enables digital loopback mode across the isolation barrier. The line-side device must be enabled and off-hook before setting this mode. This data path includes the TX and RX filters.
0	Reserved	Read returns zero.

Register 2. Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	INTE	INTP		WDTEN		RDI	HBE	RXE
Type	R/W	R/W		R/W		R/W	R/W	R/W

Reset settings = 0000_0011

Bit	Name	Function
7	INTE	**Interrupt Pin Enable.** 0 = The $\overline{INT}$ port is disabled. 1 = The $\overline{INT}$ port is enabled.
6	INTP	**Interrupt Polarity Select.** 0 = The $\overline{INT}$ port is active low. 1 = The $\overline{INT}$ port is active high.
5	Reserved	Returns to zero.
4	WDTEN	**Watchdog Timer Enable.** When set, this bit can only be cleared by a hardware reset. The watchdog timer monitors register accesses. If no register accesses occur within a 4 second window, the DAA is put into an on-hook state. A write of a DAA register restarts the watchdog timer counter. If the watchdog timer times out, the OH bit is cleared, placing the DAA into an on-hook state. Setting the OH bit places the DAA back into an off-hook state. 0 = Watchdog timer disabled. 1 = Watchdog timer enabled.
3	Reserved	Returns to zero.
2	RDI	**Ring Detect Interrupt Mode.** This bit operates in conjunction with the RDTM and RDTI bits. This bit is selected if one or two interrupts are generated for every ring burst. 0 = An interrupt is generated at the beginning of every ring burst. 1 = An interrupt is generated at the beginning and end of every ring burst. The interrupt at the beginning of the ring burst must be serviced (by writing a 0 to the RDTI bit) before the end of the ring burst for both interrupts to occur.
1	HBE	**Hybrid Enable.** 0 = Disconnects hybrid in transmit path. 1 = Connects hybrid in transmit path.
0	RXE	**Receive Enable.** 0 = Receive path disabled. 1 = Enables receive path.

Register 3. Interrupt Mask

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTM	ROVM	FDTM	BTDM	DODM	LCSOM		POLM
Type	R/W	R/W	R/W	R/W	R/W	R/W		R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RDTM	**Ring Detect Mask.** 0 = A ring signal does not cause an interrupt on the $\overline{\text{INT}}$ port. 1 = A ring signal causes an interrupt on the $\overline{\text{INT}}$ port.
6	ROVM	**Receive Overload Mask.** 0 = A receive overload does not cause an interrupt on the $\overline{\text{INT}}$ port. 1 = A receive overload causes an interrupt on the $\overline{\text{INT}}$ port.
5	FDTM	**Frame Detect Mask.** 0 = The communications link achieving frame lock does not cause an interrupt on the $\overline{\text{INT}}$ port. 1 = The communications link achieving frame lock causes an interrupt on the $\overline{\text{INT}}$ port.
4	BTDM	**Billing Tone Detect Mask.** 0 = A detected billing tone does not cause an interrupt on the $\overline{\text{INT}}$ port. 1 = A detected billing tone causes an interrupt on the $\overline{\text{INT}}$ port.
3	DODM	**Drop Out Detect Mask.** 0 = A line supply dropout does not cause an interrupt on the $\overline{\text{INT}}$ port. 1 = A line supply dropout causes an interrupt on the $\overline{\text{INT}}$ port.
2	LCSOM	**Loop Current Sense Overload Mask.** 0 = An interrupt does not occur when the LCS bits are all 1s. 1 = An interrupt occurs when the LCS bits are all 1s.
1	Reserved	Read returns zero.
0	POLM	**Polarity Reversal Detect Mask (Si3062, Si3063, and Si3065 line-side devices only).** Generated from bit 7 of the LVS register. When this bit transitions, it indicates that the polarity of TIP and RING was switched. 0 = A polarity change on TIP and RING does not cause an interrupt on the $\overline{\text{INT}}$ port. 1 = A polarity change on TIP and RING causes an interrupt on the $\overline{\text{INT}}$ port.

Register 4. Interrupt Source

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDTI	ROVI	FDTI	BTDI	DODI	LCSOI		POLI
Type	R/W	R/W	R/W	R/W	R/W	R/W		R/W

Reset settings = 0000_0000

Bit	Name	Function
7	RDTI	**Ring Detect Interrupt.** 0 = A ring signal is not occurring. 1 = A ring signal is detected. If the RDTM (Register 3) and INTE (Register 2) bits are set a hardware interrupt occurs on the $\overline{\text{INT}}$ port. This bit must be written to a 0 to be cleared. The RDI bit (Register 2) determines if this bit is set only at the beginning of a ring pulse, or at the end of a ring pulse as well. This bit should be cleared after clearing the PDL bit (Register 6) because powering up the line-side device may cause this interrupt to be triggered.
6	ROVI	**Receive Overload Interrupt.** 0 = An excessive input level on the receive pin is not occurring. 1 = An excessive input level on the receive pin is detected. If the ROVM and INTE bits are set a hardware interrupt occurs on the $\overline{\text{INT}}$ port. This bit must be written to 0 to clear it. This bit is identical in function to the ROV bit (Register 17). Clearing this bit also clears the ROV bit.
5	FDTI	**Frame Detect Interrupt**. 0 = Frame detect is established on the communications link. 1 = This bit is set when the communications link does not have frame lock. If the FDTM and INTE bits are set, a hardware interrupt occurs on the $\overline{\text{INT}}$ port. Once set, this bit must be written to a 0 to be cleared.
4	BTDI	**Billing Tone Detect Interrupt.** 0 = A billing tone has not occurred. 1 = A billing tone has been detected. If the BTDM and INTE bits are set, a hardware interrupt occurs on the $\overline{\text{INT}}$ port. This bit must be written to 0 to clear it.
3	DODI	**Drop Out Detect Interrupt**. 0 = The line-side power supply has not collapsed. 1 = The line-side power supply has collapsed. (The DOD bit in Register 19 has fired.) If the DODM and INTE bits are set, a hardware interrupt occurs on the $\overline{\text{INT}}$ port. This bit must be written to 0 to clear it. This bit should be cleared after clearing the PDL bit (Register 6) because powering as the line-side device can cause this interrupt to be triggered.
2	LCSOI	**Loop Current Sense Overload Interrupt**. 0 = The LCS bits have not reached max (all ones). 1 = The LCS bits have reached max value. If the LCSOM bit (Register 3) and the INTE bit are set, a hardware interrupt occurs on the $\overline{\text{INT}}$ port. This bit must be written to 0 to clear it. LCSOI does not necessarily imply that an overcurrent situation has occurred. An overcurrent situation in the DAA is determined by the status of the OPD bit (Register 19). After the LCSOI interrupt fires, the OPD bit should be checked to determine if an overcurrent situation exists.
1	Reserved	Read returns zero.
0	POLI	**Polarity Reversal Detect Interrupt (Si3062, Si3063, and Si3065 line-side devices only).** 0 = Bit 7 of the LVS register does not change states. 1 = Bit 7 of the LVS register changes from a 0 to a 1, or from a 1 to a 0, indicating the polarity of TIP and RING is switched. If the POLM and INTE bits are set, a hardware interrupt occurs on the $\overline{\text{INT}}$ port. To clear the interrupt, write this bit to 0.

Register 5. DAA Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		RDTN	RDTP		ONHM	RDT		OH
Type		R	R		R/W	R		R/W

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	RDTN	**Ring Detect Signal Negative.** 0 = No negative ring signal is occurring. 1 = A negative ring signal is occurring.
5	RDTP	**Ring Detect Signal Positive.** 0 = No positive ring signal is occurring. 1 = A positive ring signal is occurring.
4	Reserved	Read returns zero.
3	ONHM	**On-Hook Line Monitor.** 0 = Normal on-hook mode. 1 = Enables low-power on-hook monitoring mode allowing the host to receive line activity without going off-hook. This mode is used for caller-ID detection.
2	RDT	**Ring Detect.** 0 = Reset 5 seconds after last positive ring is detected or when the system executes an off-hook. Only a positive ring sets this bit when RFWG = 0. When RFWG = 1, either a positive or negative ring sets this bit. 1 = Indicates a ring is occurring.
1	Reserved	Read returns zero.
0	OH	**Off-Hook.** 0 = Line-side device on-hook. 1 = Causes the line-side device to go off-hook. This bit operates independently of the OHE bit and is a logic OR with the off-hook pin when enabled.

Register 6. DAA Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PDL	PDN			
Type				R/W	R/W			

Reset settings = 0001_0000

Bit	Name	Function
7:5	Reserved	Read returns zero.
4	PDL	**Powerdown Line-Side Device.** 0 = Normal operation. Program the clock generator before clearing this bit. 1 = Places the line-side device in lower power mode.
3	PDN	**Powerdown System-Side Module.** 0 = Normal operation. 1 = Powers down the system-side device. A pulse on $\overline{\text{RESET}}$ is required to restore normal operation.
2:0	Reserved	Read returns zero.

Register 7. Sample Rate Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					SRC[3:0]			
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3:0	SRC[3:0]	**Sample Rate Control.** Sets the sample rate of the line-side device. The following sample rate settings are available with either the 32.4 MHz or the 32.768 MHz system-side modules: 0000 = 7200 Hz 0001 = 8000 Hz 0010 = 8229 Hz 0011 = 8400 Hz 0100 = 9000 Hz 0101 = 9600 Hz 0110 = 10286 Hz The following sample rate settings are only available with the 32.768 MHz system-side module and are otherwise reserved bits (read returns zero): 0111 = 12000 Hz 1000 = 13714 Hz 1001 = 16000 Hz For all system-side modules: 1010–1111 = reserved

Register 8-9. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 10. DAA Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								DDL
Type								R/W

Reset settings = 0000_0000

Bit	Name	Function
7:1	Reserved	Read returns zero.
0	DDL	**Digital Data Loopback.** 0 = Normal operation. 1 = Takes data received on DRX and loops it back out to DTX before the TX and RX filters. Output data is identical to input data.

Register 11. System-Side and Line-Side

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LSID[3:0]				REVA[3:0]			
Type	R				R			

Reset settings = xxxx_xxxx

Bit	Name	Function
7:4	LSID[3:0]	**Line-Side ID Bits.** These four bits will always read one of the following values depending on which line-side device is used. LSID[3:0] Si3060 1000 Si3061 1001 Si3062 1010 Si3063 1011 Si3064 0111 Si3065 0110
3:0	REVA[3:0]	**System-Side Revision.** Four-bit value indicating the revision of the system-side device.

Register 12. Line-Side Device Status

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FDT		LCS[4:0]				
Type	R			R				

Reset settings = 0000_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6	FDT	**Frame Detect.** 0 = Indicates the communications link has not established frame lock. 1 = Indicates the communications link frame lock is established.
5	Reserved	Read returns zero.
4:0	LCS[4:0]	**Loop Current Sense.** 5-bit value returning the loop current when the DAA is in an off-hook state. 00000 = Loop current is less than required for normal operation. 00100 = Minimum loop current for normal operation. 11111 = Loop current is >127 mA, and a current overload condition may exist.

Register 13. Line-Side Device Revision

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		1	REVB[3:0]					
Type	R							

Reset settings = xxxx_xxxx

Bit	Name	Function
7	Reserved	Read returns zero.
6	1	This bit always reads a one.
5:2	REVB[3:0]	**Line-Side Device Revision.** Four-bit value indicating the revision of the line-side device.
1:0	Reserved	Read returns zero.

Register 14. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 15. TX/RX Gain Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	TXM	ATX[2:0]			RXM	ARX[2:0]		
Type	R/W	R/W			R/W	R/W		

Reset settings = 0000_0000

Bit	Name	Function
7	TXM	**Transmit Mute.** 0 = Transmit signal is not muted. 1 = Mutes the transmit signal.
6:4	ATX[2:0]	**Analog Transmit Attenuation.** 000 = 0 dB attenuation 001 = 3 dB attenuation 010 = 6 dB attenuation 011 = 9 dB attenuation 1xx = 12 dB attenuation
3	RXM	**Receive Mute.** 0 = Receive signal is not muted. 1 = Mutes the receive signal.
2:0	ARX[2:0]	**Analog Receive Gain.** 000 = 0 dB gain 001 = 3 dB gain 010 = 6 dB gain 011 = 9 dB gain 1xx = 12 dB gain

Register 16. International Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ACT2	OHS	ACT	IIRE			RZ	RT
Type	RW	R/W	R/W	R/W			R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7	ACT2	**AC Termination Select 2.** Works with the ACT bit to select one of four ac terminations. **Si3061 and Si3063 Settings:** **ACT2 ACT AC Termination** 0 0 Real, 600 Ω 0 1 Global complex impedance 1 0 TBR21 complex impedance 1 1 New Zealand complex impedance **Si3065 Settings:** **ACT2 ACT AC Termination** 0 0 Real, 600 Ω 0 1 TBR21 complex impedance 1 0 TBR21 complex impedance 1 1 Real, 600 Ω **Si3060 and Si3062 Settings:** **ACT2 ACT AC Termination** X X Real, 600 Ω The global complex impedance meets minimum return loss requirements in countries that require a complex ac termination. For improved return loss performance, the other complex impedances can be used.
6	OHS	**On-Hook Speed.** This bit, in combination with the OHS2 bit and the SQ[1:0] bits, sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **Si3061 and Si3063 Settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec) **Si3060, Si3062, and Si3065 Settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** X X XX Less than 0.5 ms
5	ACT	**AC Termination Select.** Works with the ACT2 bit to select one of four ac terminations. See ACT2 description above.
4	IIRE	**IIR Filter Enable (32.768 MHz System-Side Module only).** 0 = FIR filter enabled for transmit and receive filters. 1 = IIR filter enabled for transmit and receive filters. Refer to Figures 3–6 in the 32.768 MHz embedded system-side DAA module specification.

Bit	Name	Function
3:2	Reserved	Read returns zero.
1	RZ	**Ringer Impedance.** **Si3061 and Si3063 Settings:** 0 = Maximum (high) ringer impedance. 1 = Synthesized ringer impedance. See "6.19. Ringer Impedance and Threshold" on page 23. **Si3060, Si3062, and Si3065 Settings:** X = Maximum (high) ringer impedance.
0	RT	**Ringer Threshold Select.** This bit is used to satisfy country requirements on ring detection. Signals below the lower level do not generate a ring detection; signals above the upper level are guaranteed to generate a ring detection. 0 = 13.5 to 16.5 1 = 19.35 to 23.65 **Si3060, Si3062, and Si3065 Settings:** X = 13.5 to 16.5 V_{rms}

Register 17. International Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CALZ	MCAL	CALD		OPE	BTE	ROV	BTD
Type	R/W	R/W	R/W		R/W	R/W	R/W	R

Reset settings = 0000_0000

Bit	Name	Function
7	CALZ	**Clear ADC Calibration.** 0 = Normal operation. 1 = Clears the existing calibration data. This bit must be written back to 0 after being set.
6	MCAL	**Manual ADC Calibration.** 0 = No calibration. 1 = Initiate manual ADC calibration.
5	CALD	**ADC Auto-Calibration Disable.** 0 = Enable auto-calibration. 1 = Disable auto-calibration.
4	Reserved	Read returns zero or one.
3	OPE	**Overload Protect Enable.** 0 = Disabled. 1 = Enabled. The OPE bit should always be cleared before going off-hook.
2	BTE	**Billing Tone Detect Enable.** When set, the DAA can detect a billing tone signal on the line and maintain on off-hook state through the billing tone. If a billing tone is detected, the BTD bit (Register 17) is set to indicate the event. Writing this bit to zero clears the BTD bit. 0 = Billing tone detection disabled. The BDT bit is not function. 1 = Billing tone detection enabled. The BDT is functional.
1	ROV	**Receive Overload.** This bit is set when the receive input has an excessive input level (i.e., receive pin goes below ground). Writing a zero to this location clears this bit and the ROVI bit (Register 4, bit 6). 0 = Normal receive input level. 1 = Excessive receive input level.
0	BTD	**Billing Tone Detected.** This bit is set if a billing tone is detected. Writing a zero to BTE clears this bit. 0 = No billing tone detected. 1 = Billing tone detected.

Register 18. International Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							RFWE	
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:2	Reserved	Read returns zero or one.
1	RFWE	**Ring Detector Full Wave Rectifier Enable.** When RNGV (Register 24) is disabled, this bit controls the ring detector mode and the assertion of the RGDT pin. When RNGV is enabled, this bit configures the RGDT pin to either follow the ringing signal detected by the ring validation circuit or to follow an unqualified ring detect one-shot signal initiated by a ring-threshold crossing and terminated by a fixed counter timeout of approximately five seconds. **RNGV RFWE RGDT** 0 0 Half wave 0 1 Full wave 1 0 Validated Ring Envelope 1 1 Ring Threshold Crossing One-Shot
0	Reserved	Read returns zero.

Register 19. International Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						OVL	DOD	OPD
Type						R	R	R

Reset settings = 0000_0000

Bit	Name	Function
7:3	Reserved	Read returns zero.
2	OVL	**Receive Overload Detect.** This bit has the same function as ROV in Register 17, but clears itself after the overload is removed. This bit is only masked by the off-hook counter and is not affected by the BTE bit. 0 = Normal receive input level. 1 = Excessive receive input level.
1	DOD	**Recal/Dropout Detect.** When the line-side device is off-hook, it is powered from the line itself. This bit will read 1 when loop current is not flowing. For example, if the line-derived power supply collapses, such as when the line is disconnected, this bit is set to 1. When on-hook and the line-side device is enabled, this bit is set to 1. 0 = Normal operation. 1 = Line supply dropout detected when off-hook.
0	OPD	**Overload Protection Detect.** This bit is used to indicate that the DAA has detected a loop current overload. The detector firing threshold depends on the setting of the ILIM bit (Register 26). **OPD** **ILIM** **Overcurrent Threshold** **Overcurrent Status** 0 0 160 mA No overcurrent condition exists 0 1 60 mA No overcurrent condition exists 1 0 160 mA An overcurrent condition has been detected 1 1 60 mA An overcurrent condition has been detected

Register 20. Call Progress RX Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ARM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ARM[7:0]	**AOUT Receive Path Attenuation.** When decremented from the default setting, these bits linearly attenuate the AOUT receive path signal used for call progress monitoring. Setting the bits to all 0s mutes the AOUT receive path. Attenuation = 20log(ARM[7:0]/64) 1111_1111 = +12 dB (gain) 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute

Register 21. Call Progress TX Attenuation

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	ATM[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	ATM[7:0]	**AOUT Transmit Path Attenuation.** When decremented from the default settings, these bits linearly attenuate the AOUT transmit path signal used for call progress monitoring. Setting the bits to all 0s mutes the AOUT transmit path. Attenuation = 20log(ATM[7:0]/64) 1111_1111 = +12 dB (gain) 0111_1111 = +6 dB (gain) 0100_0000 = 0 dB 0010_0000 = –6 dB (attenuation) 0001_0000 = –12 dB . . . 0000_0000 = Mute

Register 22. Ring Validation Control 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[1:0]		RMX[5:0]					
Type	R/W		R/W					

Reset settings = 1001_0110

Bit	Name	Function
7:6	RDLY[1:0]	**Ring Delay Bits 1 and 0.** These bits, in combination with the RDLY[2] bit (Register 23), set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms . . . 1 11 1792 ms
5:0	RMX[5:0]	**Ring Assertion Maximum Count.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field and if it exceeds the value in RMX[5:0] then the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/ (2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms}, RMX \leq RAS$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.

Register 23. Ring Validation Control 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDLY[2]	RTO[3:0]				RCC[2:0]		
Type	R/W	R/W				R/W		

Reset settings = 0010_1101

Bit	Name	Function
7	RDLY[2]	**Ring Delay Bit 2.** This bit, in combination with the RDLY[1:0] bits (Register 22), set the amount of time between when a ring signal is validated and when a valid ring signal is indicated. **RDLY[2] RDLY[1:0] Delay** 0 00 0 ms 0 01 256 ms 0 10 512 ms . . . 1 11 1792 ms
6:3	RTO[3:0]	**Ring Timeout.** These bits set when a ring signal is determined to be over after the most recent ring threshold crossing. **RTO[3:0] Ring Timeout** 0000 80 ms 0001 128 ms 0010 256 ms . . . 1111 1920 ms
2:0	RCC[2:0]	**Ring Confirmation Count.** These bits set the amount of time that the ring frequency must be within the tolerances set by the RAS[5:0] bits and the RMX[5:0] bits to be classified as a valid ring signal. **RCC[2:0] Ring Confirmation Count Time** 000 100 ms 001 150 ms 010 200 ms 011 256 ms 100 384 ms 101 512 ms 110 640 ms 111 1024 ms

Register 24. Ring Validation Control 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RNGV		RAS[5:0]					
Type	R/W		R/W					

Reset settings = 0001_1001

Bit	Name	Function
7	RNGV	**Ring Validation Enable.** 0 = Ring validation feature is disabled. 1 = Ring validation feature is enabled in both normal operating mode and low-power mode.
6	Reserved	Reserved and may read either a 1 or 0.
5:0	RAS[5:0]	**Ring Assertion Time.** These bits set the maximum ring frequency for a valid ring signal within a 10% margin of error. During ring qualification, a timer is loaded with the RAS[5:0] field upon a TIP/RING event and decrements at a regular rate. When a subsequent TIP/RING event occurs, the timer value is compared to the RMX[5:0] field and if it exceeds the value in RMX[5:0] then the frequency of the ring is too high and the ring is invalidated. The difference between RAS[5:0] and RMX[5:0] identifies the minimum duration between TIP/RING events to qualify as a ring, in binary-coded increments of 2.0 ms (nominal). A TIP/RING event typically occurs twice per ring tone period. At 20 Hz, TIP/RING events would occur every 1/ (2 x 20 Hz) = 25 ms. To calculate the correct RMX[5:0] value for a frequency range [f_min, f_max], the following equation should be used: $$RMX[5:0] \geq RAS[5:0] - \frac{1}{2 \times f\_max \times 2\ ms}, RMX \leq RAS$$ To compensate for error margin and ensure a sufficient ring detection window, it is recommended that the calculated value of RMX[5:0] be incremented by 1.

Register 25. Resistor Calibration

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RCALS	RCALM	RCALD		RCAL[3:0]			
Type	R	R/W	R/W	R	R/W			

Reset settings = xxxx_xxxx

Bit	Name	Function
7	RCALS	**Resistor Auto Calibration.** 0 = Resistor calibration is not in progress. 1 = Resistor calibration is in progress.
6	RCALM	**Manual Resistor Calibration.** 0 = No calibration. 1 = Initiate manual resistor calibration. (After a manual calibration has been initiated, this bit must be cleared within 1 ms.)
5	RCALD	**Resistor Calibration Disable.** 0 = Internal resistor calibration enabled. 1 = Internal resistor calibration disabled.
4	Reserved	Do not write to this register bit. This bit always reads a zero.
3:0	RCAL[3:0]	Always write back the value read.

Register 26. DC Termination Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DCV[1:0]		MINI[1:0]				ILIM	DCR
Type	R/W		R/W				R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:6	DCV[1:0]	**TIP/RING Voltage Adjust.** Adjust the voltage on the DCT pin of the line-side device, which affects the TIP/RING voltage on the line. Low voltage countries should use a lower TIP/RING voltage. Raising the TIP/RING voltage improves signal headroom. **Si3061 and Si3063 settings:** **DCV[1:0] DCT Pin Voltage** 00 3.1 V 01 3.2 V 10 3.35 V 11 3.5 V **Si3060, Si3062, and Si3065 settings:** **DCV[1:0] DCT Pin Voltage** XX 3.35 V
5:4	MINI[1:0]	**Minimum Operational Loop Current.** Adjusts the minimum loop current so the DAA can operate. Increasing the minimum operational loop current improves signal headroom at a lower TIP/RING voltage. **Si3061 and Si3063 settings:** **MINI[1:0] Min Loop Current** 00 10 mA 01 12 mA 10 14 mA 11 16 mA **Si3060, Si3062, and Si3065 settings:** **MINI[1:0] Min Loop Current** XX 10 mA
3:2	Reserved	Do not write to these register bits.
1	ILIM	**Current Limiting Enable.** **Si3061, Si3063, and Si3065 settings:** 0 = Current limiting mode disabled. 1 = Current limiting mode enabled. Limits loop current to a maximum of 60 mA per the TBR21 standard. **Si3060 and Si3062 settings:** X = Current limiting mode disabled.
0	DCR	**DC Impedance Selection.** 0 = 50 Ω dc termination is selected. Use this mode for all standard applications. 1 = 800 Ω dc termination is selected.

Register 27. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Do not read or write.

Register 28. Loop Current Status (Si3063 and Si3064 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LCS2[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	LCS2[7:0]	**Loop Current Status.** Eight-bit value returning the loop current. Each bit represents 1.1 mA of loop current. 0000_0000 = Loop current is less than required for normal operation.

Register 29. Line Voltage Status (Si3063 and Si3064 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	LVS[7:0]							
Type	R							

Reset settings = 0000_0000

Bit	Name	Function
7:0	LVS[7:0]	**Line Voltage Status.** Eight-bit value returning the loop voltage. Each bit represents 1 V of loop voltage. This register operates in on-hook and off-hook modes. Bit seven of this register indicates the polarity of the TIP/RING voltage. When this bit changes state, it indicates that a polarity reversal has occurred. The value returned is represented in 2s compliment format. 0000_0000 = No line is connected.

Register 30. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 31. DAA Control 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		FOH[1:0]			OHS2		FILT	LVFD
Type	R/W				R/W		R/W	R/W

Reset settings = 0010_0000

Bit	Name	Function
7	Reserved	Read returns zero.
6:5	FOH[1:0]	**Fast Off-Hook Selection.** These bits determine the length of the off-hook counter. The default setting is 128 ms. 00 = 512 ms 01 = 128 ms 10 = 64 ms 11 = 8 ms
4	Reserved	Read returns zero.
3	OHS2	**On-Hook Speed 2.** This bit, in combination with the OHS bit (Register 16) and the SQ[1:0] bits on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **OHS** **OHS2** **SQ[1:0]** **Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms ±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec)
2	Reserved	Read returns zero.
1	FILT	**Filter Pole Selection (Si3064 Line-Side Device Only).** 0 = The receive path has a low –3 dBFS corner at 5 Hz. 1 = The receive path has a low –3 dBFS corner at 200 Hz.
0	LVFD	**Line Voltage Force Disable (Si3062, Si3063, and Si3065 Line-Side Devices Only).** 0 = Normal operation. 1 = The circuitry that forces the LVS register (Register 29) to all 0s at 3 V or less is disabled. The LVS register may display unpredictable values at voltages between 0 to 2 V. All 0s are displayed if the line voltage is 0 V.

Register 32-42. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = 0000_0000

Bit	Name	Function
7:0	Reserved	Read returns zero.

Register 43. Line Current / Voltage Threshold Interrupt (Si3062, Si3063, and Si3065 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	CVT[7:0]							
Type	R/W							

Reset settings = 0000_0000

Bit	Name	Function
7:0	CVT[7:0]	**Current/Voltage Threshold.** Determines the threshold at which an interrupt is generated from either the LCS or LVS register. Generate this interrupt to occur when the line current or line voltage rises above or drops below the value in the CVT[7:0] register.

Register 44. Line Current/Voltage Threshold Interrupt Control (Si3062, Si3063, and Si3065 Line-Side Device Only)

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					CVI	CVS	CVM	CVP
Type					R/W	R/W	R/W	R/W

Reset settings = 0000_0000

Bit	Name	Function
7:4	Reserved	Read returns zero.
3	CVI	**Current/Voltage Interrupt.** 0 = The current / voltage threshold has not been crossed. 1 = The current / voltage threshold is crossed. If the CVM and INTE bits are set, a hardware interrupt occurs on the $\overline{INT}$ port. Once set, this bit must be written to 0 to be cleared.
2	CVS	**Current/Voltage Select.** 0 = The line current shown in the LCS2 register generates an interrupt. 1 = The line voltage shown in the LVS register generates an interrupt.
1	CVM	**Current/Voltage Interrupt Mask.** 0 = The current / voltage threshold being triggered does not cause a hardware interrupt on the $\overline{INT}$ port. 1 = The current / voltage threshold being triggered causes a hardware interrupt on the $\overline{INT}$ port.
0	CVP	**Current/Voltage Interrupt Polarity.** 0 = The current / voltage threshold is triggered by the absolute value of the number in either the LCS2 or LVS register falling below the value in the CVT[7:0] register. 1 = The current / voltage threshold is triggered by the absolute value of the number in the either the LCS2 or LVS register rising above the value in the CVT[7:0] Register.

Register 45-58. Reserved

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type								

Reset settings = xxxx_xxxx

Bit	Name	Function
7:0	Reserved	Do not write to these register bits.

Register 59. Spark Quenching Control

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		SQ1		SQ0		RG1	GCE	
Type		R/W		R/W		R/W	R/W	

Reset settings = xxxx_xxxx

Bit	Name	Function
7	Reserved	Always write this bit to zero.
6	SQ[1:0]	**Spark Quenching.** This bit, in combination with the OHS bit (Register 16), and the OHS2 bit (Register 31), sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **Si3061 and Si3063 settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec) **Si3060, Si3062, and Si3065 settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** X X XX Less than 0.5 ms
5	Reserved	Always write this bit to zero.
4	SQ[1:0]	**Spark Quenching.** This bit, in combination with the OHS bit (Register 16), and the OHS2 bit (Register 31), sets the amount of time for the line-side device to go on-hook. The on-hook speeds specified are measured from the time the OH bit is cleared until loop current equals zero. **Si3061 and Si3063 settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** 0 0 00 Less than 0.5 ms 0 1 00 3 ms±10% (meets ETSI standard) 1 X 11 26 ms ±10% (meets Australia spark quenching spec) **Si3060, Si3062, and Si3065 settings:** **OHS OHS2 SQ[1:0] Mean On-Hook Speed** X X XX Less than 0.5 ms
3	Reserved	Always write this bit to zero.
2	RG1	**Receive Gain 1 (Si3064 Line-side Revision E or later).** This bit enables receive path gain adjustment. 0 = No gain applied to hybrid, full scale RX on line = 0 dBm 1 = 1 dB of gain applied to hybrid, full scale RX on line = –1 dBm.
1	GCE	**Guarded Clear Enable (Si3064 Line-side Revision E or later).** This bit (in conjunction with the R2 bit set to 1), enables the Si306x to meet BT's Guarded Clear Spec (B5 6450, Part 1: 1993, Section 15.4.3.3). With these bits set, the DAA will draw approximately 2.5 mA of current from the line while on-hook. 0 = Default, DAA does not draw loop current. 1 = Guarded Clear enabled, DAA draws 2.5 mA while on-hook to meet Guarded Clear requirement.
0	Reserved	Always write this bit to zero.

APPENDIX—UL1950 3RD EDITION

Although designs using the Si306x comply with UL1950 3rd Edition and pass all overcurrent and overvoltage tests, there are still several issues to consider.

Figure 11 shows two designs that can pass the UL1950 overvoltage tests, and electromagnetic emissions. The top schematic of Figure 11 shows the configuration in which the ferrite beads (FB1, FB2) are on the unprotected side of the sidactor (RV1). For this configuration, the current rating of the ferrite beads needs to be 6 A. However, the higher current ferrite beads are less effective in reducing electromagnetic emissions.

The bottom schematic of Figure 11 shows the configuration in which the ferrite beads (FB1, FB2) are on the protected side of the sidactor (RV1). For this design, the ferrite beads can be rated at 200 mA.

In a cost optimized design, compliance to UL1950 does not always require overvoltage tests. Plan ahead to know which overvoltage tests apply to the system. System-level elements in the construction, such as fire enclosure and spacing requirements, need to be considered during the design stages. Consult with a professional testing agency during the design of the product to determine the tests that apply to the system.

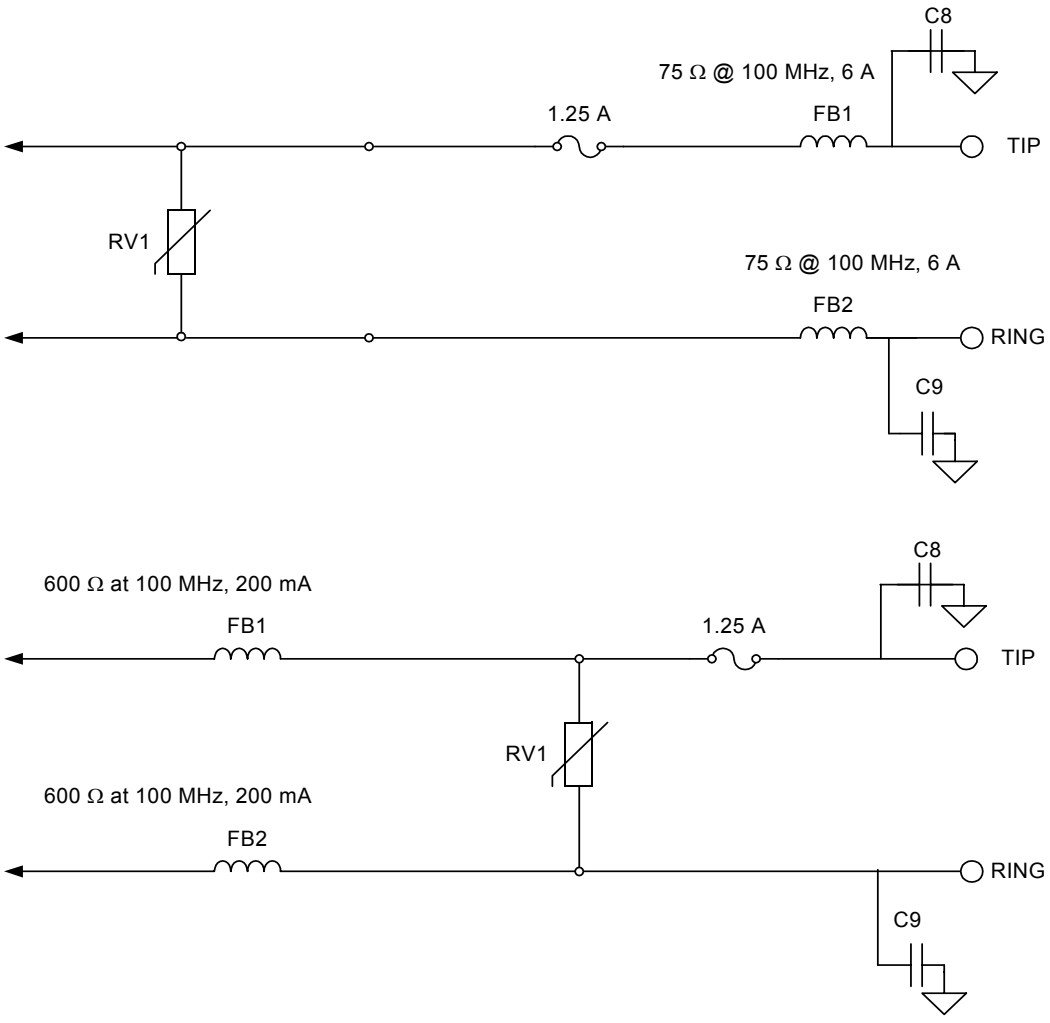


Figure 11. Circuits that Pass All UL1950 Overvoltage Tests

8. Pin Descriptions: Si306x

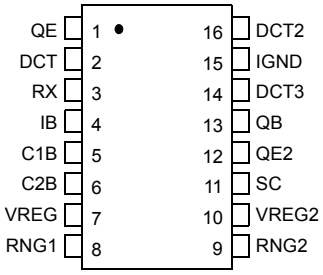


Table 13. Si306x Pin Descriptions

Pin #	Pin Name	Description
1	QE	**Transistor Emitter.** Connects to the emitter of Q3.
2	DCT	**DC Termination.** Provides dc termination to the telephone network.
3	RX	**Receive Input.** Serves as the receive side input from the telephone network.
4	IB	**Isolation Capacitor 1B.** Connects to one side of isolation capacitor C1. Used to communicate with the system-side device.
5	C1B	**Internal Bias.** Provides internal bias.
6	C2B	**Isolation Capacitor 2B.** Connects to one side of the isolation capacitor C2. Used to communicate with the system-side device.
7	VREG	**Voltage Regulator.** Connects to an external capacitor to provide bypassing for an internal power supply.
8	RNG1	**Ring 1.** Connects through a resistor to the RING lead of the telephone line. Provides the ring and caller ID signals to the system-side device.
9	RNG2	**Ring 2.** Connects through a resistor to the TIP lead of the telephone line. Provides the ring and caller ID signals to the system-side device.
10	VREG2	**Voltage Regulator 2.** Connects to an external capacitor to provide bypassing for an internal power supply.
11	SC	**SC Connection.** Enables external transistor network. Should be tied through a 0 Ω resistor to I_{GND}.
12	QE2	**Transistor Emitter 2.** Connects to the emitter of transistor Q4.

Table 13. Si306x Pin Descriptions (Continued)

Pin #	Pin Name	Description
13	QB	**Transistor Base.** Connects to the base of transistor Q4.
14	DCT3	**DC Termination 3.** Provides dc termination to the telephone network.
15	IGND	**Isolated Ground.** Connects to ground on the line-side interface.
16	DCT2	**DC Termination 2.** Provides dc termination to the telephone network.

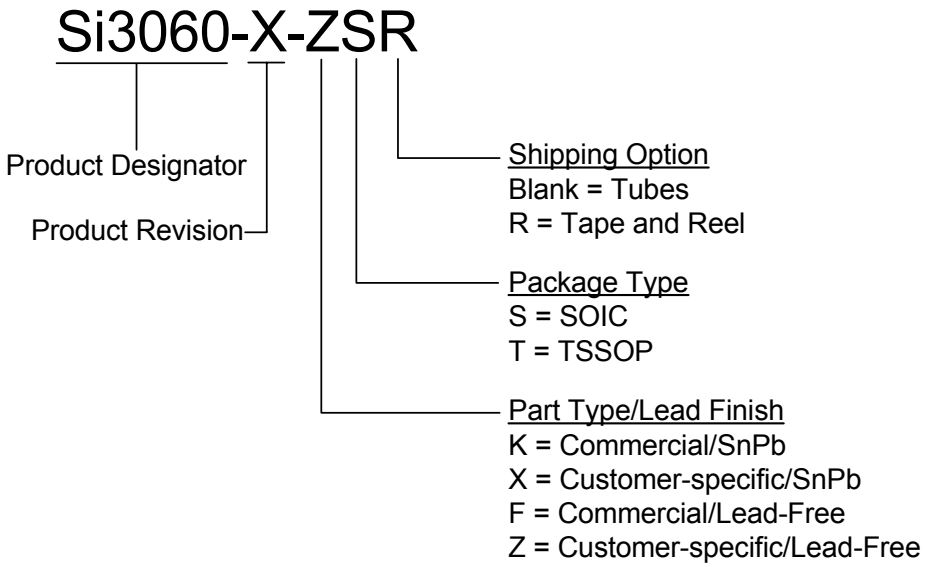
9. Ordering Guide

Device	Interface	Region	Line-Side Part Number	Temperature
Si3060	For use with integrated system-side module only	FCC	Si3060-X-FS	0 to 70 °C
Si3061		Global	Si3061-X-FS	0 to 70 °C
Si3062		Enhanced FCC	Si3062-X-FS	0 to 70 °C
Si3063		Enhanced Global	Si3063-X-FS	0 to 70 °C
Si3064		Enhanced Global Voice	Si3064-X-FS	0 to 70 °C

10. Product Identification

The product identification number is a finished goods part number or is specified by a finished goods part number, such as a special customer part number.

Example:



11. Package Outline: 16-Pin SOIC

Figure 12 illustrates the package details for the Si306x. Table 14 lists the values for the dimensions shown in the illustration.

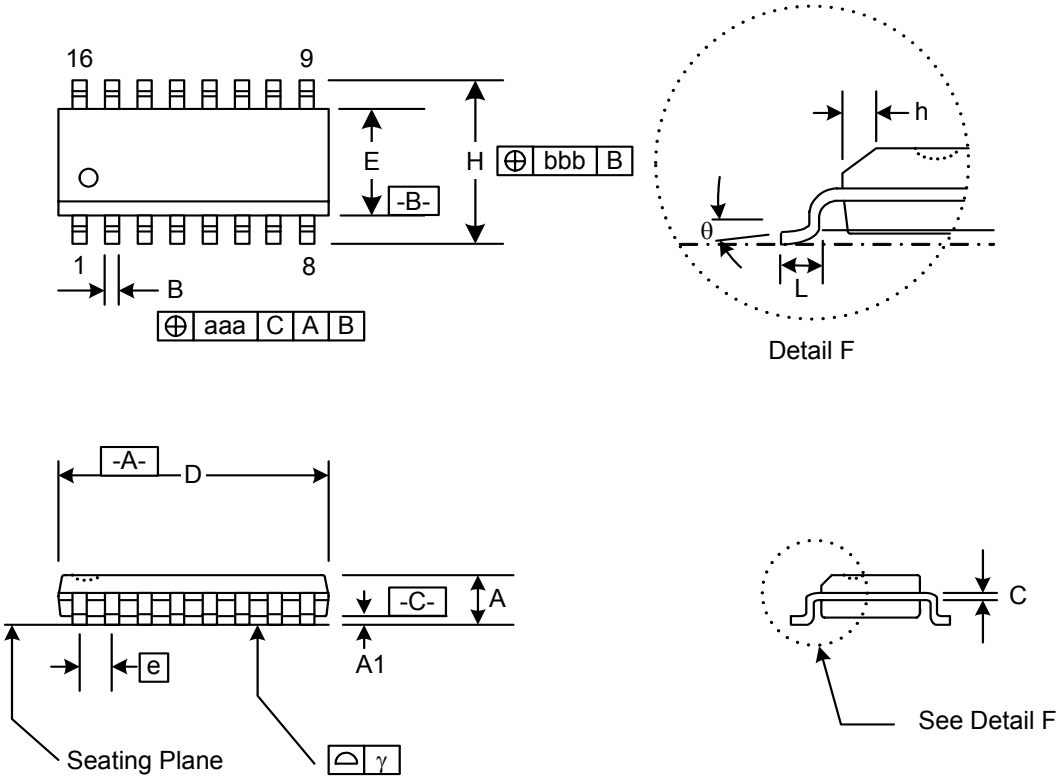


Figure 12. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 14. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	1.35	1.75
A1	.10	.25
B	.33	.51
C	.19	.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	.25	.50
L	.40	1.27
γ	0.10	
θ	0º	8º
aaa	0.25	
bbb	0.25	

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.9

- Updated Figure 3 on page 11.
- Updated Table 2 on page 5.
- Updated Table 4 on page 7.
- Updated Table 6 on page 11.
- Updated Table 7 on page 13.
  - Changed recommended country settings for Australia, Bahrain, Brazil, Bulgaria, China, Croatia, Cyprus, Czech Republic, Egypt, Germany, Hungary, India, Israel, Japan, Jordan, Kazakhstan, Latvia, Lebanon, Malaysia, Malta, Morocco, Nigeria, Oman, Pakistan, Philippines, Poland, Romania, Russia, Slovakia, Slovenia, South Africa, South Korea, Syria, Taiwan, TBR21, Thailand.
- Updated Table 12 on page 28.
- Updated Table 14 on page 60.
- Updated "4. Bill of Materials" on page 10.
- Updated functional description in "5. AOUT PWM Output" on page 11.
- Updated "7. Control Registers" on page 28 and the following register descriptions:
  - Registers 3, 4, 11, 12, 15, 16, 18, 19, 26, 30, 31, 43, 44, and 59.
- Updated "9. Ordering Guide" on page 59.
- Updated "11. Package Outline: 16-Pin SOIC" on page 60.

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