



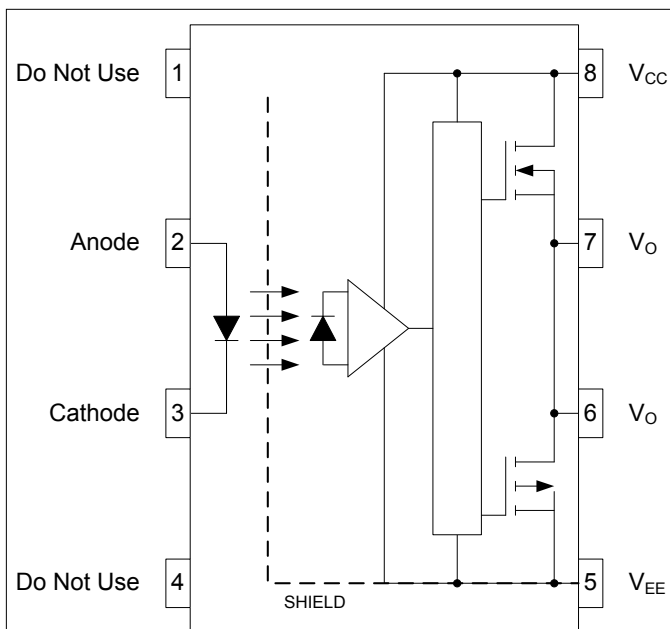
Description

The SI3150 is an optically coupled 0.6A Output Current Gate Driver, designed to drive most 1200V / 50A IGBTs and MOSFETs. It is intended for driving high power IGBTs and MOSFETs used in motor control inverter applications.

The circuit consists of an infrared input LED optically coupled to an integrated circuit which utilizes a high speed driver.

The SI3150 comes standard in a miniature 8 pin DIP package.

Schematic Diagram



SI3150

Truth Table (Positive Logic)

LED	$V_{CC}-V_{EE}$ ("Positive Going") Turn On	$V_{CC}-V_{EE}$ ("Negative Going") Turn Off	V_O
OFF	0 – 30V	0 – 30V	LOW
ON	0 – 11V	0 – 10V	LOW
ON	11.5 – 13.5V	10 – 12V	TRANSITION
ON	13.5 – 30V	12 – 30V	HIGH

**** A 0.1 μ F bypass Capacitor must be connected between pins 5 & 8 (GND & V_{CC})**

Applications

- IGBT / MOSFET Gate Drives
- AC & Brushless DC Motor Drives
- Industrial Inverters
- Uninterruptable Power Supplies (UPS)
- Switch Mode Power Supplies

Features

- High Common Mode Rejection: 15kV/ μ S minimum @ $V_{CM} = 1500V$
- 0.6A Maximum Peak Output Current
- Fast Switching Speeds
 - 500nS Maximum Propagation Delay
- $I_{CC}=3.5mA$ Maximum Supply Current
- Wide Supply Voltage Range (15V to 30V)
- Under Voltage Lockout Protection (UVLO) with Hysteresis
- Broad Temperature Performance Range (-40°C to 100°C)
- Low Power Dissipation ($R_{ON} \leq 1\Omega$)
- Rail-to-Rail Output Voltage
- High Input to Output Isolation (5kV_{RMS})
- RoHS / Pb-Free / REACH Compliant

Agency Approvals

- UL/C-UL approved to UL1577
- VDE approved to EN60747-5-5

Ordering Information

Part Number	Description
SI3150	8 pin DIP, (50/Tube)
SI3150-H	0.40" (10.16mm) Wide Lead Spacing (VDE0884)
SI3150-S	8 pin SMD, (50/Tube)
SI3150-STR	8 pin SMD, Tape and Reel (1000/Reel)

NOTE: Suffixes listed above are not included in marking on device for part number identification

Absolute Maximum Ratings, $T_A = 25^\circ\text{C}$ (unless otherwise specified)

The values indicated are absolute stress ratings. Functional operation of the device is not implied at these or any conditions in excess of those defined in electrical characteristics section of this document. Exposure to absolute Maximum Ratings may cause permanent damage to the device and may adversely affect reliability.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
General Maximum Ratings								
Storage Temperature	T_{ST}	-55	-	125	$^\circ\text{C}$			
Operating Temperature	T_A	-40	-	100	$^\circ\text{C}$			
Isolation Voltage	V_{ISO}	5000	-	-	V_{RMS}			
Supply Voltage	V_{CC}	0	-	35	V			
Solder Temperature – Wave (10 sec)	T_{SOL}	-	-	260	$^\circ\text{C}$			8
Total Power Dissipation	P_T	-	-	295	mW			
Input Maximum Ratings								
Average Forward Input Current	$I_{F(AVG)}$	-	-	25	mA			
Reverse Input Voltage	V_R	-	-	5	V			
Peak Transient Input Current	$I_{F(TRAN)}$	-	-	1	A	<1 μS pulse width, 300pps		
Input Current (Rise / Fall Time)	$t_{r(IN)} / t_{f(IN)}$	-	-	500	nS			
Input Power Dissipation	P_I	-	-	45	mW			9
Output Maximum Ratings								
“High” Peak Output Current	$I_{OH(PEAK)}$	0.6	-	-	A			1
“Low” Peak Output Current	$I_{OL(PEAK)}$	-0.6	-	-	A			1
Output Voltage	V_O	-	-	V_{CC}	V			
Output Power Dissipation	P_O	-	-	250	mW			10

Recommended Operating Conditions

The values indicated are recommended for steady, consistent operation with optimal performance across the operating temperature range.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Recommended Specifications								
Operating Temperature	T_A	-40	-	100	$^\circ\text{C}$			
Supply Voltage	V_{CC}	15	-	30	V			
Input Current (ON)	$I_{FL(ON)}$	7	-	16	mA			
Input Voltage (OFF)	$V_{F(OFF)}$	-3.0	-	0.8	V			

Electrical Characteristics, $T_A = 25^\circ\text{C}$, $V_{EE} = \text{Ground}$ and $V_{CC} = 30\text{V}$ (unless otherwise specified)

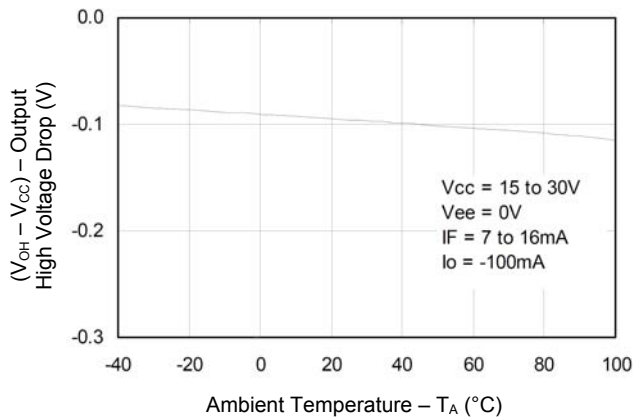
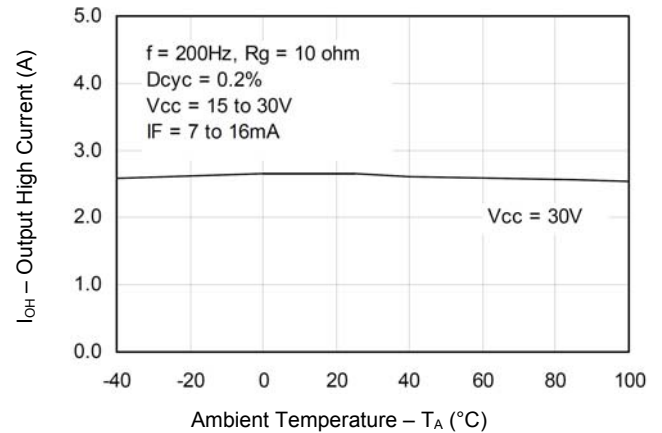
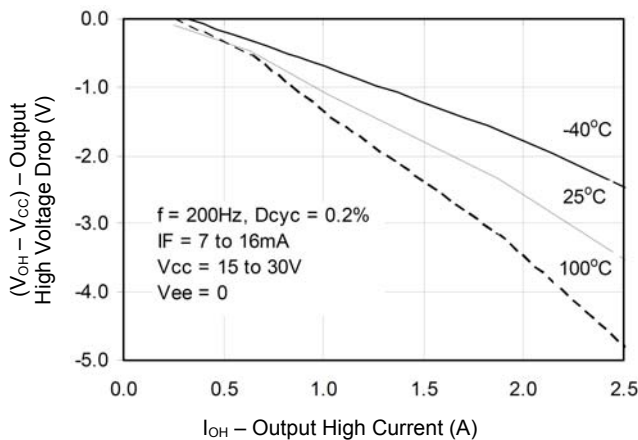
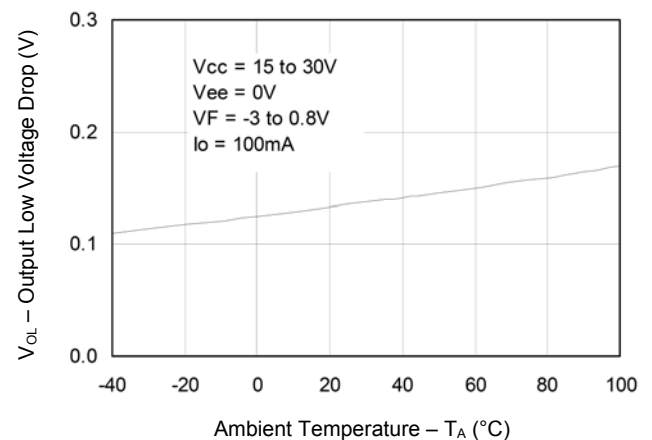
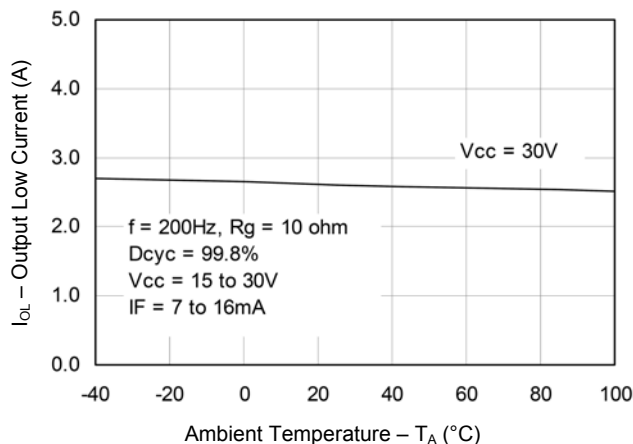
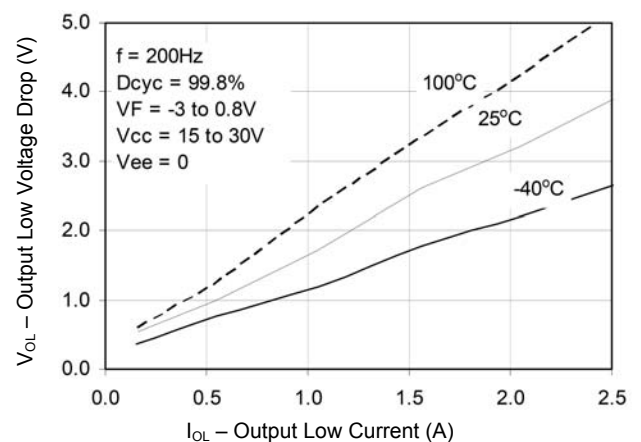
Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Input Specifications								
LED Forward Voltage	V_F	1.2	1.4	1.8	V	$I_F = 10\text{mA}$	15	
LED Forward Voltage Temperature Coefficient	$\Delta V_F / \Delta T$	-	-1.24	-	mV/°C	$I_F = 10\text{mA}$		
LED Reverse Voltage	BV_R	5	-	-	V	$I_R = 10\mu\text{A}$		
Input Threshold Current (Low to High)	I_{FLH}	-	-	5	mA	$V_O > 5\text{V}$, $I_O = 0\text{A}$	9,16,21	
Input Threshold Voltage (High to Low)	V_{FHL}	0.8	-	-	V	$V_O < 5\text{V}$, $I_O = 0\text{A}$		
Input Capacitance	C_{IN}	-	33	-	pF	$f = 1\text{MHz}$, $V_F = 0\text{V}$		
Output Specifications								
High Level Supply Current	I_{CCH}	-	1	3.5	mA	Open V_O , $I_F = 10$ to 16mA	7,8	
Low Level Supply Current	I_{CCL}	-	1	3.5	mA	Open V_O , $V_F = -3$ to $+0.8\text{V}$	7,8	
High Level Output Current	I_{OH}	-0.6	-	-	A	$V_O = (V_{CC} - 6\text{V})$	2,13,19	1
Low Level Output Current	I_{OL}	0.6	-	-	A	$V_O = (V_{CC} + 6\text{V})$	5,6,20	1
High Level Output Voltage	V_{OH}	$V_{CC}-1$	-	-	V	$I_F = 10\text{mA}$, $I_O = -100\text{mA}$	1,3,17	
Low Level Output Voltage	V_{OL}	-	-	$V_{EE}+1$	V	$I_F = 0\text{mA}$, $I_O = 100\text{mA}$	4,16,18	
Under Voltage Lockout Threshold	V_{UVLO+}	11	12.3	13.5	V	$V_O > 5\text{V}$, $I_F = 10\text{mA}$	22	
	V_{UVLO-}	9.5	10.7	12.0	V	$V_O < 5\text{V}$, $I_F = 10\text{mA}$	22	
Under Voltage Lockout Hysteresis	$UVLO_{HYS}$	-	1.6	-	V		22	
Isolation Specifications								
Withstand Insulation Test	V_{ISO}	5000	-	-	V	$RH \leq 40-60\%$, $t = 1$ min		2,3
Input-Output Resistance	R_{I-O}	-	10^{12}	-	Ω	$V_{I-O} = 500\text{V}_{DC}$		2
Input-Output Capacitance	C_{I-O}	-	0.9	-	pF	$f = 1\text{MHz}$		2

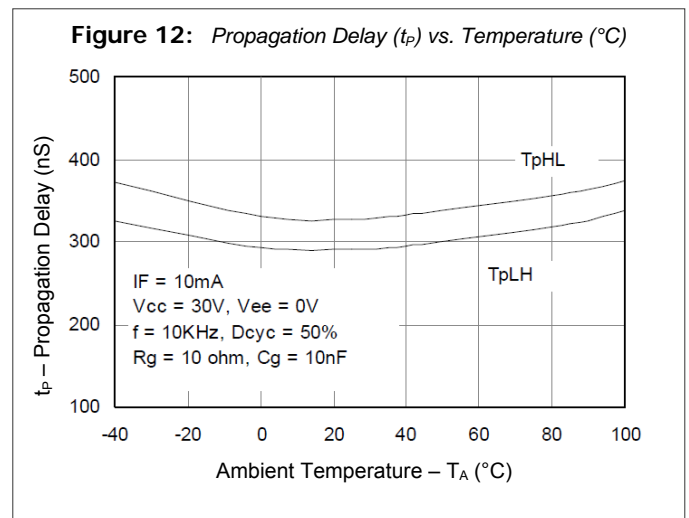
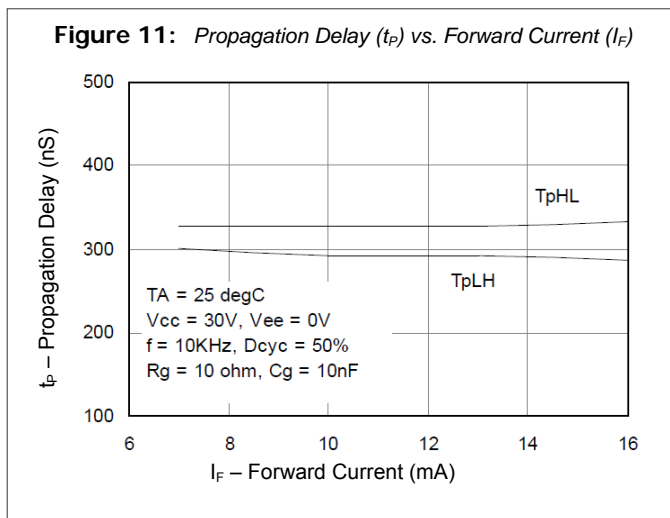
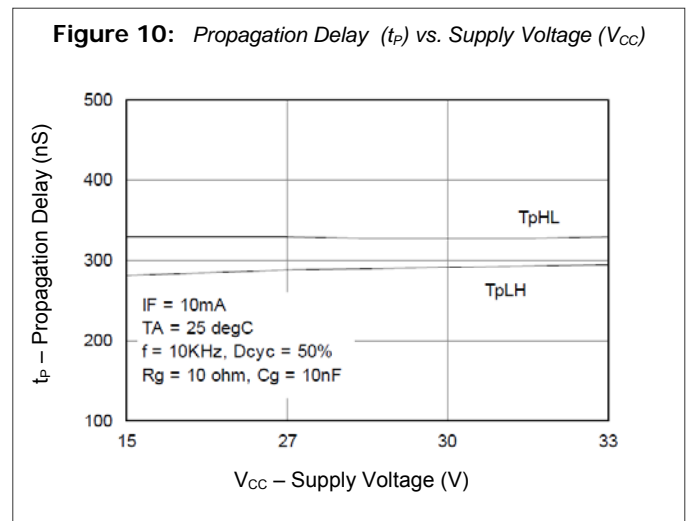
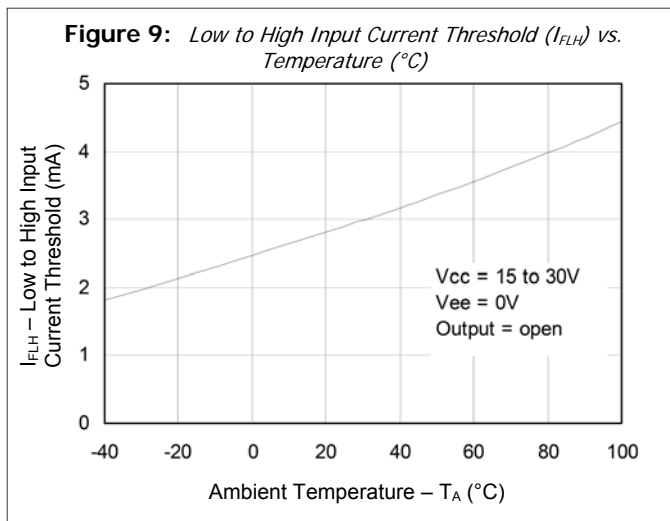
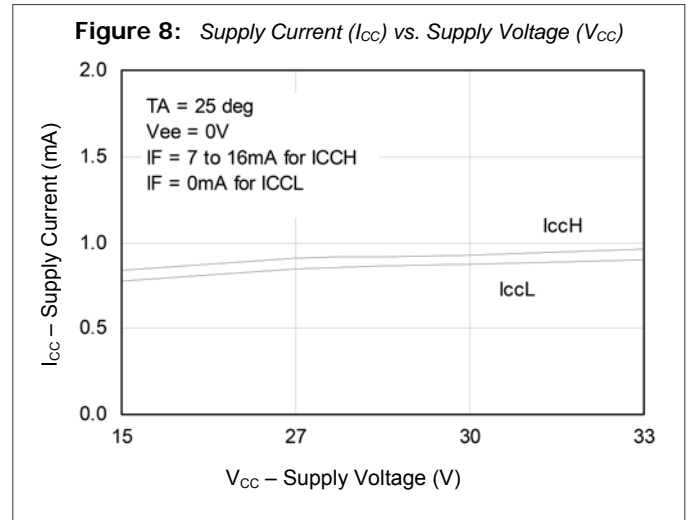
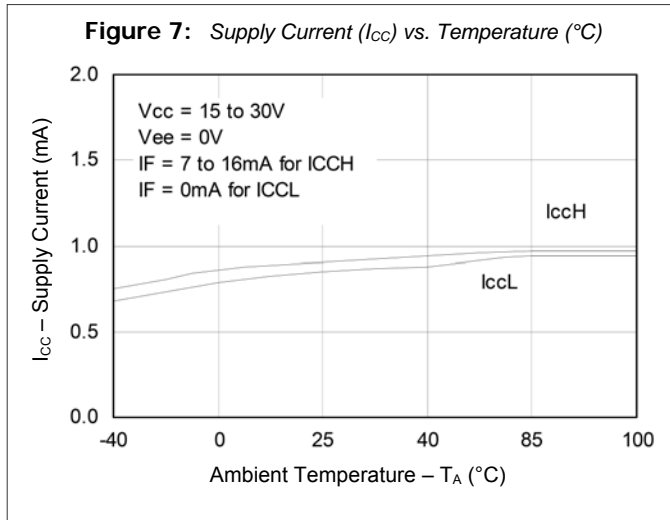
Electrical Characteristics, continued... $T_A = 25^\circ\text{C}$, $V_{EE} = \text{Ground}$ and $V_{CC} = 30\text{V}$ (unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Notes
Switching Specifications								
Propagation Delay Time to High Output Level	t_{PLH}	100	300	500	nS	$I_F = 7$ to 16mA $V_{CC} = 15$ to 30V $V_{EE} = \text{Ground}$ $R_g = 10\Omega$ $C_g = 10\text{nF}$ $f = 10\text{kHz}$ Duty Cycle = 50%	10 11 12 13 14 23	7
Propagation Delay Time to Low Output Level	t_{PHL}	100	300	500				
Pulse Width Distortion	PWD	-	-	300				
Propagation Delay Difference Between Any Two Parts	PDD	-300	-	350			23	4
Output Rise Time (10 to 90%)	t_r	-	75	-				
Output Fall Time (90 – 10%)	t_f	-	50	-				
UVLO Turn On Delay	$t_{UVLO\ ON}$	-	2	-	μS	$I_F = 10\text{mA}$, $V_O > 5\text{V}$		
UVLO Turn Off Delay	$t_{UVLO\ OFF}$	-	0.3	-	μS	$I_F = 10\text{mA}$, $V_O < 5\text{V}$		
Common Mode Transient Immunity at HIGH Level Output	$ CM_H $	15	25	-	$\text{kV}/\mu\text{S}$	$I_F = 7$ to 16mA $V_{CM} = 1500\text{V}$ $T_A = 25^\circ\text{C}$ $V_{CC} = 30\text{V}$	24	5
Common Mode Transient Immunity at LOW Level Output	$ CM_L $	15	25	-	$\text{kV}/\mu\text{S}$	$V_F = 0\text{V}$ $V_{CM} = 1500\text{V}$ $T_A = 25^\circ\text{C}$ $V_{CC} = 30\text{V}$		6

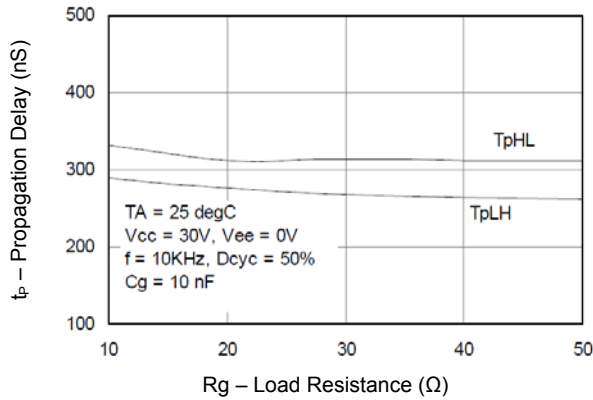
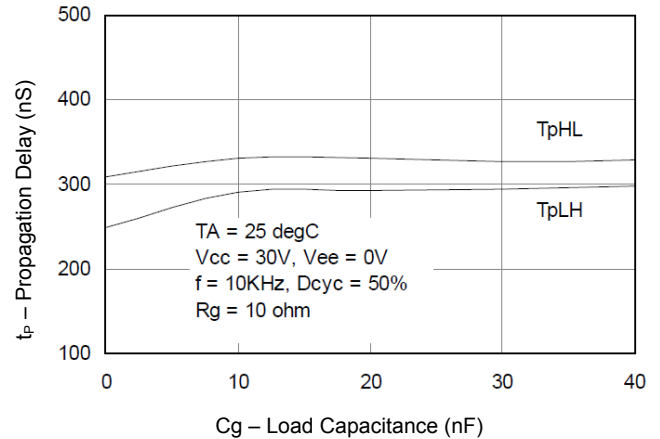
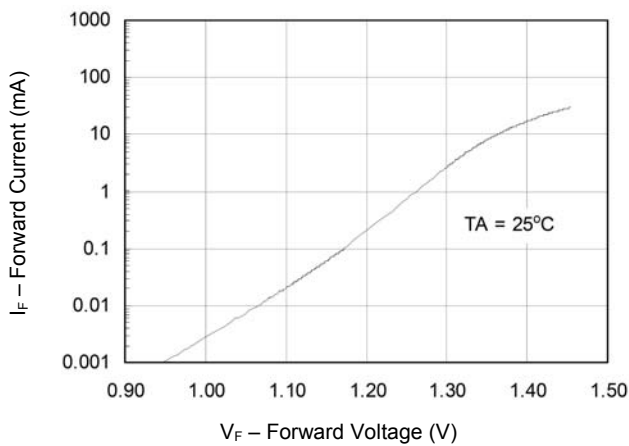
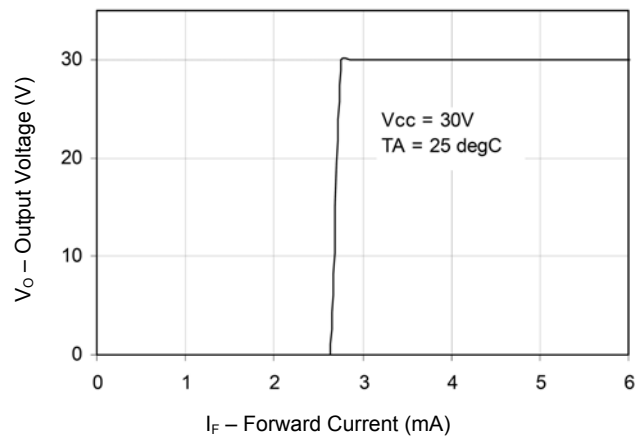
Notes

- Maximum pulse width = $10\mu\text{S}$, maximum duty cycle = 0.2%
- Device is considered a two-terminal device: pins 1, 2, 3, and 4 shorted together, and pins 5, 6, 7, and 8 shorted together
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 6000 V_{RMS}$ for one second (leakage current less than $5\mu\text{A}$)
- The difference between T_{PHL} and T_{PLH} between any two SI3150 devices under the same test conditions
- Common mode transient immunity in HIGH stage is the maximum tolerable negative dV_{CM}/dt on the trailing edge of the common mode impulse signal, V_{CM} , to assure that the output will remain HIGH
- Common mode transient immunity in LOW stage is the maximum tolerable positive dV_{CM}/dt on the leading edge of the common mode impulse signal, V_{CM} , to assure that the output will remain LOW
- Pulse Width Distortion is defined as $|T_{PHL} - T_{PLH}|$ for any given device
- 260°C for 10 seconds. Refer to the lead free solder reflow profile for more information
- Derate linearly above 70°C free air temperature at a rate of $0.47\text{mW} / ^\circ\text{C}$
- Derate linearly above 70°C free air temperature at a rate of $4.8\text{mW} / ^\circ\text{C}$

SI3150 Performance & Characteristics Plots, $T_A = 25^\circ\text{C}$ (unless otherwise specified)
Figure 1: Output High Voltage Drop vs. Temperature ($^\circ\text{C}$)

Figure 2: Output High Current vs. Temperature ($^\circ\text{C}$)

Figure 3: Output High Voltage Drop vs. High Current

Figure 4: Output Low Voltage Drop vs. Temperature ($^\circ\text{C}$)

Figure 5: Output Low Current vs. Temperature ($^\circ\text{C}$)

Figure 6: Output Low Voltage Drop vs. Low Current


SI3150 Performance & Characteristics Plots, continued... $T_A = 25^\circ\text{C}$ (unless otherwise specified)


SI3150 Performance & Characteristics Plots, continued... $T_A = 25^\circ\text{C}$ (unless otherwise specified)

Figure 13: Propagation Delay (t_p) vs. Series Load Resistance (R_g)

Figure 14: Propagation Delay (t_p) vs. Load Capacitance (C_g)

Figure 15: Forward Current (I_F) vs. Forward Voltage (V_F)

Figure 16: Transfer Characteristics


SI3150 Electrical Test Circuits

Figure 17: High Level Output Voltage (V_{OH}) Test Circuit

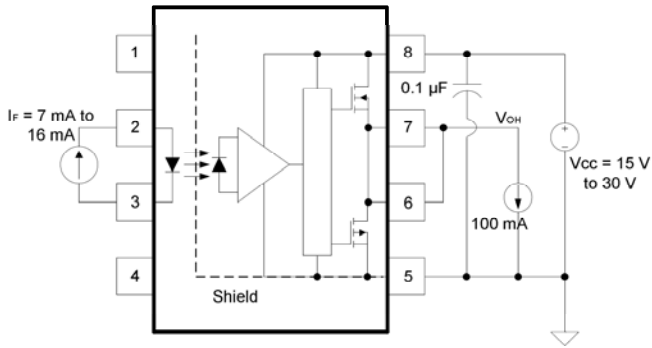


Figure 18: Low Level Output Voltage (V_{OL}) Test Circuit

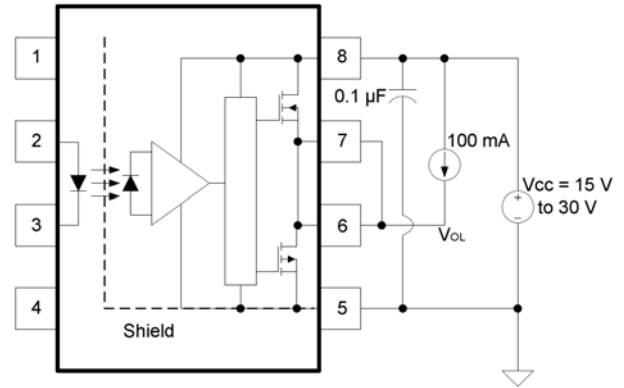


Figure 19: High Level Output Current (I_{OH}) Test Circuit

$I_F = 7\text{mA to }16\text{mA}$
 $PW = 10\mu\text{S}$
Period = 5mS

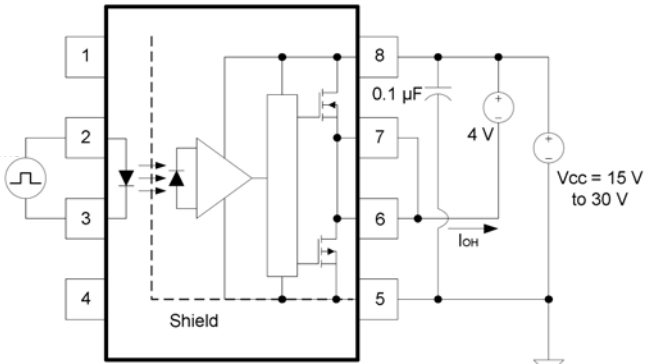


Figure 20: Low Level Output Current (I_{OL}) Test Circuit

$I_F = 7\text{mA to }16\text{mA}$
 $PW = 4.99\text{mS}$
Period = 5mS

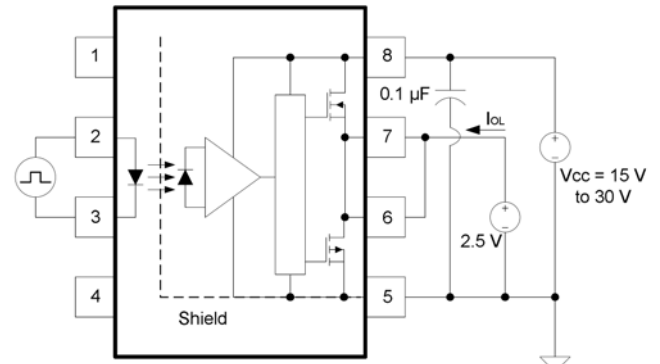


Figure 21: Input Threshold Current (I_{FLH}) Test Circuit

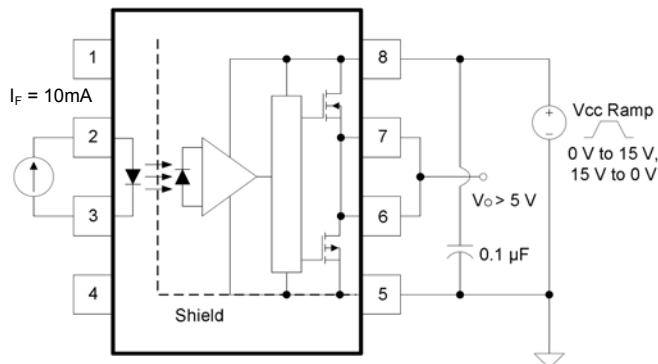
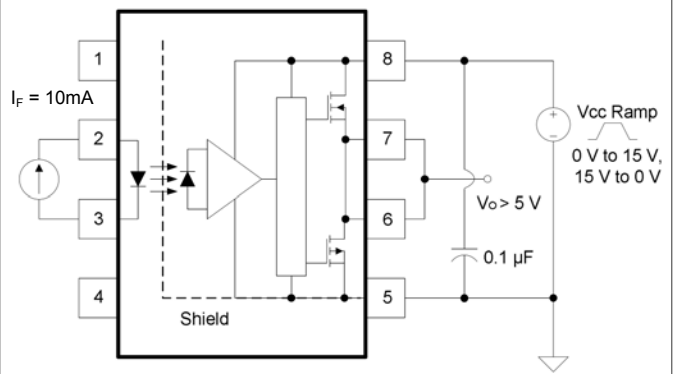


Figure 22: UVLO Test Circuit



SI3150 Electrical Test Circuits, continued...

Figure 23: Rise Time (t_r), Fall Time (t_f), and Propagation Delay Times (t_{PLH} and t_{PHL}) Test Circuit & Waveforms

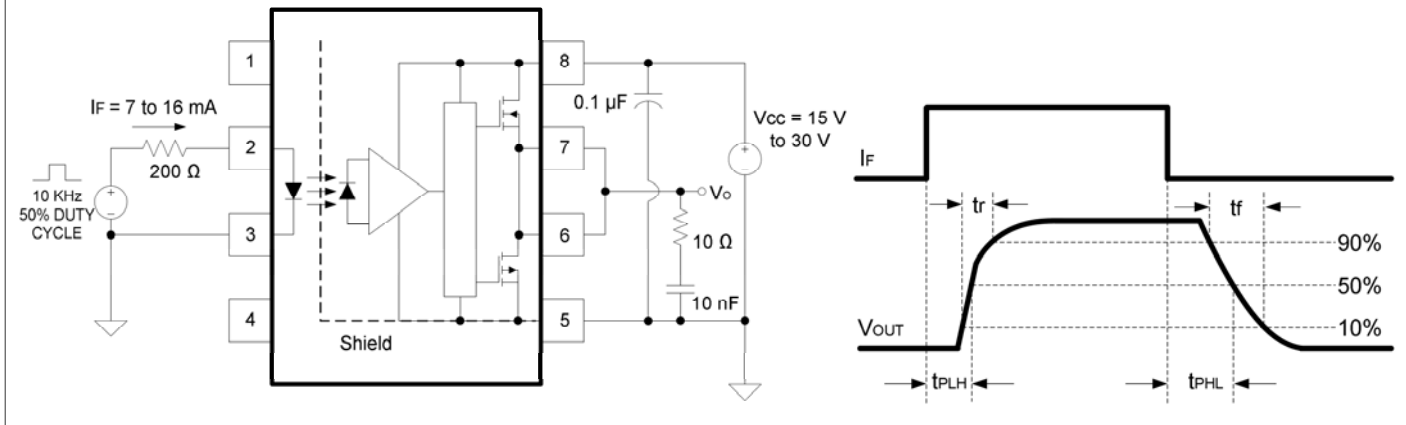
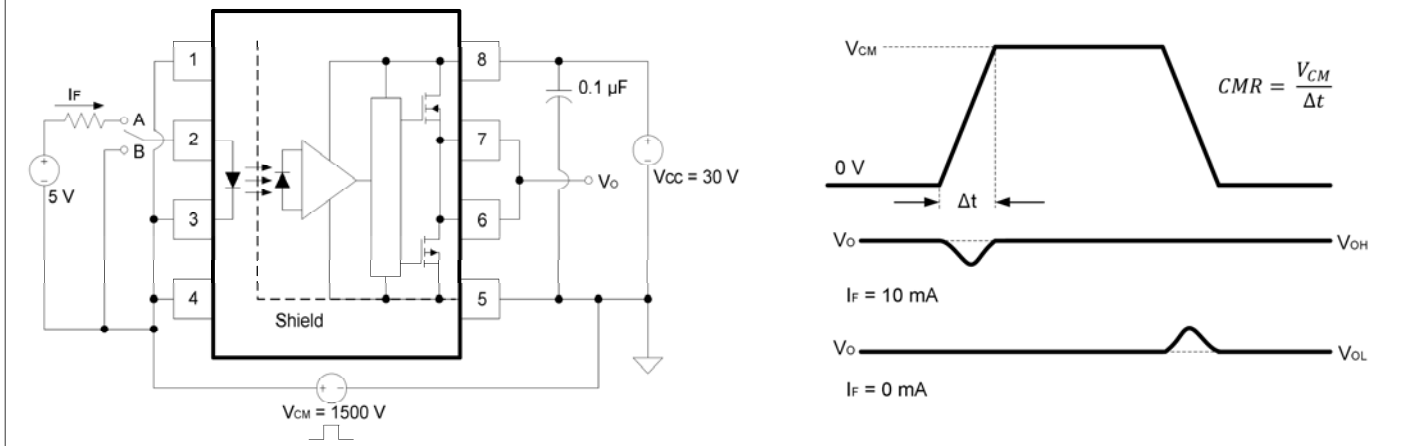
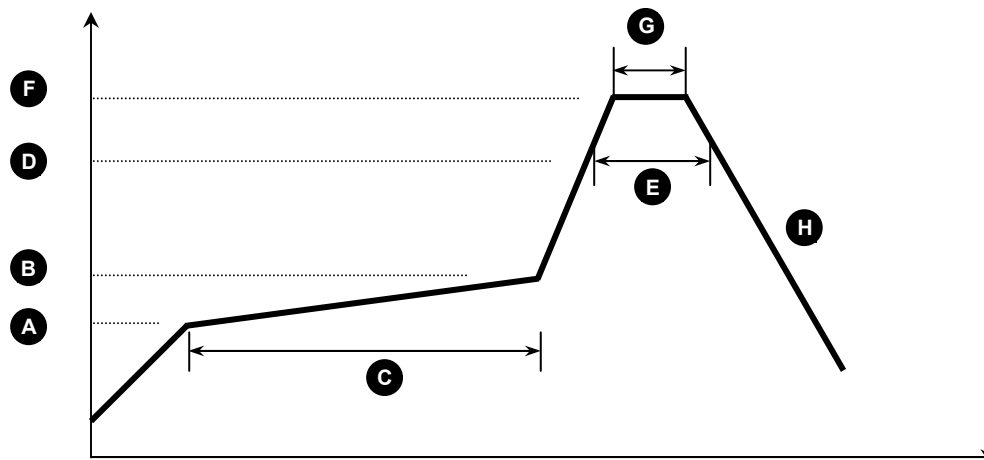


Figure 24: CMR Test Circuit & Waveforms



SI3150 Solder Reflow Temperature Profile Recommendations
(1) Infrared Reflow:

Refer to the following figure as an example of an optimal temperature profile for single occurrence infrared reflow. Soldering process should not exceed temperature or time limits expressed herein. Surface temperature of device package should not exceed 250°C:



Process Step	Description	Parameter
A	Preheat Start Temperature (°C)	150°C
B	Preheat Finish Temperature (°C)	180°C
C	Preheat Time (s)	90 - 120s
D	Melting Temperature (°C)	230°C
E	Time above Melting Temperature (s)	30s
F	Peak Temperature, at Terminal (°C)	260°C
G	Dwell Time at Peak Temperature (s)	10s
H	Cool-down (°C/s)	<6°C/s

(2) Wave Solder:

Maximum Temperature: 260°C (at terminal)
 Maximum Time: 10s
 Pre-heating: 100 - 150°C (30 - 90s)
 Single Occurrence

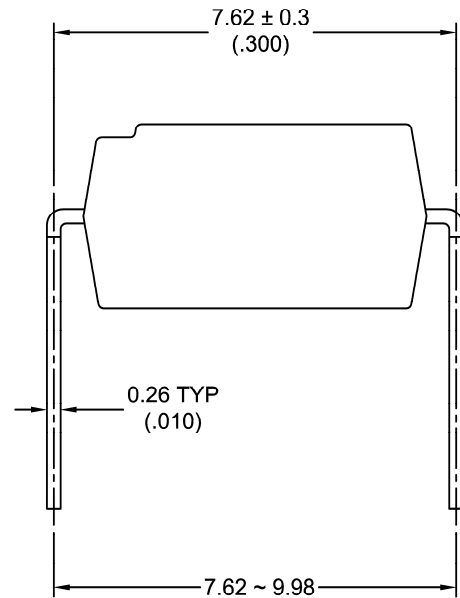
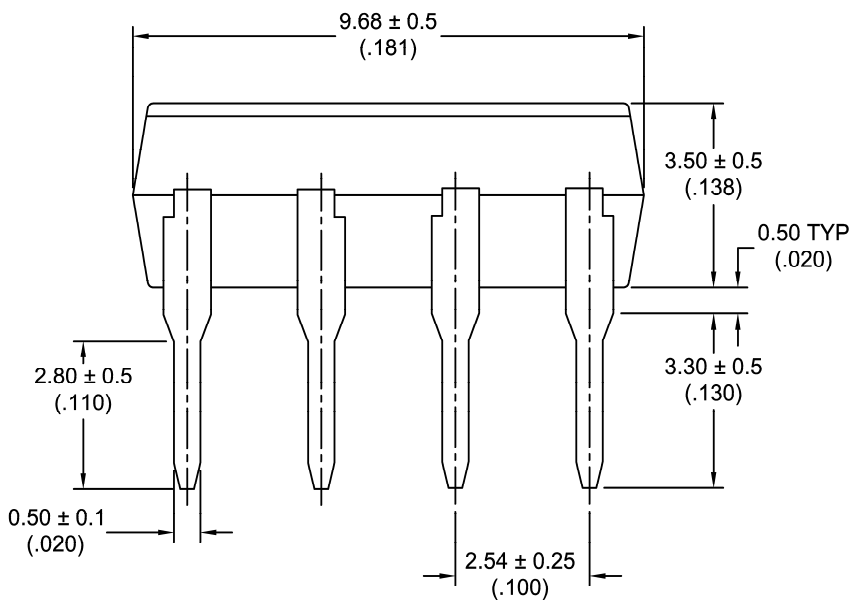
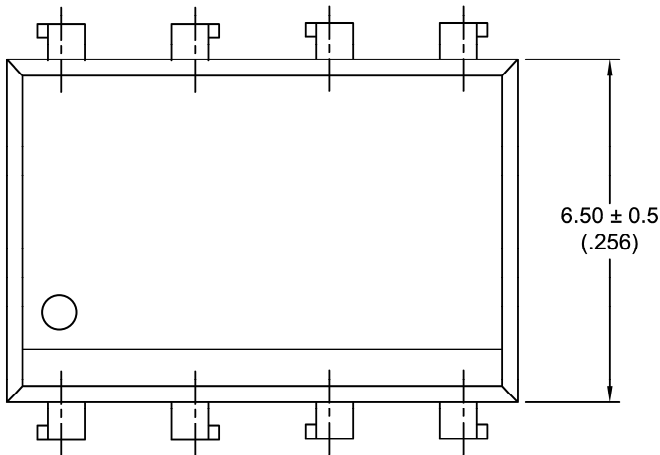
(3) Hand Solder:

Maximum Temperature: 350°C (at tip of soldering iron)
 Maximum Time: 3s
 Single Occurrence

SI3150 Package Dimensions

8 PIN DIP Package

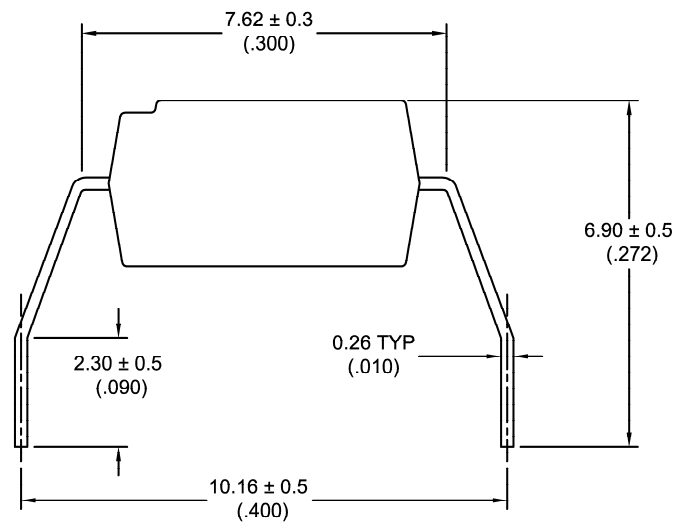
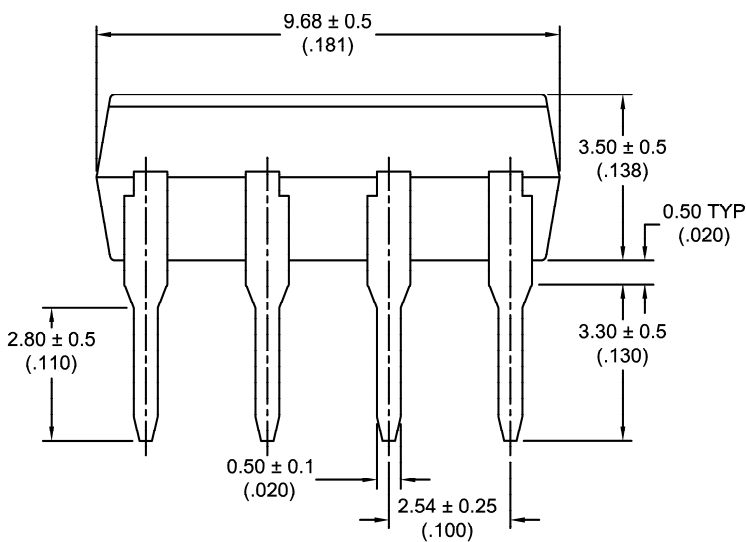
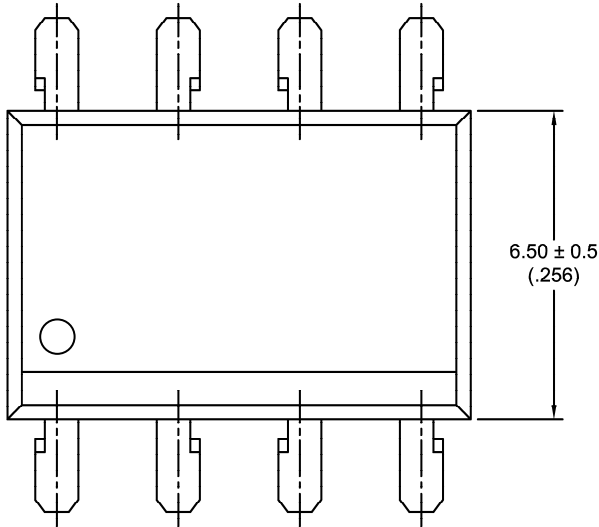
Note: All dimensions in millimeters [mm] with inches in parenthesis ()



SI3150 Package Dimensions

8 PIN WIDE Lead Space Package (-H)

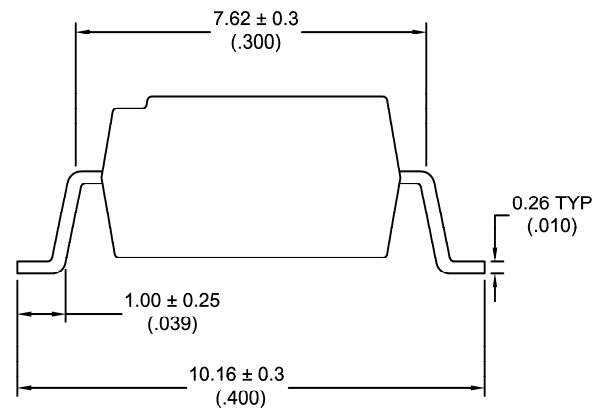
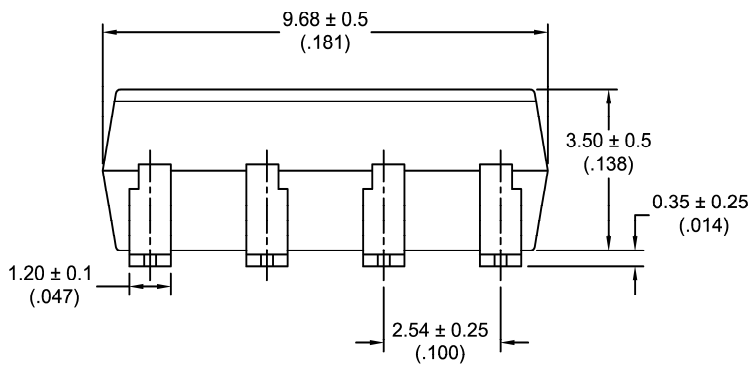
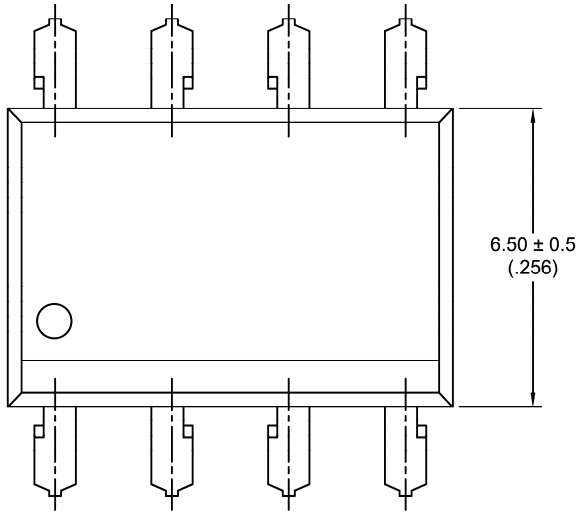
Note: All dimensions in millimeters [mm] with inches in parenthesis ()

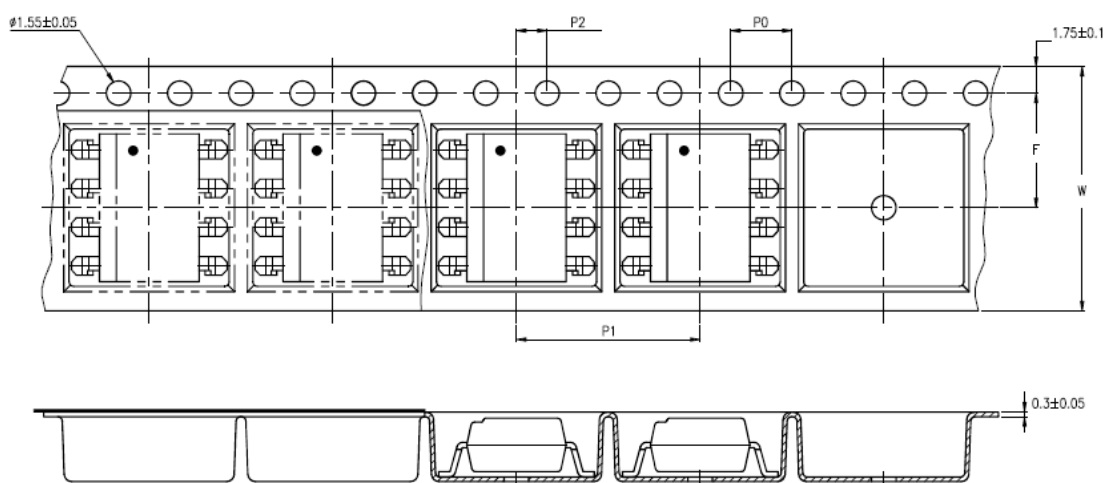


SI3150 Package Dimensions

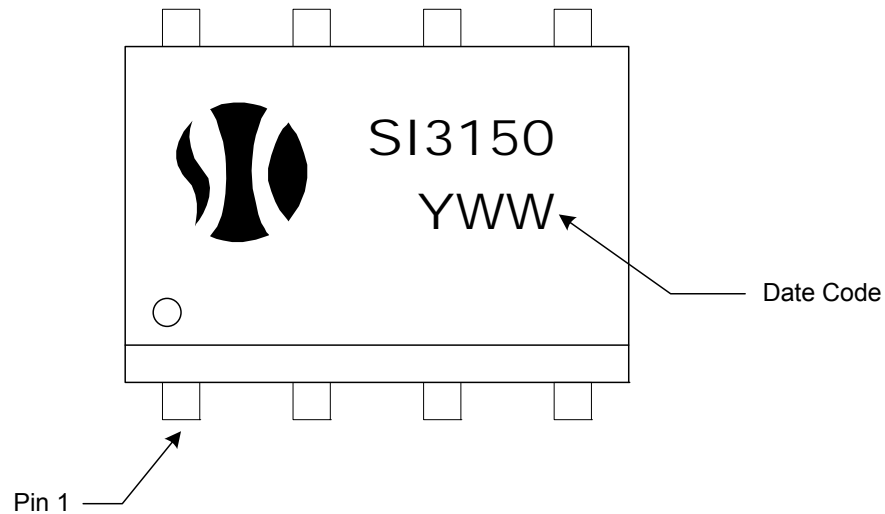
8 PIN SMD Surface Mount Package (-S)

Note: All dimensions in millimeters [mm] with inches in parenthesis ()



SI3150 Packaging Specifications
Tape & Reel Specifications (T&R)
Note: All dimensions in millimeters [mm] with inches in parenthesis ()


Specification	Symbol	Dimensions, mm (inches)
Tape Width	W	16 ± 0.3 (0.63)
Sprocket Hole Pitch	P0	4 ± 0.1 (0.15)
Compartment Location	F P2	7.5 ± 0.1 (0.295) 2 ± 0.1 (0.079)
Compartment Pitch	P1	12 ± 0.1 (0.472)

SI3150 Packaging Marking**DISCLAIMER**

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