

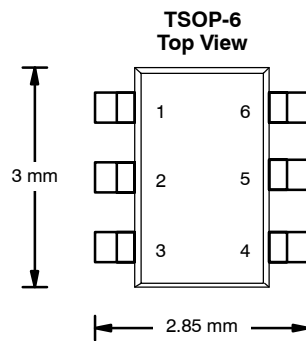
N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY

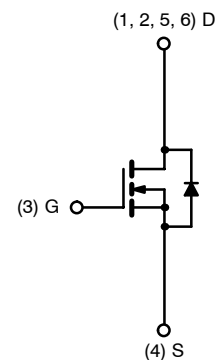
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.170 @ $V_{GS} = 10$ V	2.4
	0.185 @ $V_{GS} = 6.0$ V	2.3

FEATURES

- High-Efficiency PWM Optimized
- 100% R_g Tested



Ordering Information: Si3430DV-T1



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	5 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	100		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 175°C) ^a	T _A = 25°C	I _D	2.4	1.8	A
	T _A = 85°C		1.7	1.3	
Pulsed Drain Current		I _{DM}	8		
Avalanche Current	L = 0.1 mH	I _{AR}	6		
Repetitive Avalanche Energy (Duty Cycle ≤ 1%)		E _{AR}	1.8		mJ
Continuous Source Current (Diode Conduction) ^a		I _S	1.7	1.0	A
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.0	1.14	W
	T _A = 85°C		1.0	0.59	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 5$ sec	R_{thJA}	45	62.5	$^\circ\text{C/W}$
	Steady State		90	110	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	25	30	

Notes

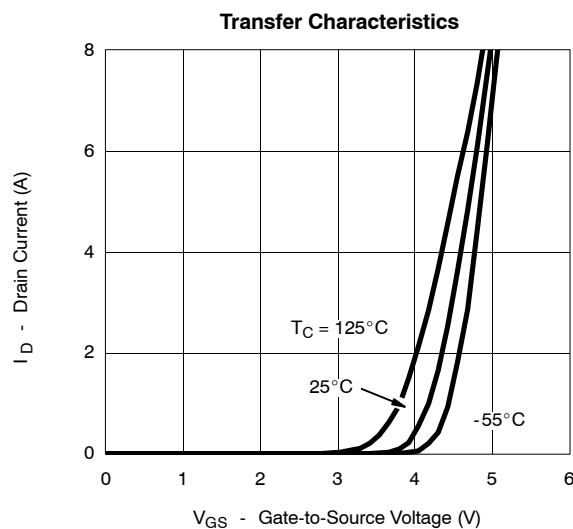
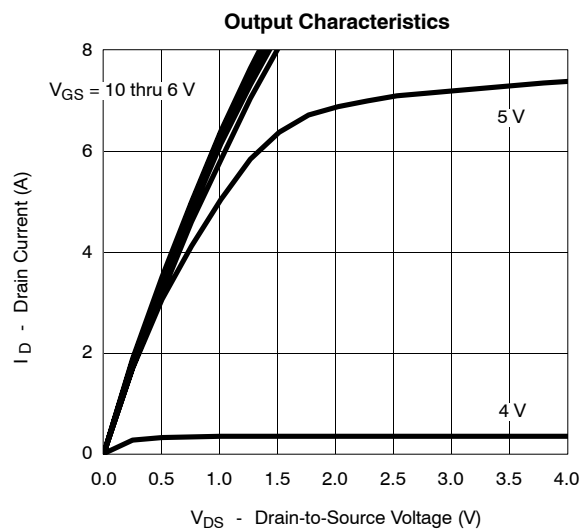
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 85^\circ\text{C}$			25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	8			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 2.4\ \text{A}$		0.148	0.170	Ω
		$V_{GS} = 6.0\ \text{V}$, $I_D = 2.3\ \text{A}$		0.160	0.185	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 2.4\ \text{A}$		7		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 2.4\ \text{A}$		5.5	6.6	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			1.4		
Gate Resistance	R_g		1		4	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ \text{V}$, $R_L = 50\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$		9	20	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			16	30	
Fall Time	t_f			9	20	
Gate Resistance	R_g	$V_{GS} = 0.1\ \text{V}$, $f = 5\ \text{MHz}$		2.8		Ω
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		50	80	ns

Notes

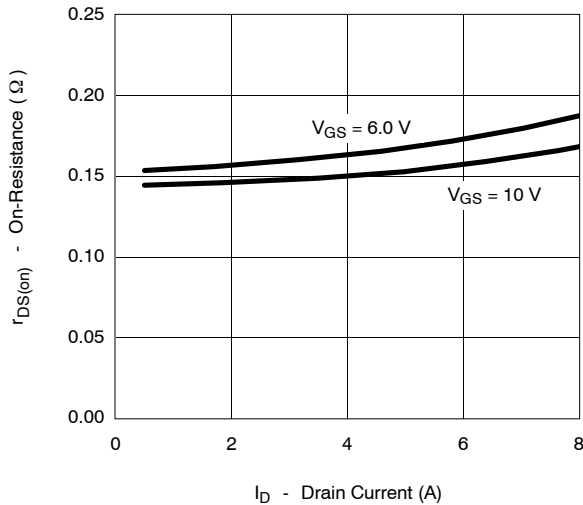
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

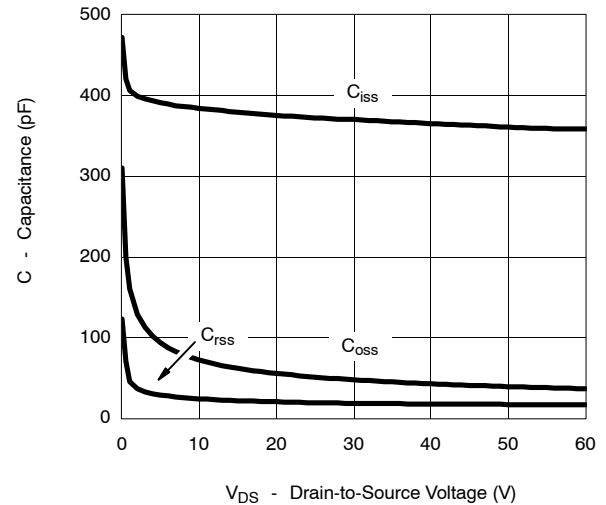


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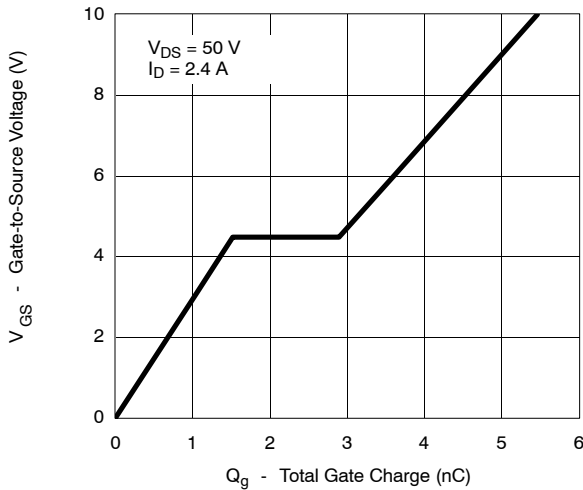
On-Resistance vs. Drain Current



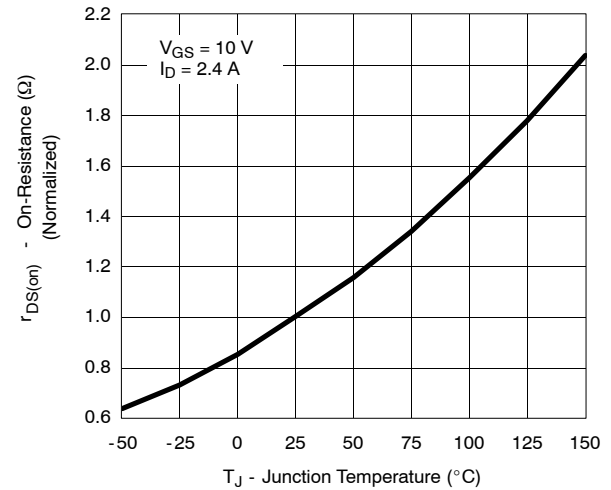
Capacitance



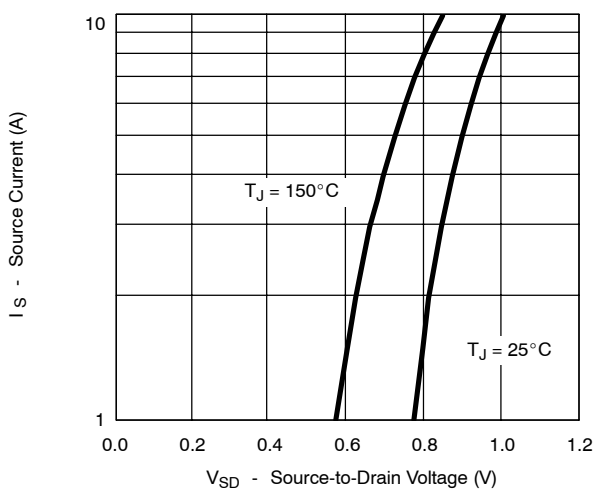
Gate Charge



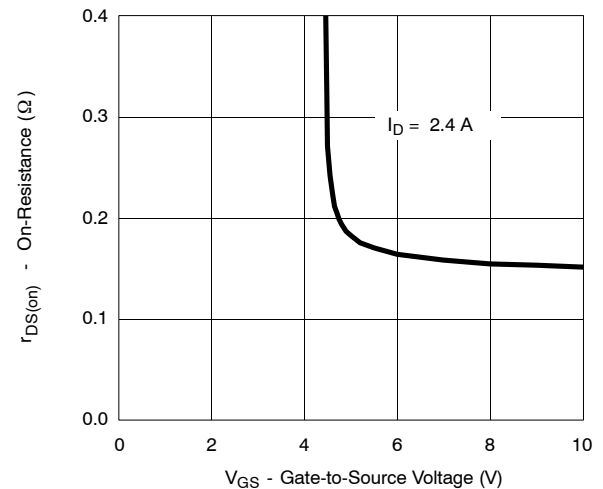
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)
