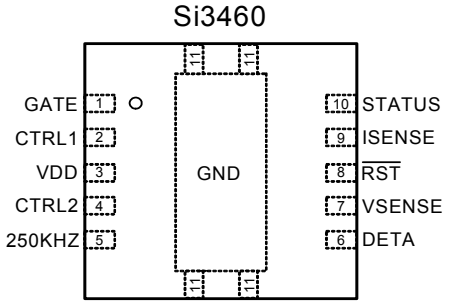
Si3460

IEEE 802.3af PSE INTERFACE AND DC-DC CONTROLLER

Features

- IEEE 802.3af™ compliant PSE and dc-dc controller
- Autonomous operation requires no host processor interface
- Complete reference design available, including Si3460 controller, PSE firmware, and schematic:
  - Low-cost BOM with compact PCB footprint
  - Operates directly from a +12 or +15 V isolated supply
  - dc-dc controller generates –48 V PSE output for SELV compatibility with telephony interfaces
  - Supports up to 15.4 W maximum output power (Class 0)
  - Robust 3-point detection algorithm eliminates false detection events
  - IEEE-compliant classification
  - IEEE-compliant disconnect
  - Inrush current control
  - Short-circuit output fault protection
  - LED status signal (detect, power good, output fault)
- UNH Interoperability Test Lab test report available
- Extended operating range (–40 to +85 °C)
- 11-Pin Quad Flat No-Lead (QFN)
  - Tiny 3 x 3 mm PCB footprint; Pb-free, RoHS-compliant

Pin Assignments



11-pin QFN (3x3 mm)
Top View—Pads on bottom of package

Applications

- IEEE 802.3af endpoints and midspans
- Environment A and B PSEs
- Embedded PSEs
- Set-top boxes
- FTTH media converters
- Cable modem and DSL gateways

Description

The Si3460 is a single-port –48 V power management controller for IEEE 802.3af-compliant Power Sourcing Equipment (PSE). Designed to minimize system cost and ease of implementation in embedded PSE endpoint (switches) or midspan (power injector) applications, the Si3460 operates directly from a 12 or 15 V input supply and integrates a digital PWM-based dc-dc converter for generating the –48 V PSE output supply. The IEEE-required Powered Device (PD) detection feature uses a robust 3-point algorithm to avoid false detection events. The Si3460's reference design kit also provides full IEEE-compliant classification and PD disconnect. Intelligent protection circuitry includes input undervoltage lockout (UVLO), current limiting, and output short circuit protection. The Si3460 is designed to operate completely independently of host processor control. An LED status signal is provided to indicate the port status, including detect, power good, and output fault event information for use within the host system. The Si3460 is pin-programmable to support endpoint and midspan applications, as well as each of the different classification power levels specified by the IEEE 802.3af standard. A comprehensive reference design kit is available (Si3460-EVB), including a complete schematic and BOM (Bill-of-Materials) for the dc-dc converter and PSE functions.

1. Block Diagram

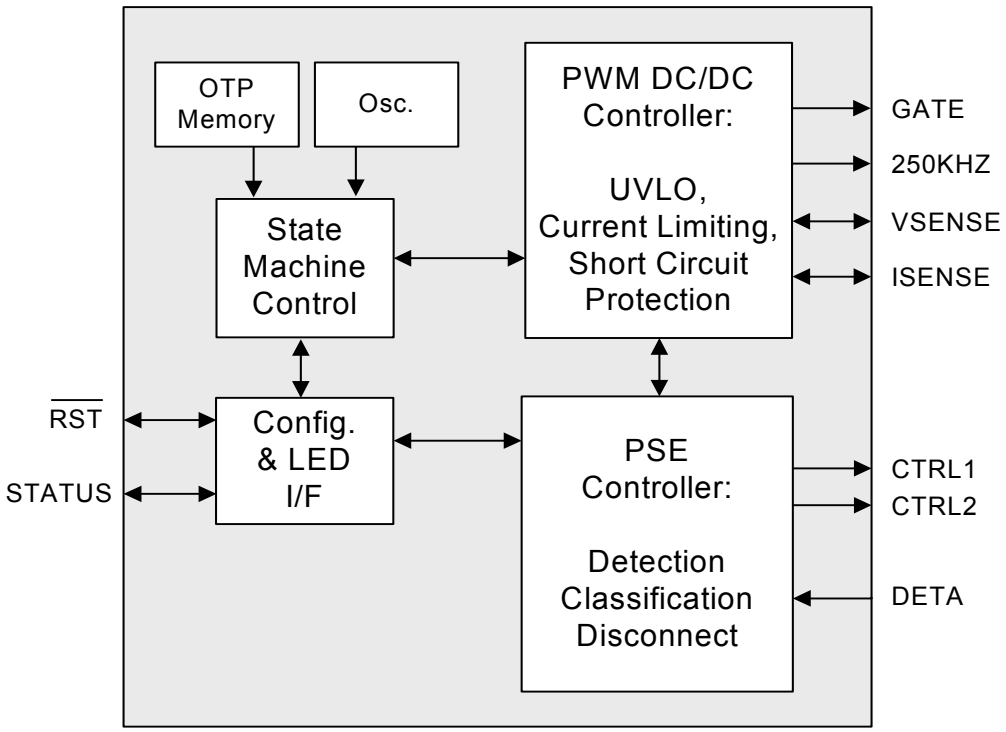
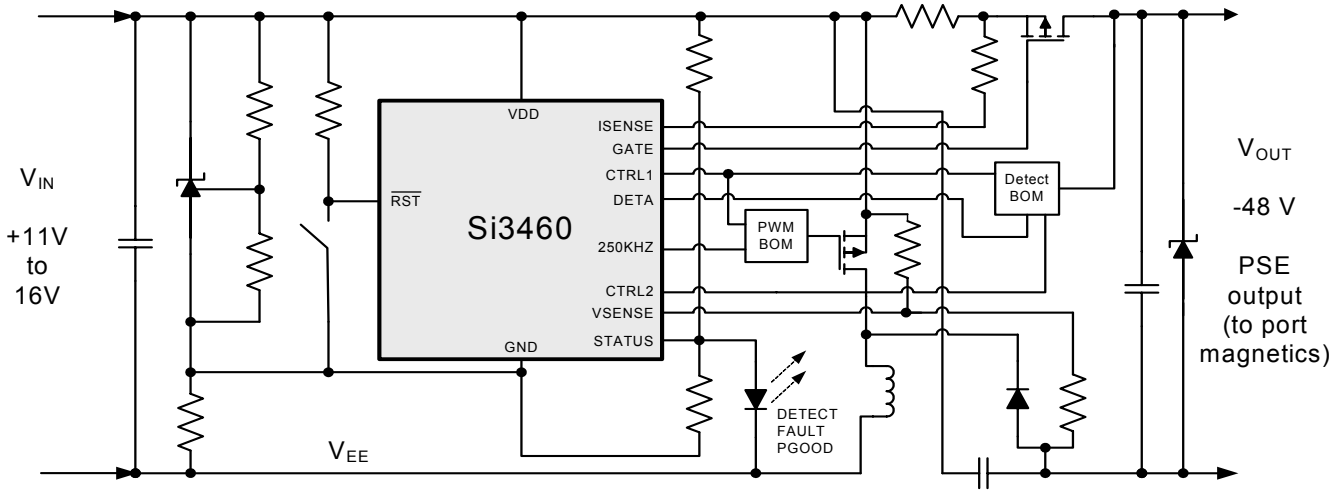


Figure 1. Si3460 Block Diagram

TABLE OF CONTENTS

Section **Page**

2. Si3460-EVB Application Diagram



Note: Refer to the Si3460-EVB User Guide for complete schematic details

Figure 2. Si3460-EVB Application Diagram

2.1. Si3460-EVB Performance Characteristics

When implemented according to the recommended external components and layout guidelines for the Si3460-EVB, the Si3460 enables the following performance specifications in single-port PSE applications. Please refer to the Si3460-EVB User's Guide and schematics for details.

Table 1. Selected Electrical Specifications (Si3460-EVB)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Power Supplies						
V_{IN} input supply range	V_{IN}	–40 to +85 °C ambient range	11	12, 15	16	V
V_{IN} input UVLO voltage	UVLO	UVLO turn-off voltage at V_{IN}	10	—	—	V
VDD supply voltage range	V_{DD}	Si3460 supply voltage range	2.7	3.3	3.6	V
VDD UVLO voltage	V_{DDmin}	Si3460 UVLO turn-off voltage	2.7	—	—	V
Output supply voltage	V_{OUT}	PSE output voltage at V_{IN} = 11 V (min) to 16 V (max)	–54	–50	–46	V
Supply current	I_{IN}	Current into V_{DD} (including gate drive and detect)	—	5	—	mA
Detection Specifications						
Minimum signature resistance	R_{DETmin}		15	17	19	kΩ
Maximum signature resistance	R_{DETmax}		26.5	29	33	kΩ
Classification Specifications						
Classification voltage	V_{CLASS}	0 mA < I_{CLASS} < 45 mA	–20.5	—	–15.5	V
Classification current limit	I_{CLASS}	Measured with 200 Ω across V_{OUT}	55	—	95	mA
Classification current region	I_{CLASS_REGION}	Class 0	0	—	5	mA
		Class 1	8	—	13	mA
		Class 2	16	—	21	mA
		Class 3	25	—	31	mA
		Class 4	35	—	45	mA

Table 1. Selected Electrical Specifications (Si3460-EVB)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Protection and Current Control						
Overload current threshold	I_{CUT}	All class levels	15,400/ V_{OUT}	340	400	mA
Overload current limit	I_{LIM}	Output = 100 Ω across V_{OUT}	400	425	450	mA
Overload time	T_{LIM}	Output = 100 Ω across V_{OUT}	50	60	75	ms
Output power at overload	P_{LIM}		15.4	17	—	W
Disconnect current	I_{MIN}	Disconnect current	5	7.5	10	mA
Efficiency						
System efficiency	η	(P_{IN} @ V_{IN}) to (P_{OUT} @ V_{OUT})	—	75	—	%

3. Si3460 Electrical Specifications

The following specifications apply to the Si3460 controller. Refer to Tables 1, 5, 6, and 7, the Si3460-EVB User's Guide, and schematics for additional details about the electrical specifications of the Si3460-EVB reference design.

Table 2. Recommended Operating Conditions*

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating temperature range	T_A		–40	25	+85	°C
Thermal impedance	θ_{JA}	No airflow		75		°C/W
VDD input supply voltage	VDD	During all operating modes (detect, classification, disconnect)	2.7	3.3	3.6	V
***Note:** VDD = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.						

Table 3. Absolute Maximum Ratings*

Parameter	Conditions	Max Rating	Unit
Ambient temperature under bias		–55 to +125	°C
Storage Temperature		–65 to +150	°C
Voltage on $\overline{RST}$ or any I/O pin with respect to GND	VDD > 2.2 V	–0.3 to 5.8	V
Voltage on VDD with respect to GND		–0.3 to 4.2	V
Maximum total current through VDD and GND		500	mA
Maximum output current into GATE, CTRL1, CTRL2, 250KHZ, STATUS, ISENSE, $\overline{RST}$, VSENSE, DETA (any I/O pin)		100	mA
ESD tolerance	Human Body Model	–2 kV to +2 kV	V
Lead Temperature	Soldering, 10 seconds maximum	260	°C
***Note:** Stresses above those listed in this table may cause permanent device damage. This is a stress rating only, and functional operation of the devices at these or any conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.			

Table 4. Electrical Characteristics*

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Digital Pins: GATE, CTRL1, CTRL2, 250KHZ, STATUS (Output mode), $\overline{RST}$						
Output high voltage	V_{OH}	I_{OH} = –3 mA I_{OH} = –10 µA I_{OH} = –10 mA	0.8 x VDD VDD – 0.1 —	— — 0.7 x VDD	— — —	V
Output low voltage	V_{OL}	I_{OL} = 8.5 mA I_{OL} = 10 µA I_{OL} = 25 mA	— — —	— — 0.4 x VDD	0.6 0.1 —	V
Input high voltage	V_{IH}	Any digital pin	0.7 x VDD			V
Input low voltage	V_{IL}	Any digital pin	—	—	0.3 x VDD	V
Input leakage current	I_{IL}	V_{IN} = 0 V	—	±1	—	µA
Analog Pins: ISENSE, VSENSE, DETA, STATUS (Input mode)						
Input capacitance			—	5	—	pF
Input leakage current	I_{IL}		—	±1	—	µA
***Note:** VDD = 2.7 to 3.6 V, –40 to +85 °C unless otherwise specified.						

4. Si3460-EVB Performance Characteristics

When implemented in accordance with the recommended external components and layout guidelines, the Si3460 controller enables the following typical performance characteristics in single-port PSE applications. Refer to the Si3460-EVB applications note, schematics, and user's guide for more details.

Table 5. PSE Performance Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Protection and Current Control						
Overload current threshold	I_{CUT}	All class levels	15,400/ V_{OUT}	340	400	mA
Overload current limit	I_{LIM}	Output = 100 Ω across V_{OUT}	400	425	450	mA
Overload time	T_{LIM}	Output = 100 Ω across V_{OUT}	50	60	75	ms
Output power at overload	P_{LIM}		15.4	17	—	W
Disconnect current	I_{MIN}	Disconnect current	5	7.5	10	mA
Detection Specifications[2]						
Detection voltage	V_{DET}	Detection point 1 (w/ 10 kΩ source) Detection point 2 (w/ 10 kΩ source) Detection point 3 (w/ 10 kΩ source)		4.5 7.5 4.5		V
Minimum signature resistance	R_{DETmin}		15	17	19	kΩ
Maximum signature resistance	R_{DETmax}		26.5	29	33	kΩ
Classification Specifications[2]						
Classification voltage	V_{CLASS}	0 mA < ICLASS < 45 mA	–20.5		–15.5	V
Classification current limit	I_{CLASS}	Measured with 200 Ω across V_{OUT}	55		95	mA
Classification current region[3]	I_{CLASS_REGION}	Class 0 Class 1 Class 2 Class 3 Class 4	0 8 16 25 35		5 13 21 31 45	mA mA mA mA mA

Notes:
1. Typical specifications are based on an ambient operating temperature of 25 ºC and V_{IN} = +12 V unless otherwise specified.
2. See “4. Si3460-EVB Performance Characteristics” for more details.
3. Absolute classification current limits are programmable.

4.1. PSE Timing Characteristics

When implemented in accordance with the recommended external components and layout guidelines, the Si3460 controller enables the following typical performance characteristics in single-port PSE applications. Refer to the Si3460-EVB applications note, schematics, and user's guide for more details.

Table 6. PSE Timing*

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Endpoint detection delay cycle	t_{DET_CYCLE}	Time from PD connection to port to completion of detection process.	70		400	ms
Detection time	t_{DETECT}	Time required to measure PD signature resistance.		70		ms
Classification delay cycle	t_{CLASS_CYCLE}	Time from successful detect mode to classification complete.	10		50	ms
Classification time	t_{CLASS}		10		50	ms
Power-up turn-on delay	t_{PWRUP}	Time from when a valid detection is completed until V_{OUT} power is applied		30		ms
Midspan detect backoff time	t_{BOM}		2			s
Current limit time	t_{LIM}			60		ms
Disconnect delay	t_{DC_DIS}			350		ms

***Note:** These typical specifications are based on an ambient operating temperature of 25 ºC and V_{IN} = +12 V.

4.1.1. PSE Timing Diagrams

The basic sequence of applying power is shown in Figure 3. Following is the description of the function that must be performed in each phase.

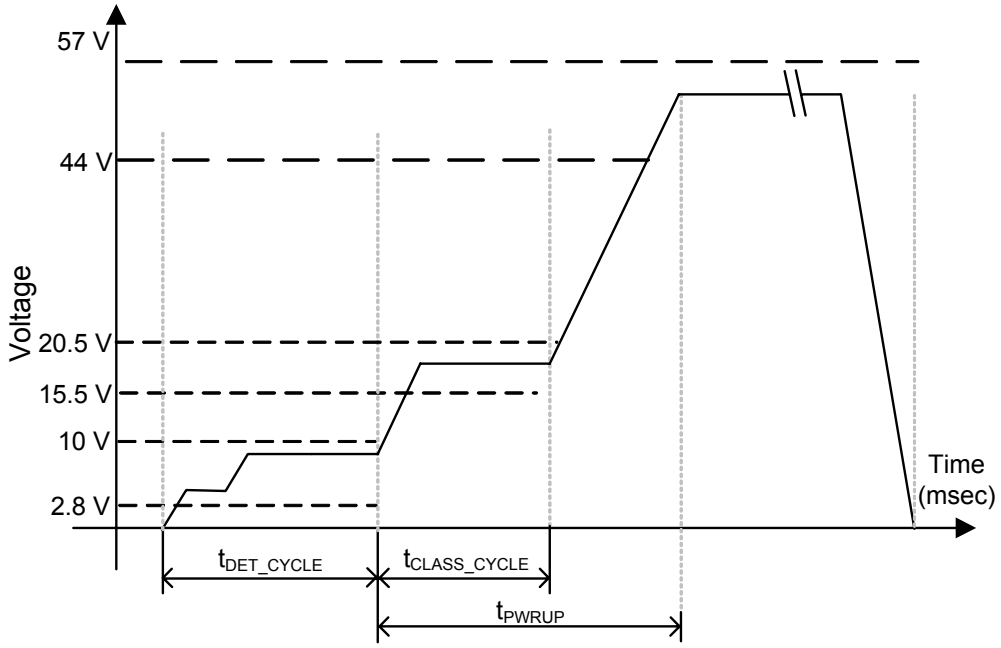


Figure 3. Detection, Classification, Powerup, and Disconnect Sequence

4.2. DC-DC Converter Performance Characteristics

The dc-dc converter utilizes a digital control loop architecture operating at 250 kHz. The complete converter is comprised of the Si3460 controller and the external components in the Si3460-EVB schematics. The performance specifications in Table 7 are typical for the Si3460-EVB reference design.

Table 7. DC-DC Performance[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC-DC Controller Performance Characteristics[2]						
PWM operating frequency	f_{PWM}			250		kHz
Efficiency	η	V_{IN} to V_{OUT}		75		%
Load regulation	R_{LOAD}	Minimum to maximum load		±1		%
Line regulation	R_{LINE}	For V_{IN} ranging from 11 to 16 V		±1		%
Output ripple	R	250 kHz PWM frequency < 500 Hz		100 200		mV

Notes:
1. Typical specifications are based on an ambient operating temperature of 25 ºC and V_{IN} = +12 V.
2. See “4. Si3460-EVB Performance Characteristics” for more details.

5. Si3460-EVB Functional Description

In combination with low-cost external components, the Si3460 controller provides a complete PSE solution for embedded PoE applications. Included in the Si3460-EVB reference design is a digital PWM controller-based dc-dc converter that simplifies overall system design by generating the –48 V PSE supply voltage. An isolated 11 to 16 V input dc supply is all that is needed to supply the Si3460-EVB reference design. Refer to the Si3460-EVB User's Guide and schematics for descriptions in the following sections.

5.1. Reset State

At powerup or if reset is held low, the Si3460 is in an inactive state with the PWM turned off (the switcher FET, M1, is off) and the pass FET, M2, is off.

5.2. Operating Mode Configuration

At powerup, the Si3460 reads the voltage on the STATUS pin, which is set by a resistor divider from V_{EE} to chip ground. The STATUS pin voltage level configures all of the Si3460's operating modes as summarized in Table 8.

Table 8. Operating Modes

STATUS Pin Voltage	Operating Mode			
	Power Level Supported (W)	Classes Supported	Midspan/ Endpoint	Restart Action on Fault or Overload Event Condition
Pin voltage at V_{EE} (no resistors populated)	15.4	All class levels	Endpoint	Auto restart after 2 s
3.0 V	7.0	Class 1 or 2	Endpoint	Auto restart after 2 s
2.75 V	4.0	Class 1	Endpoint	Auto restart after 2 s
2.5 V	15.4	All class levels	Endpoint	Restart on $\overline{RST}$
2.25 V	7.0	Class 1 or 2	Endpoint	Restart on $\overline{RST}$
2.0 V	4.0	Class 1	Endpoint	Restart on $\overline{RST}$
1.75 V	4.0	Class 1	Midspan	Restart on $\overline{RST}$
1.5 V	7.0	Class 1 or 2	Midspan	Restart on $\overline{RST}$
1.25 V	15.4	All class levels	Midspan	Restart on $\overline{RST}$
1.0 V	4.0	Class 1	Midspan	Auto restart after 2 s
0.5 V	7.0	Class 1 or 2	Midspan	Auto restart after 2 s
< 0.25 V (pullup resistor only)	15.4	All class levels	Midspan	Auto restart after 2 s

After powerup, the STATUS pin drives the base of a PNP transistor that controls an LED. To maintain an accurate voltage level at the transistor base, it is recommended that the parallel resistance setting the pin voltage be less than 1 kΩ.

5.3. Operating Mode Sequencing

5.3.1. Detection

After powerup and passing the UVLO threshold voltage of 10 V, the Si3460 enters into the detection state, with FET M2 off and the dc-dc converter disabled so as to generate no output. Prior to turning on the PSE output FET M2 and enabling the 250 kHz square wave for the dc-dc converter, a valid detection sequence must take place.

According to the IEEE specifications, the detection process consists of sensing a nominal 25 kΩ signature resistance in parallel with up to 0.15 µF of capacitance. To eliminate the possibility of false detection events, the Si3460-EVB reference design performs a robust 3-point detection sequence by varying the voltage across the sense bridge R1, R2, and R3. The fourth leg of the sense bridge is the load that connects to the drain of M2 and returns to V_{EE} via D8 and L1.

At the beginning of the detection sequence, V_{OUT} is at zero output voltage for 250 ms. With a 10 kΩ source impedance, V_{OUT} is then varied from 4.5 to 7.5 V and then back to 4.5 V for 20 ms at each level. If the PD's signature resistance is in the RGOOD range of 19 to 26.5 kΩ, the Si3460 proceeds to classification and powerup. If the PD resistance is not in this range, the detection sequence repeats continuously.

Detection is sequenced approximately every 320 msec and repeats until RGOOD is sensed, indicating a valid PD has been detected. The STATUS LED (D13) is flashed at the 320 ms rate in synchronization with the detection process to indicate the PSE is searching for a valid PD.

5.3.2. Classification

After a valid PD is detected, the pass transistor, M2, and the PWM controller are turned on and programmed for an output voltage of 18 V with a current limit of 75 mA. The current measured during the classification process determines the class level of the PD. If the class level of the PD is not within the supported level as set by the initial voltage on the Si3460's STATUS pin (refer to the Operating Mode Configuration section above), an error is declared and the LED blinks rapidly. If the class level is in the supported range, the Si3460 proceeds to powerup. Classification level is determined according to the current at ISENSE as shown in Table 9.

Table 9. Classification Levels

ISENSE Current (Nominal)	Classification Level	Minimum Power Level
< 6.5 mA	Class 0	15.4 W
6.5mA to 14.5 mA	Class 1	4 W
14.5 mA to 23 mA	Class 2	7 W
> 23 mA	Class 3 or 4	15.4 W

If the classification level is at a greater power than can be supported based on R28 and R30, an error condition is reported by flashing the LED at a 10 Hz rate for two seconds before the state machine goes back to the detection cycle.

5.3.3. DC-DC Converter Ramp-Up

After the optional classification sequence, the dc-dc converter is powered up to –50 V with a current limit corresponding to 430 mA. After powerup, power is applied to V_{OUT} as long as there is not an overcurrent fault, disconnect, or input undervoltage (UVLO) condition. The STATUS LED is continuously lit when power is applied. If the output power exceeds the level determined by the initial voltage of the STATUS pin, the Si3460 will declare an error and shut down the port, flashing the LED rapidly to indicate the error (for either two seconds or until reset as determined by the initial voltage on the STATUS pin).

5.3.4. DC-DC Converter Soft Start

The PWM control loop of the dc-dc converter is designed to produce a gradual rise in output voltage to eliminate any inrush current issues. The nominal set point of the dc-dc converter is –50 V. V_{OUT} at –50 V results in 0.930 V at the VSENSE pin. It is possible for there to be almost no load on the dc-dc converter; so, the duty cycle is ramped slowly up to the dc set point. The duty cycle is initially set to zero (dc-dc converter off). Once the desired voltage set point is reached, the feedback path from VSENSE is enabled, and the converter is allowed to regulate at the desired set point.

5.3.5. Disconnect

The Si3460 implements a robust disconnect algorithm. If the output current level drops below 7.5 mA (nominal) for more than 350 msec, the Si3460 will declare a PD disconnect, and the dc-dc converter clock (250 kHz) and FET M1 will be turned off. As set by the initial voltage on the STATUS pin, the Si3460 will then automatically resume the detection process after 250 ms for "Endpoint mode" and two seconds for "Midspan mode." The difference in these two backoff timings is specified by the IEE 802.3af standard for the midspan and endpoint operating modes.

5.3.6. Current Limit Control

The Si3460's overcurrent trip point is set to 340 mA (nominal), corresponding to 17 W of output power for a nominal V_{OUT} voltage of –50 V. If the output current exceeds 340 mA, a timer counts up towards a time-out of 60 ms. If the current drops below 340 mA, the timer counts down towards zero at 1/16th the rate. If the timer reaches 60 msec, an overcurrent fault is declared, and the channel is shut down by turning off the dc-dc converter clock and then turning off FET M1. After an overcurrent fault event, the LED is flashed rapidly. As set by the initial voltage on the STATUS pin at power-up, the Si3460 will then either automatically resume the detection process (restart on fault or overload mode) or wait until $\overline{RST}$ is asserted (restart on reset) before the detect process resumes.

5.3.7. UVLO

The Si3460-EVB reference design is optimized for 12 to 15 V nominal input voltages (11 V min to 16 V maximum). If the input voltage drops below 10 V in detection mode or if the output voltage drops below 10 V in classification or powerup mode, a UVLO condition is declared, which generates the error condition (LED flashing rapidly). An undervoltage event is a fault condition reported through the status LED as a rapid blinking of 10 flashes per second. The UVLO condition is continuously monitored in all operating states.

5.3.8. Status LED Function

During the normal detection sequence, the STATUS LED flashes approximately three times per second as the detection process continues. After successful powerup, the LED glows continuously. If there is an error condition (i.e. class level is beyond programmed value or a fault or overcurrent condition has been detected), the LED flashes rapidly 10 times per second). This occurs for two seconds for normal error delay and will continue until reset if this operational mode is set.

If the Powered Device (PD) is disconnected so that a disconnect event occurs, the LED will start flashing three times per second once the detect process resumes.

6. Design Considerations

6.1. Isolation

The Si3460-EVB's PSE output power at V_{OUT} is not isolated from the input power source (V_{IN}). Isolation of PSE output power requires that the input be isolated from earth ground. Typically, an ac to dc power supply or "wall wart" is used to provide the 12 V power so the output of this supply is isolated from earth ground.

6.2. External Component Selection

Detailed notes on external component selection are provided in the Si3460-EVB User's Guide schematics and BOM. In general, these recommendations must be followed closely to ensure output power stability and ripple (power stage components), surge protection (surge protection diode), and overall IEEE 802.3 compliance.

6.3. Input DC Supply

The input power supply should be rated for at least 25% higher power level than the output power level chosen. This is primarily to account for the 75 to 80% nominal efficiency performance of the Si3460-EVB reference design. For example, to support a Class 0 PSE, for example, the input supply should be capable of supplying 19.25 W (15.4 W x 1.25 = 19.25 W).

6.4. STATUS and RESET Interface

To reference the RESET and STATUS pins to system ground, the level shifting method shown in Figure 4 can be used. Refer to the schematic in the Si3460-EVB document.

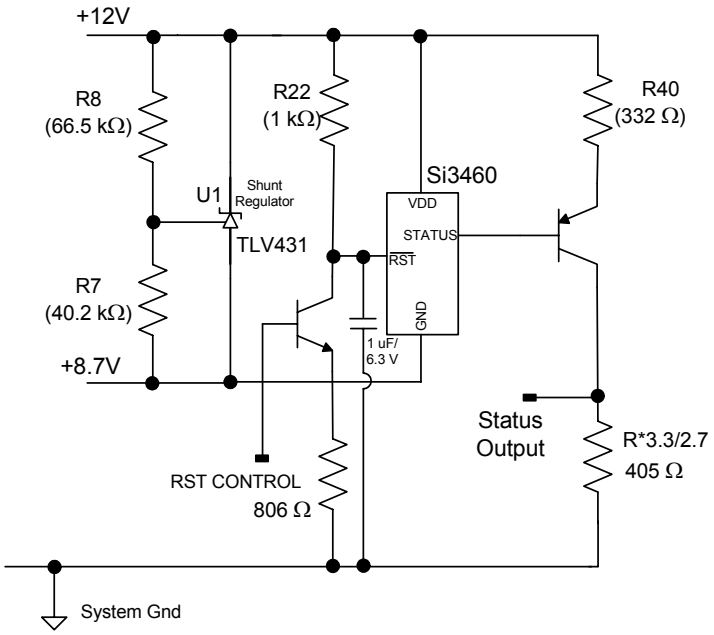


Figure 4. STATUS and RESET Pin Interface when Referenced to System Ground

7. Si3460 Pin Descriptions

Si3460 pin functionality is described in Table 10. Note that the information applies to the Si3460 device pins, while the Si3460-EVB User's Guide describes the inputs and outputs of the evaluation system.

The electrical characteristics of the Si3460-EVB are summarized in Table 1, "Si3460-EVB Performance Characteristics Summary," on page 4. Refer to the complete Si3460-EVB schematics and BOM listing for information about the external components needed for the complete PSE and dc-dc controller application circuit.

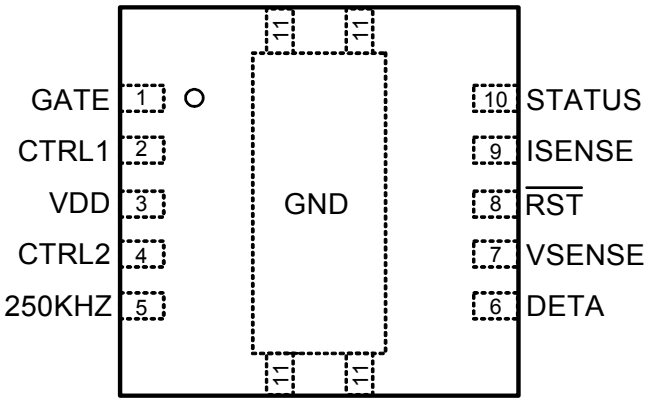


Table 10. Si3460 Pin Functionality

Pin #	Pin Name	Pin Type	Pin Function
1	GATE	Digital output	A logic low on this pin turns on the output FET to enable the PSE output voltage. Refer to the Si3460-EVB schematics for the circuit connections between the external FET and this pin.
2	CTRL1	Digital output	The output of this pin is averaged with CTRL2 to control PWM duty cycle for the dc-dc controller. This output also controls the dc output for the detection circuitry.
3	VDD	Power	3.3 V power supply input.
4	CTRL2	Digital output	The output of this pin is averaged with CTRL1 to control PWM duty cycle for the dc-dc controller. This output also controls the dc output for the detection circuitry.
5	250KHZ	Digital output	This is a 250 kHz square wave (50% duty cycle) that is filtered into a triangular wave signal for the dc-dc controller. The 250 kHz output on this pin is gated off when it is desired to keep the switcher FET off.
6	DETA	Analog input	DETA is an analog input pin. During the detection process, the CTRL1 and CTRL2 pin duty cycle is varied to generate filtered dc voltages across a resistive bridge. The null indicator for this bridge is connected to pin DETA.
7	VSENSE	Analog input	VSENSE is an analog input used for sensing the PSE output voltage.

Table 10. Si3460 Pin Functionality (Continued)

Pin #	Pin Name	Pin Type	Pin Function
8	$\overline{\text{RST}}$	Digital input	Active low reset input. When low (to GND), places the Si3460 device into an inactive state. The dc-dc converter is disabled. When pulled high, the device begins the detection process sequence. The dc-dc begins to function after a valid R_{GOOD} signature is detected, indicating a valid PD has been detected.
9	ISENSE	Analog input	ISENSE is an analog input connected to a current sense resistor for output current sensing.
10	STATUS	Analog in/Digital out	At powerup, the voltage on this pin is sensed to configure the classification level, mid span timing mode, and the device's restart behavior when a fault condition is detected. Refer to "5.2. Operating Mode Configuration" on page 11 and "5.3.8. Status LED Function" on page 13 for more information. After reading the voltage present at this pin at powerup, the STATUS pin becomes a digital output used to control an external LED, which indicates when a detect, power good, or output fault condition has occurred. A logic low turns the LED on, and logic high turns the LED off.
11	GND	GND	Ground connection for the Si3460. This is NOT earth ground. Refer to the Si3460-EVB schematics for more information.

8. Ordering Guide

Ordering Part Number	Description	Package Information	Temperature Range (Ambient)
Si3460-XYY-GM	Single-port PSE controller for embedded applications; extended temperature range	11-pin QFN 3 x 3 mm RoHS, Pb-free	–40 to 85 °C
Si3460-EVB	Single-port PSE evaluation board and reference design	Evaluation board	N/A

Notes:
1. “X” denotes silicon revision. “YY” denotes firmware revision.
2. Add “R” to part number for tape and reel option (e.g. Si3460-X-GMR).
3. The ordering part number above is not the same as the device mark. The first line of the device mark is “3460”. See "9.3. Device Marking of Production Devices" on page 21 for more information.

9. Package Outline: 11-Pin QFN

Figure 5 illustrates the package details for the Si3460. Table 11 lists the values for the dimensions shown in the illustration. The Si3460 is packaged in an industry-standard, 3x3 mm, RoHS-compliant, Pb-free, 11-pin QFN package.

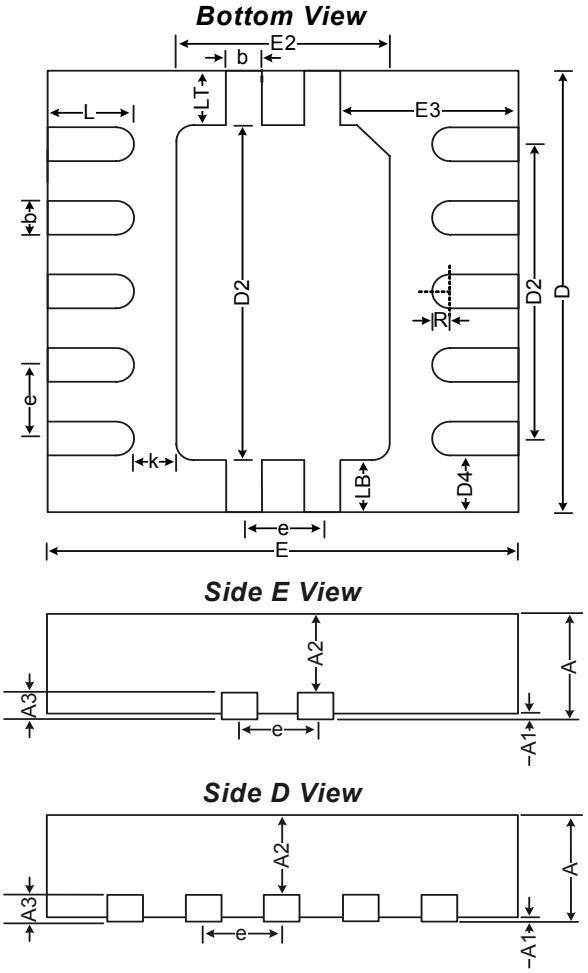


Figure 5. QFN-11 Package Drawing

Table 11. QFN-11 Package Dimensions

	MM		
	Min	**Typ**	**Max**
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	0	0.65	1.00
A3	—	0.25	—
b	0.18	0.23	0.30
D	—	3.00	—
D2	—	2.20	2.25
D3	—	2.00	—
D4	—	0.386	—
E	—	3.00	—
E2	—	1.36	—
E3	—	1.135	—
e	—	0.5	—
k	—	0.27	—
L	0.45	0.55	0.65
LB	—	0.36	—
LT	—	0.37	—
R	0.09	—	—

9.1. Solder Paste Mask

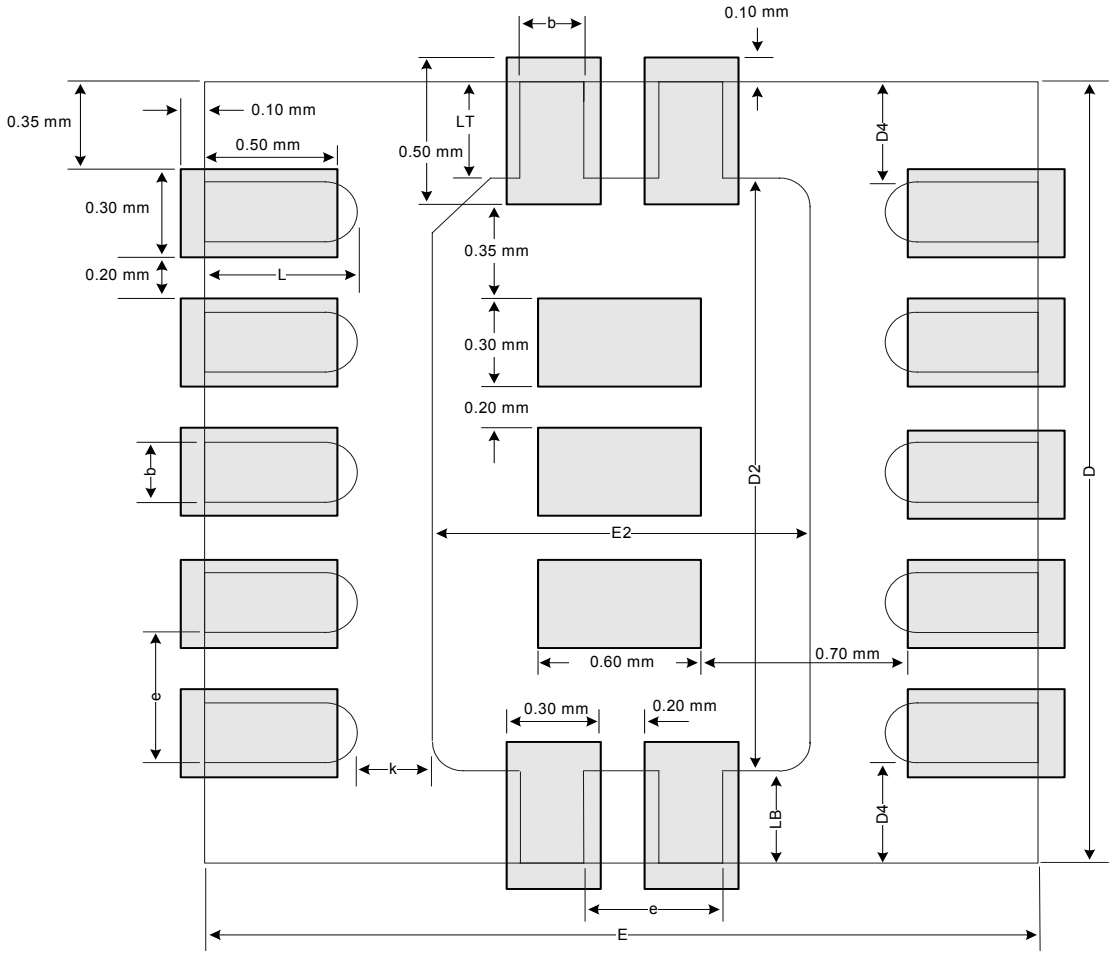


Figure 6. Solder Paste Mask

9.2. PCB Landing Pattern

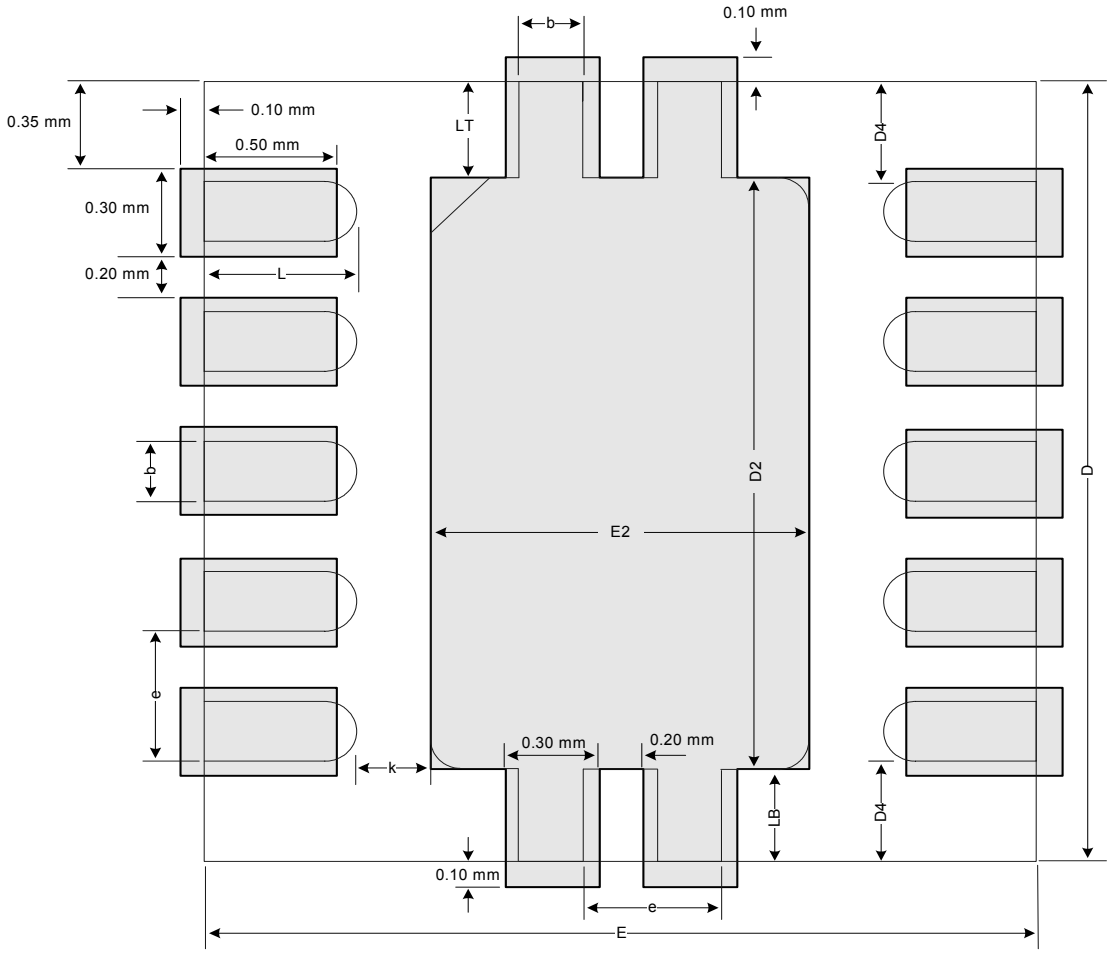


Figure 7. Typical QFN-11 Landing Diagram

9.3. Device Marking of Production Devices

Line 1 is the part number; line 2 is the lot code, and line 3 is the date code. The Lot ID Code on the top side of the device package can be used for decoding device revision information. On Si3460 devices, the silicon revision letter is the first letter of the Lot ID Code on the second line of the device mark. Figure 8 shows how to find the Lot ID Code on the top side of the device package for production devices.

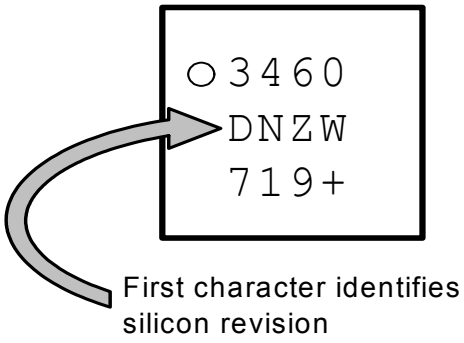


Figure 8. QFN 11 Device Marking Example

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