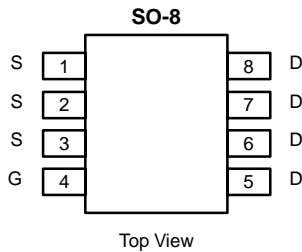




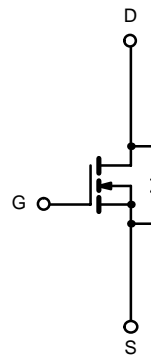
N-Channel 80-V (D-S) MOSFET

175°C Rated
Maximum Junction Temperature
TrenchFET®
Power MOSFETs

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
80	0.035 @ $V_{GS} = 10$ V	6.2
	0.040 @ $V_{GS} = 6.0$ V	5.8



Ordering Information: Si4480EY
Si4480EY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	80	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^{a, b}	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	40	A
Continuous Source Current (Diode Conduction) ^{a, b}	I_S	2.5	
Maximum Power Dissipation ^{a, b}	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	40	50	$^\circ\text{C/W}$
		Steady State	85	100	
Maximum Junction-to-Lead	R_{thJL}	20	24		

Notes

- a. Surface Mounted on FR4 Board, $t \leq 10$ sec.
- b. $t \leq 10$ sec.

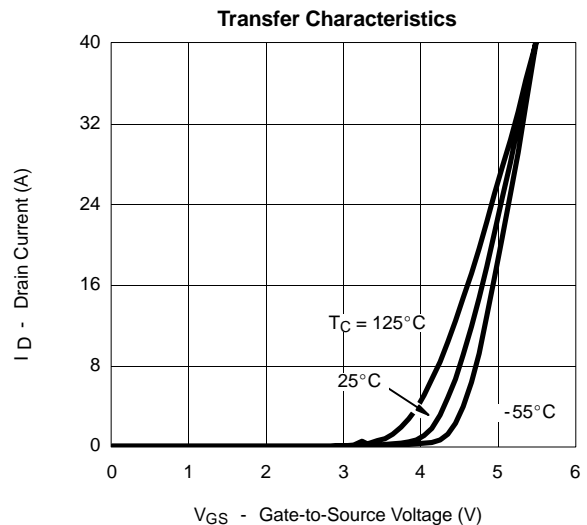
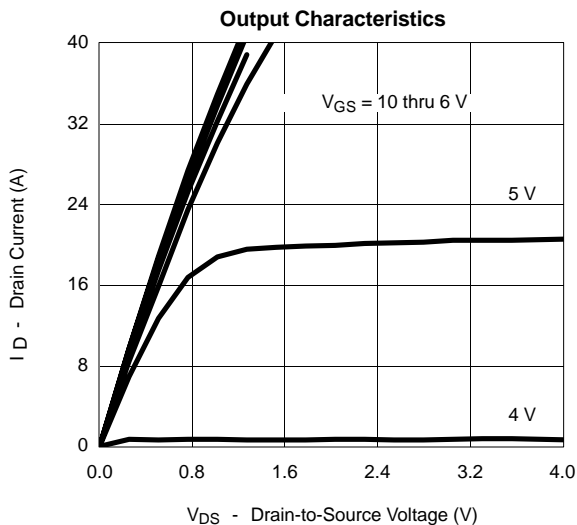


SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^b	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
		V _{DS} = 80 V, V _{GS} = 0 V, T _J = 55 °C			20	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 6.2 A		0.026	0.035	Ω
		V _{GS} = 6.0 V, I _D = 5.8 A		0.030	0.040	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 6.2 A		25		S
Diode Forward Voltage ^a	V _{SD}	I _S = 2.1 A, V _{GS} = 0 V			1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = 40 V, V _{GS} = 10 V, I _D = 6.2 A		30	50	nC
Gate-Source Charge	Q _{gs}			9		
Gate-Drain Charge	Q _{gd}			5.6		
Gate Resistance	R _g		1.5		4.0	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 40 V, R _L = 30 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω		12.5	25	ns
Rise Time	t _r			12.5	25	
Turn-Off Delay Time	t _{d(off)}			52	80	
Fall Time	t _f			22	40	
Source-Drain Reverse Recovery Time	t _{rr}		I _F = 2.1 A, di/dt = 100 A/μs		50	

Notes

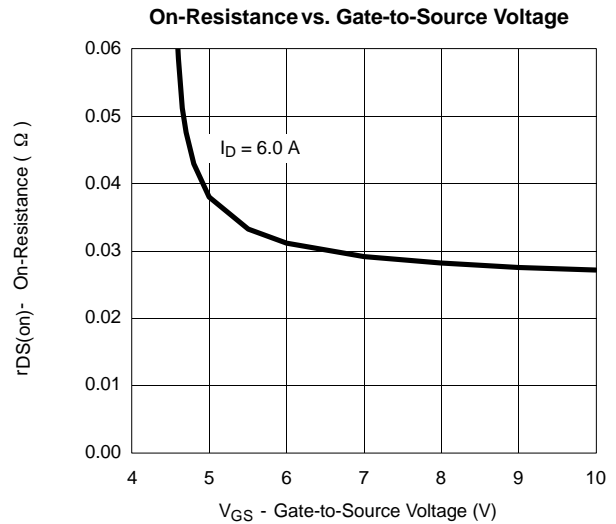
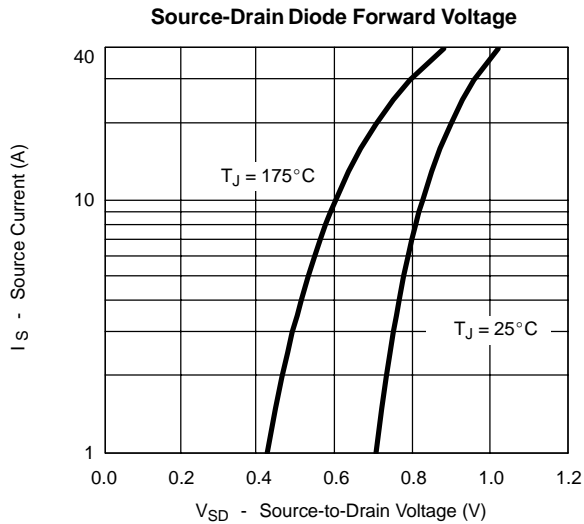
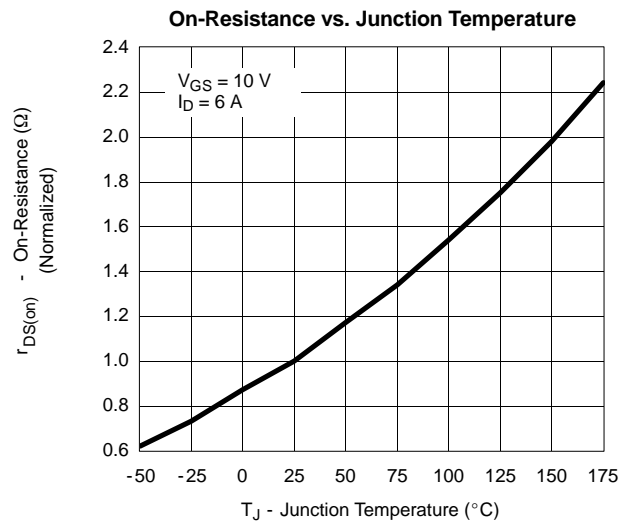
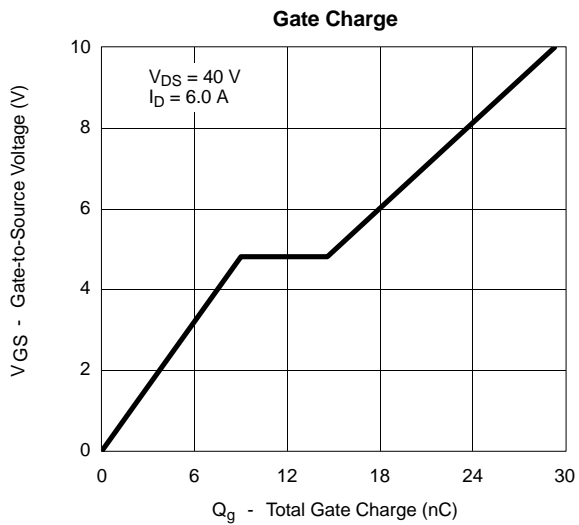
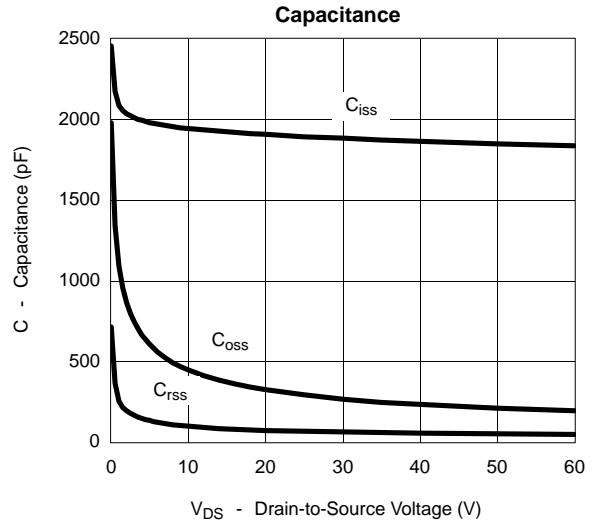
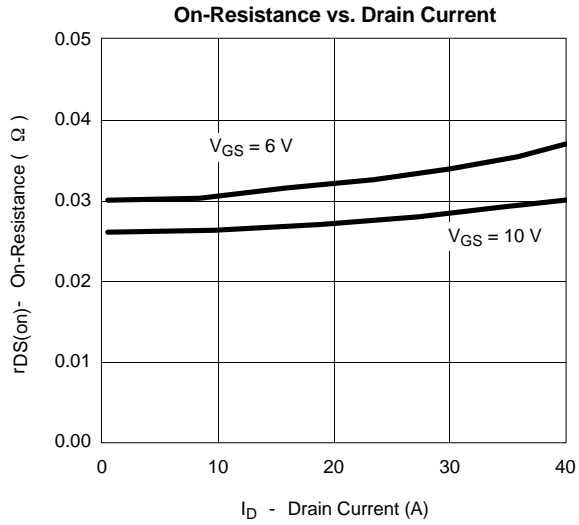
- a. For design aid only; not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

