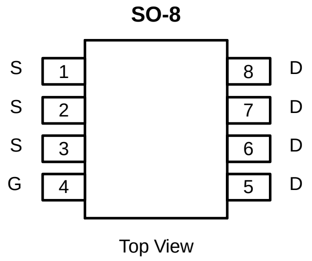
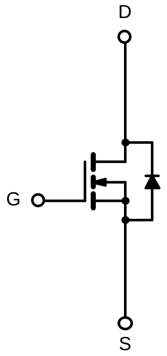
N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.034 @ V_{GS} = 10 V	6.9
	0.040 @ V_{GS} = 6.0 V	6.4

175°C Rated
Maximum Junction Temperature
High-Efficiency
PWM Optimized





N-Channel MOSFET

Ordering Information: Si4484EY
Si4484EY-T1 (with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	100		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 175°C)[a]	T_A = 25°C	I_D	6.9	4.8	A
	T_A = 85°C		5.4	3.7	
Pulsed Drain Current		I_{DM}	30		
Avalanche Current	L = 0.1 mH	I_{AR}	25		
Repetitive Avalanche Energy (Duty Cycle ≤1%)		E_{AR}	31		mJ
Continuous Source Current (Diode Conduction)[a]		I_S	3.1	1.5	A
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.8	1.8	W
	T_A = 85°C		2.3	1.1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	33	40	°C/W
	Steady State		70	85	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	17	21	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

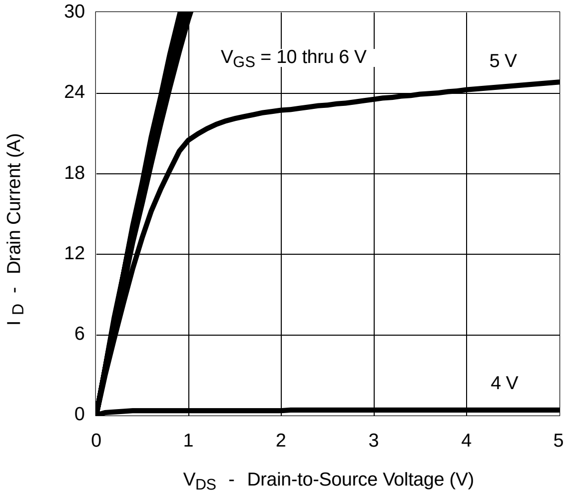
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ V$, $V_{GS} = \pm 20\ V$			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ V$, $V_{GS} = 0\ V$			1	µA
		$V_{DS} = 80\ V$, $V_{GS} = 0\ V$, $T_J = 85°C$			20	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \geq 5\ V$, $V_{GS} = 10\ V$	30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = 10\ V$, $I_D = 6.9\ A$		0.028	0.034	Ω
		$V_{GS} = 6.0\ V$, $I_D = 6.4\ A$		0.032	0.040	
Forward Transconductance[a]	g_{fs}	$V_{DS} = 15\ V$, $I_D = 6.9\ A$		25		S
Diode Forward Voltage[a]	V_{SD}	$I_S = 3.1\ A$, $V_{GS} = 0\ V$		0.8	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	$V_{DS} = 50\ V$, $V_{GS} = 10\ V$, $I_D = 6.9\ A$		24	30	nC
Gate-Source Charge	Q_{gs}			7.6		
Gate-Drain Charge	Q_{gd}			5.4		
Gate Resistance	R_g		0.5	1.25	2.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ V$, $R_L = 50\ \Omega$ $I_D \cong 1\ A$, $V_{GEN} = 10\ V$, $R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	t_f			20	40	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.1\ A$, di/dt = 100 A/µs		50	80	

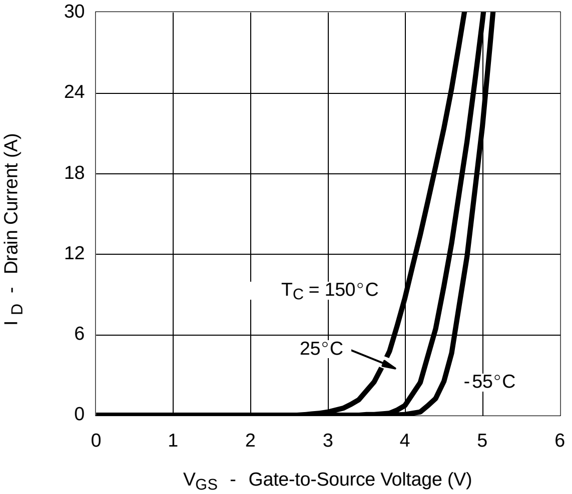
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

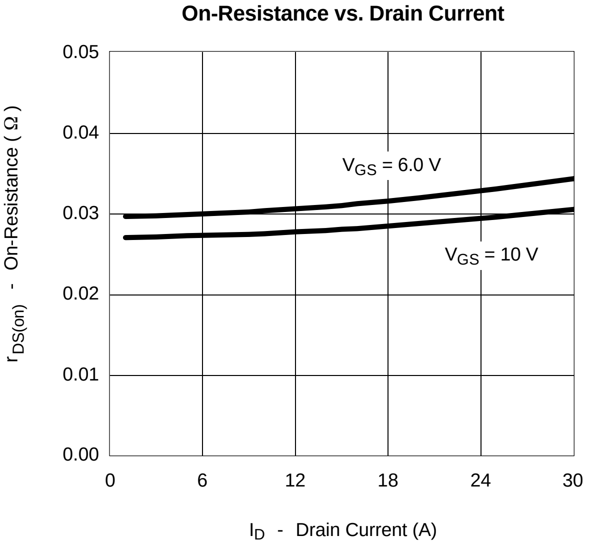
Output Characteristics

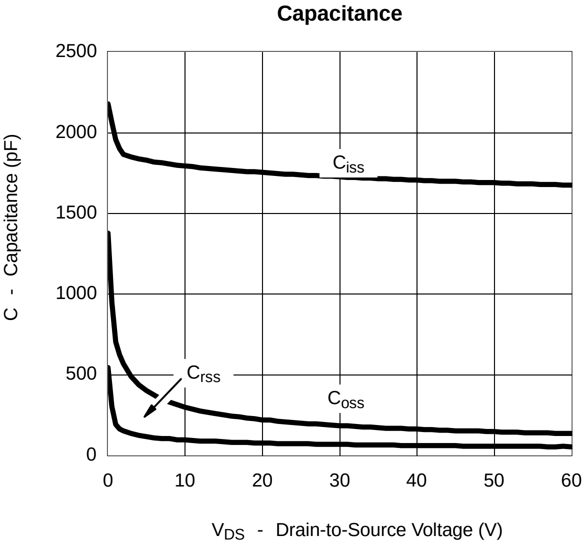


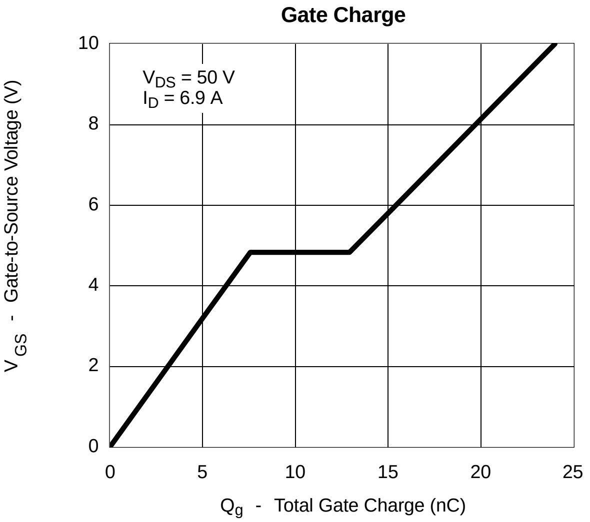
Transfer Characteristics

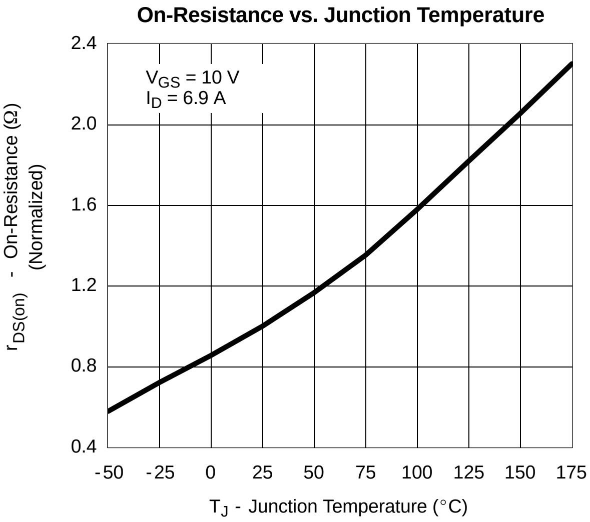


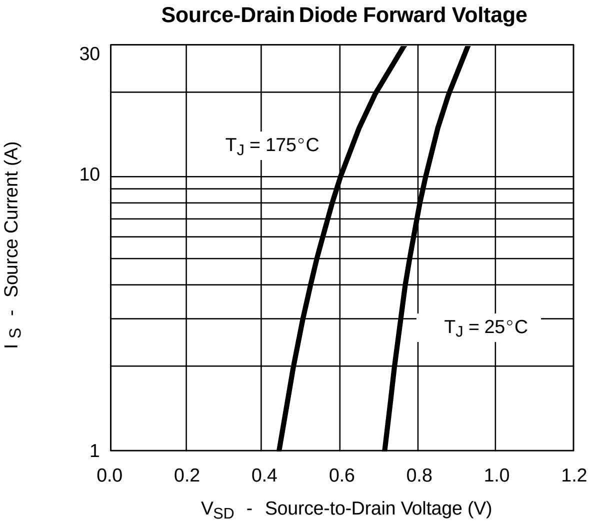
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

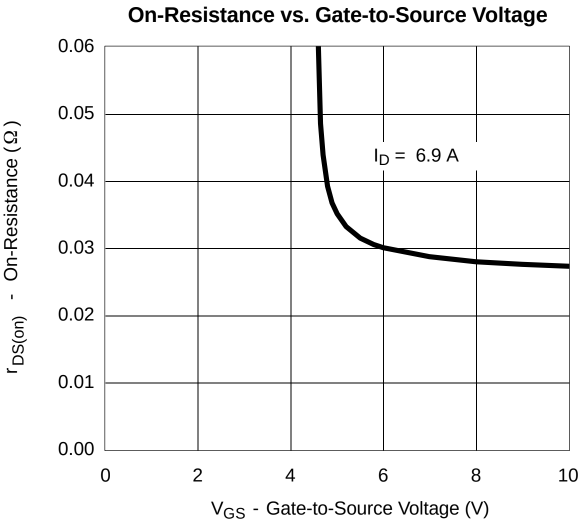






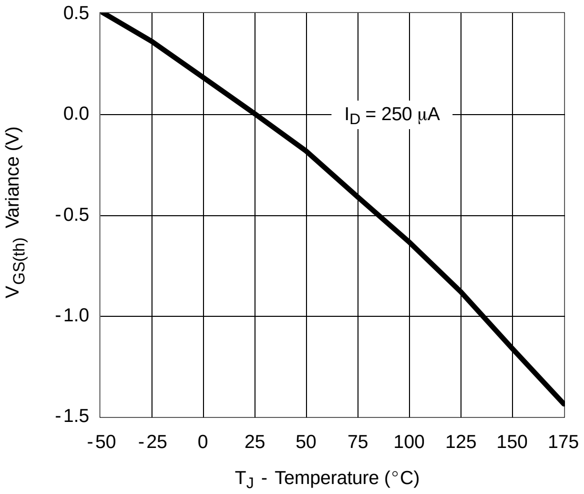




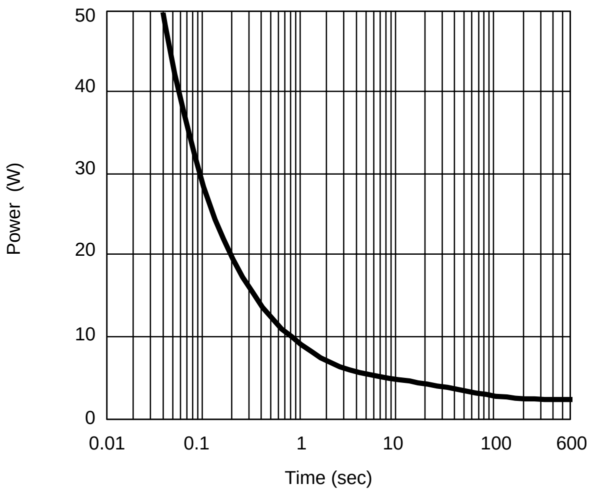


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

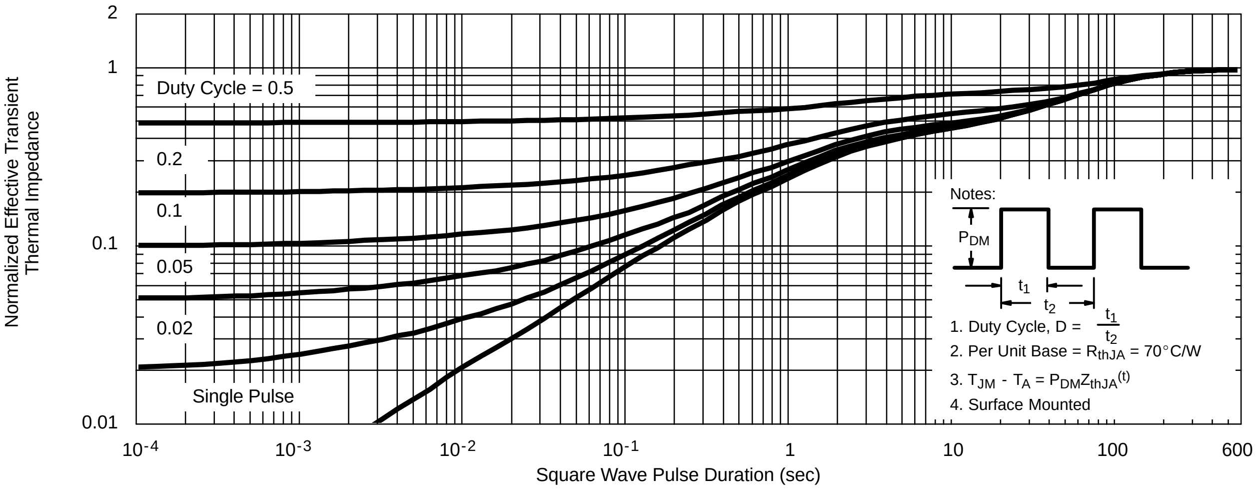
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Notes:

1. Duty Cycle, D = $\frac{t_1}{t_2}$
2. Per Unit Base = R_{thJA} = 70°C/W
3. $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$
4. Surface Mounted

Normalized Thermal Transient Impedance, Junction-to-Foot