

SI4884

TrenchMOS™ logic level FET

Rev. 02 — 12 April 2002

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

SI4884 in SOT96-1 (SO8).

1.2 Features

- Low on-state resistance
- Fast switching.

1.3 Applications

- DC to DC converters
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} = 30\text{ V}$
- $I_D = 12\text{ A}$
- $P_{tot} = 2.5\text{ W}$
- $R_{DS(on)} = 16.5\text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBK187</p>	<p>MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		

SOT96-1 (SO8)



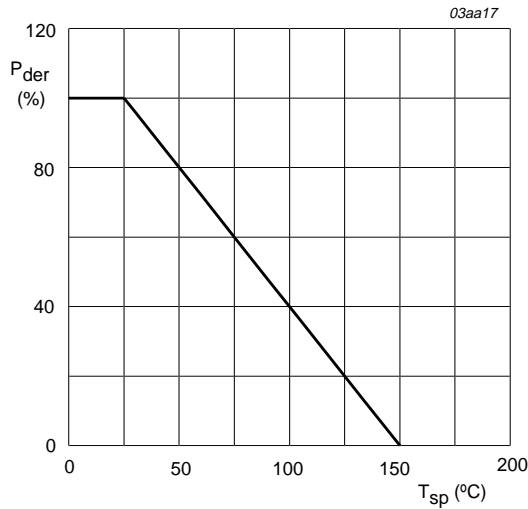
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3. Limiting values

Table 2: Limiting values

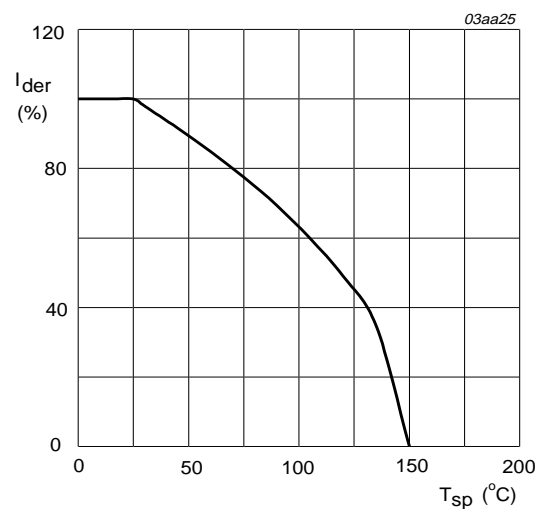
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$T_j = 25$ to 150 °C	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{sp} = 25$ °C; Figure 2 and 3	-	12	A
I_{DM}	peak drain current	$T_{sp} = 25$ °C; pulsed; Figure 3	-	45	A
P_{tot}	total power dissipation	$T_{sp} = 25$ °C; Figure 1	-	2.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current	$T_{sp} = 25$ °C	-	12	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

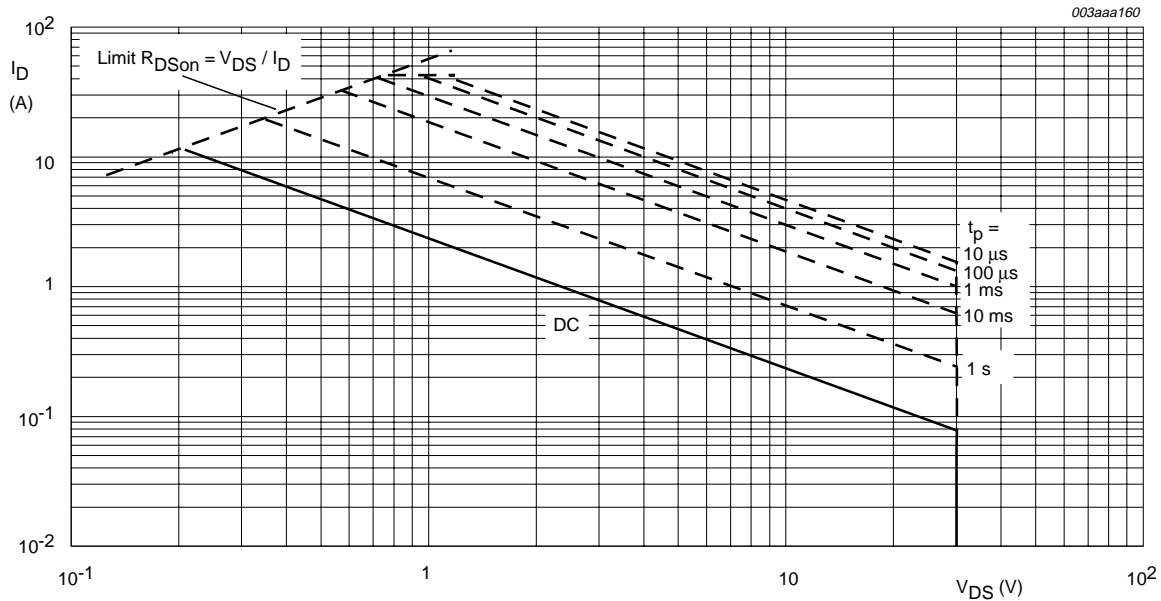
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$V_{GS} \geq 5\text{ V}$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; $t_p \leq 10$ s; minimum footprint; Figure 4	-	60	-	K/W

4.1 Transient thermal impedance

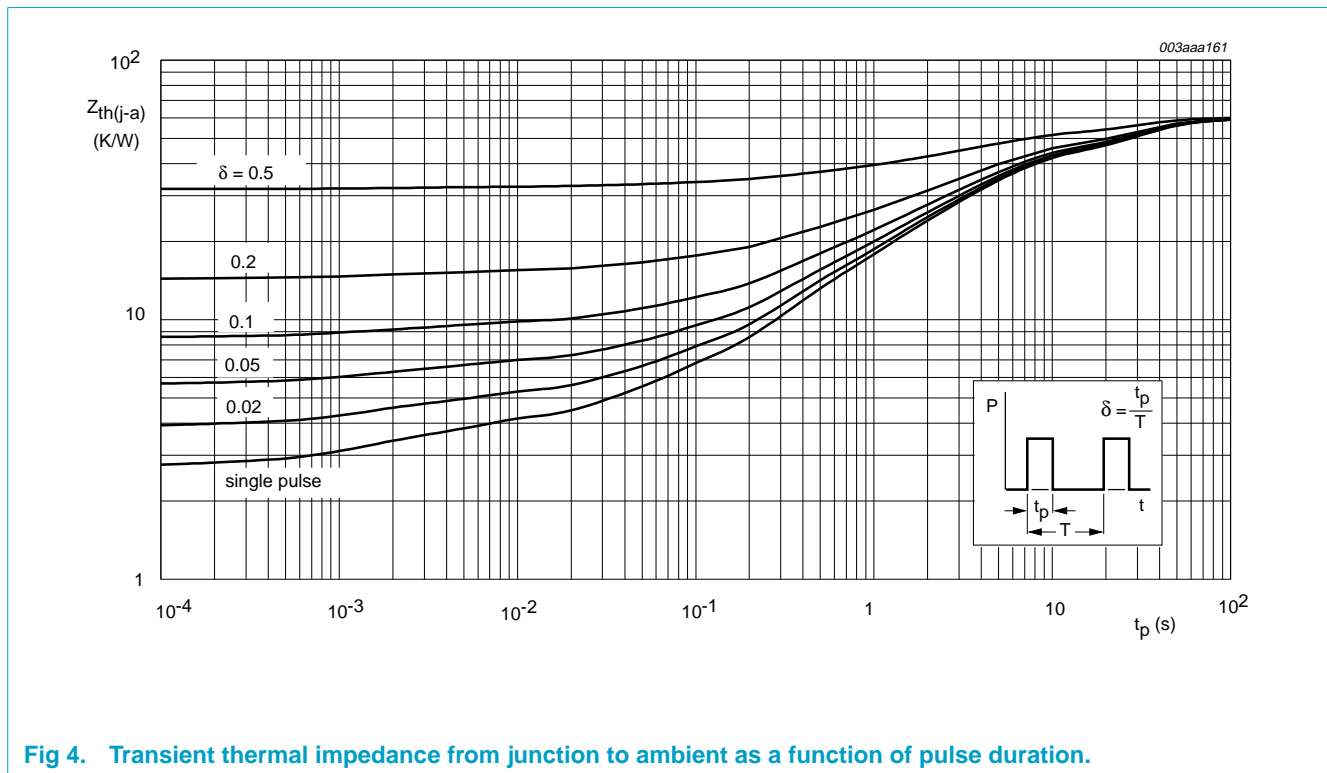
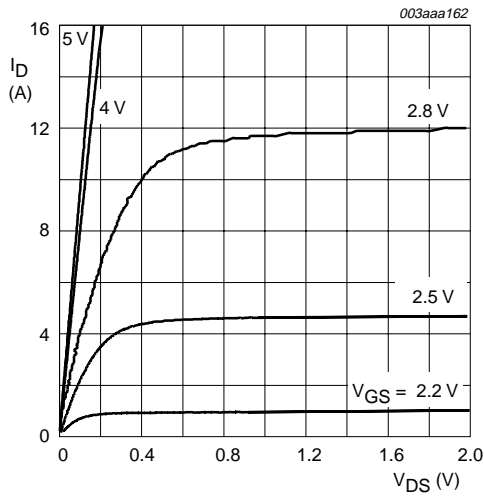


Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration.

5. Characteristics

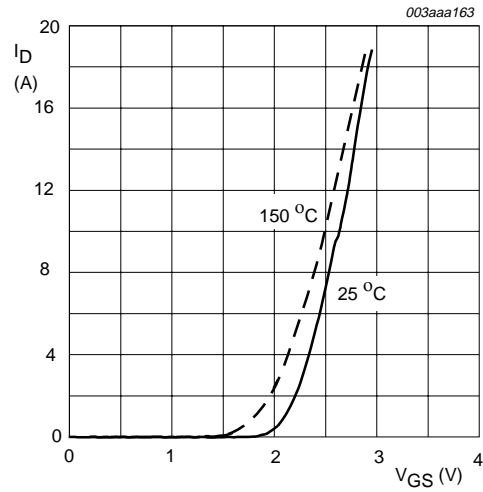
Table 4: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V	30	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; Figure 9	1	-	2	V
I _{DSS}	drain-source leakage current	V _{DS} = 24 V; V _{GS} = 0 V T _j = 25 °C	-	-	1	μA
			-	-	5	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±20 V; V _{DS} = 0 V	-		100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 10 A; Figure 7 and 8	-	11	16.5	mΩ
		V _{GS} = 10 V; I _D = 12 A;	-	8.9	10.5	mΩ
Dynamic characteristics						
g _{fs}	forward transconductance	V _{DS} = 15 V; I _D = 10 A;	-	34	-	S
Q _{g(tot)}	total gate charge	I _D = 15 A; V _{DD} = 16 V; V _{GS} = 5 V; Figure 13	-	17.6	-	nC
Q _{gs}	gate-source charge		-	4	-	nC
Q _{gd}	gate-drain (Miller) charge		-	4.4	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 16 V; f = 1 MHz; Figure 11	-	1335	-	pF
C _{oss}	output capacitance		-	391	-	pF
C _{rss}	reverse transfer capacitance		-	190	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 16 V; R _D = 10 Ω; V _{GS} = 10 V	-	10.6	-	ns
t _r	rise time		-	11.7	-	ns
t _{d(off)}	turn-off delay time		-	37	-	ns
t _f	fall time		-	19	-	ns
Source-drain (reverse) diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 1 A; V _{GS} = 0 V; Figure 12	-	0.7	1.0	V
t _{rr}	reverse recovery time	I _S = 2.3 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V	-	70	-	ns



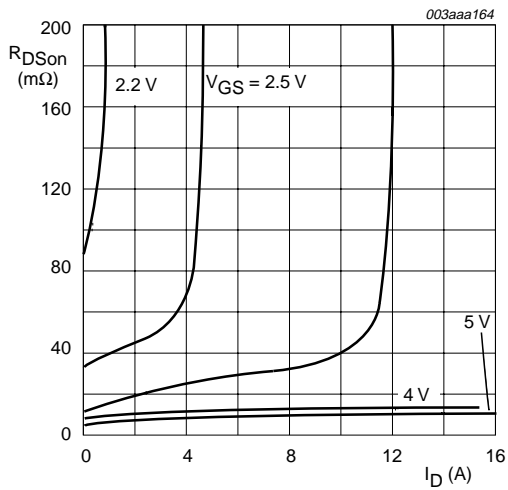
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



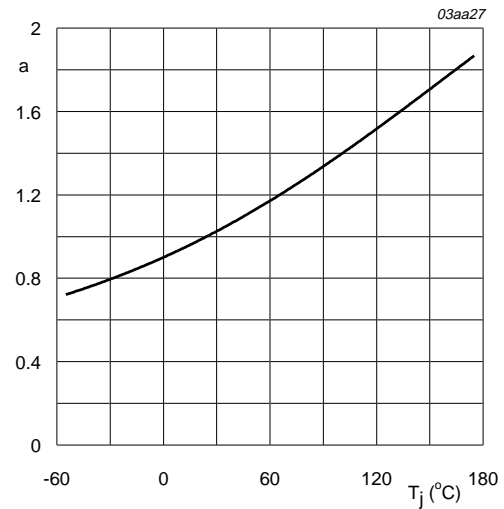
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



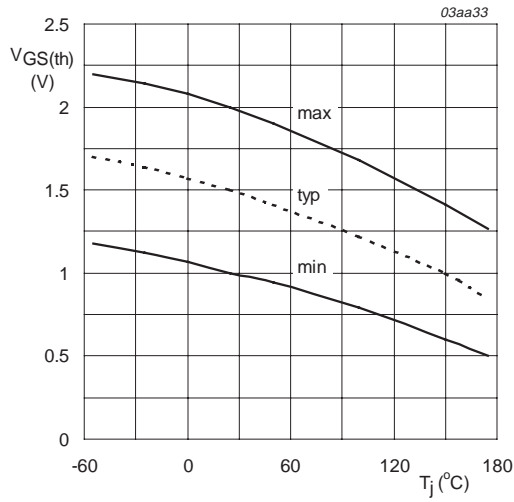
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



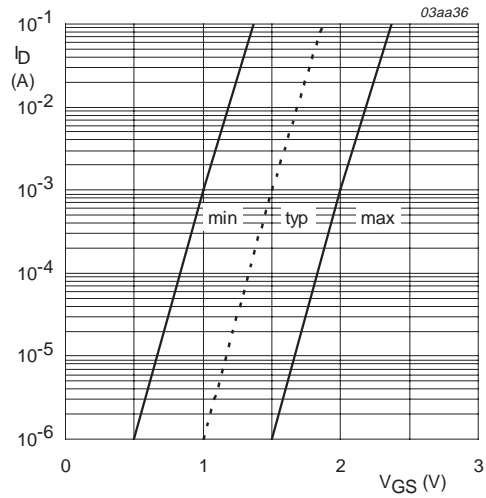
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.



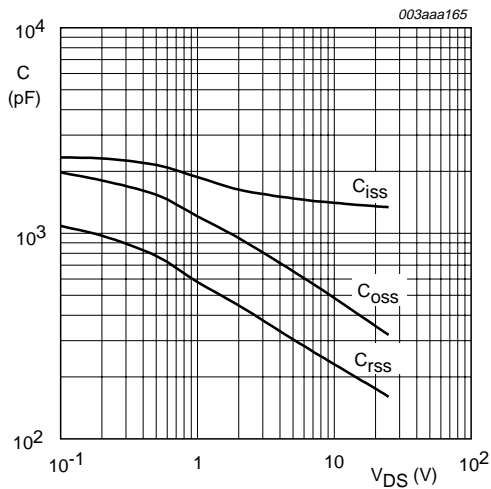
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



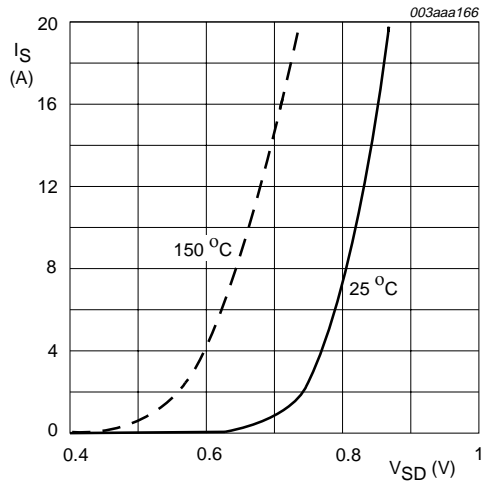
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



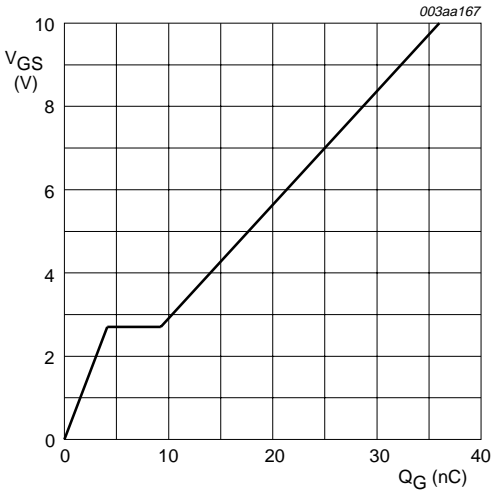
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25 \text{ }^\circ\text{C} \text{ and } 150 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 15\text{ A}; V_{DD} = 16\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

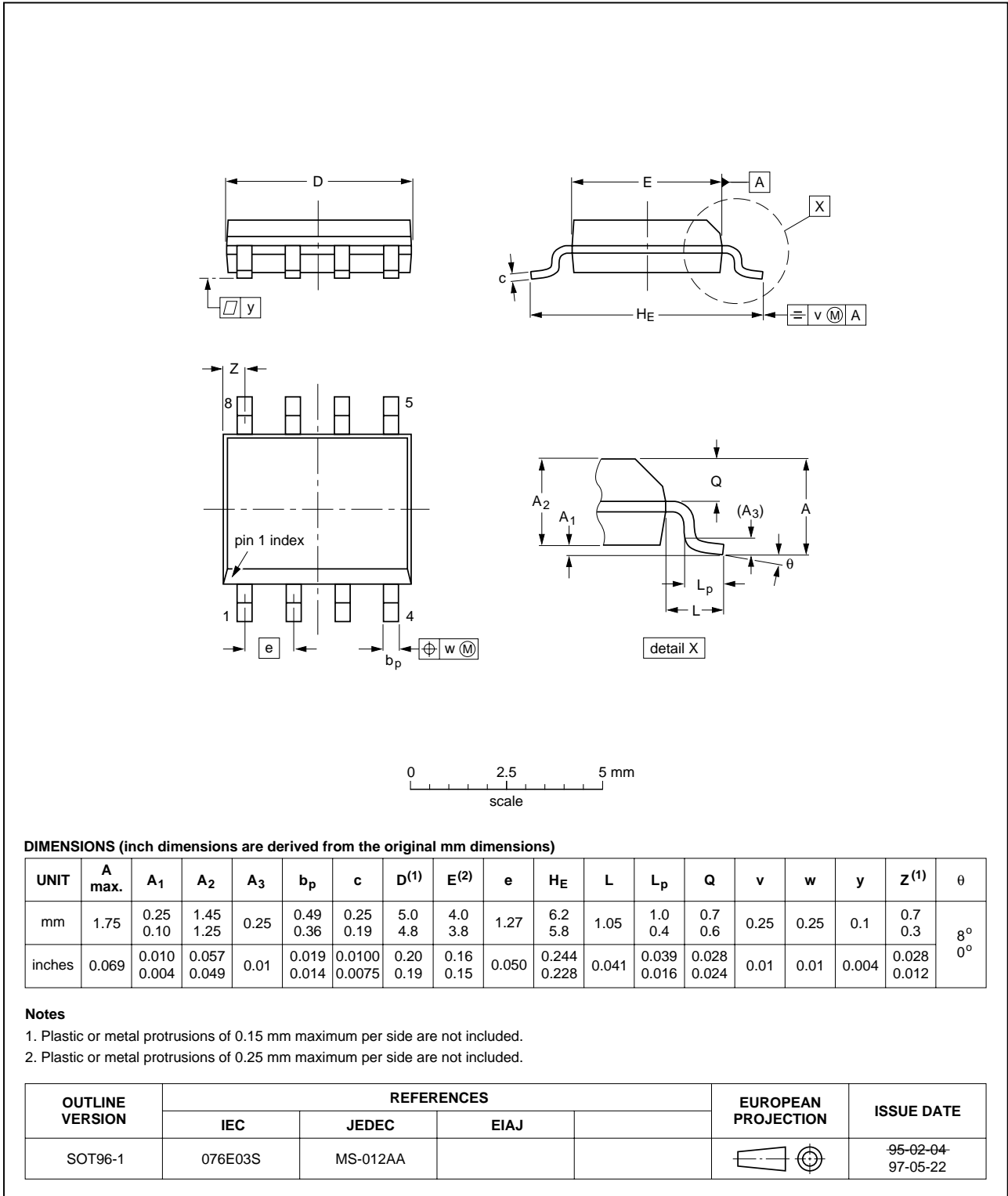


Fig 14. SOT96-1 (S08).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
02	20020412	-	Product data; version 02. Supersedes data of 15 March 2002. Figure 3 t_p label error corrected.
01	20020315	-	Product data; initial version

8. Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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