Dual P-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

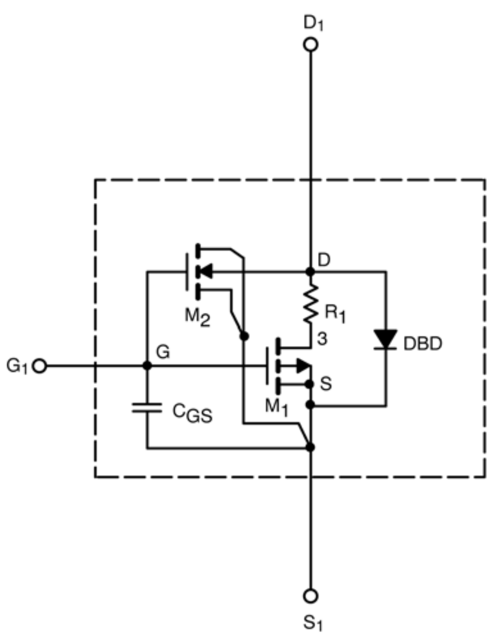
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

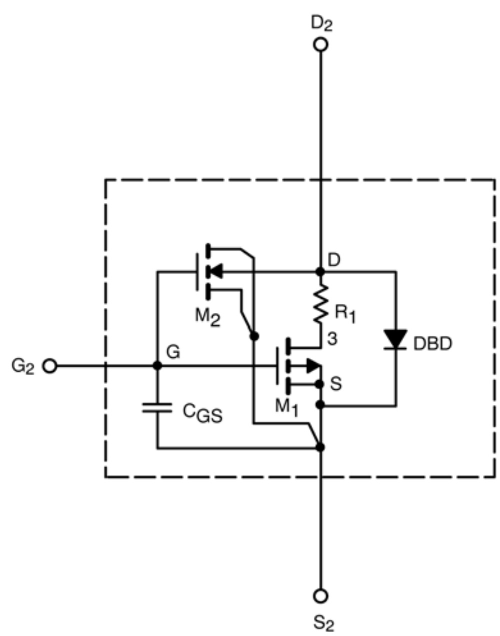
DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 5-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



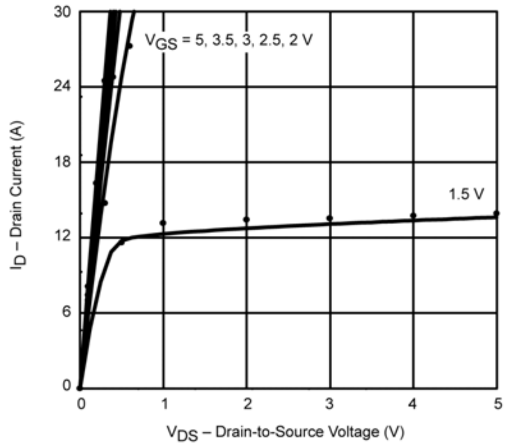


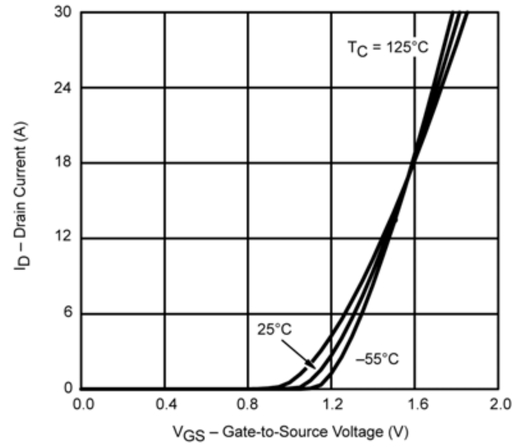
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

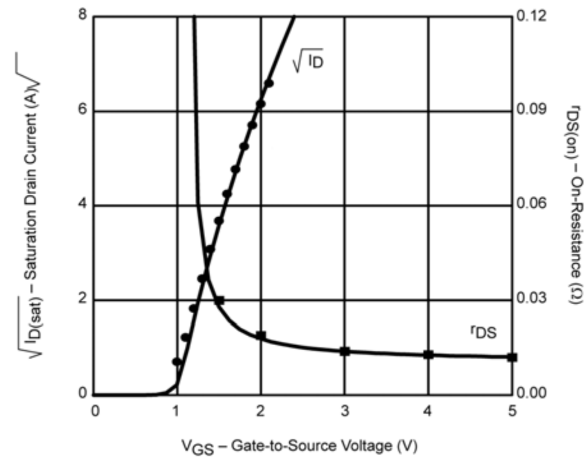
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -500\ \mu A$	0.75		V
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} = -5$ V, $V_{GS} = -4.5$ V	235		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	$V_{GS} = -4.5$ V, $I_D = -9.4$ A	0.0124	0.0125	Ω
		$V_{GS} = -2.5$ V, $I_D = -8.4$ A	0.015	0.0155	
		$V_{GS} = -1.8$ V, $I_D = -5$ A	0.019	0.020	
Forward Transconductance[a]	g_{fs}	$V_{DS} = -10$ V, $I_D = -9.4$ A	42	40	S
Diode Forward Voltage[a]	V_{SD}	$I_S = -1.7$ A, $V_{GS} = 0$ V	−0.80	−0.70	V
Dynamic[b]					
Total Gate Charge	Q_g	$V_{DS} = -6$ V, $V_{GS} = -4.5$ V, $I_D = -9.4$ A	47	43	nC
Gate-Source Charge	Q_{gs}		7.1	7.1	
Gate-Drain Charge	Q_{gd}		10.9	10.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6$ V, $R_L = 6\ \Omega$ $I_D \cong -1$ A, $V_{GEN} = -4.5$ V, $R_G = 6\ \Omega$	36	32	ns
Rise Time	t_r		35	42	
Turn-Off Delay Time	$t_{d(off)}$		166	350	
Fall Time	t_f		43	160	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7$ A, di/dt = 100 A/µs	135	127	

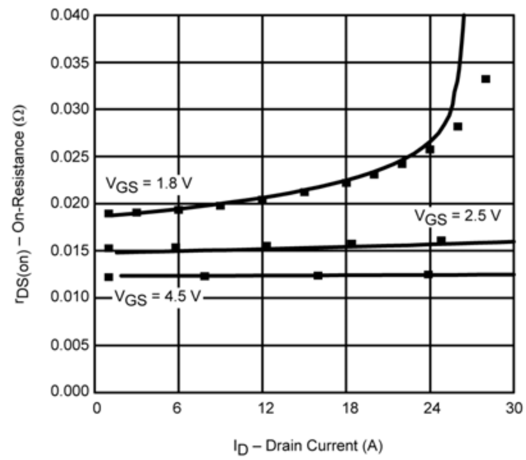
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

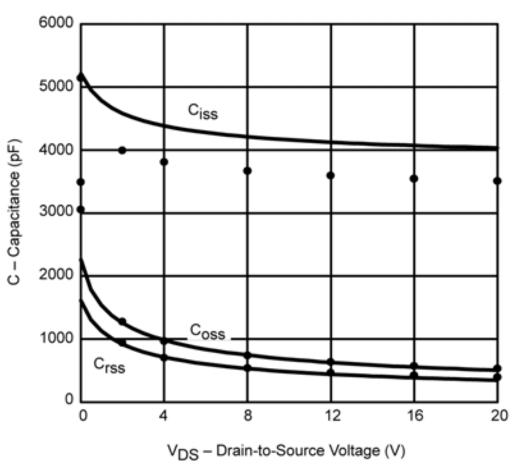
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

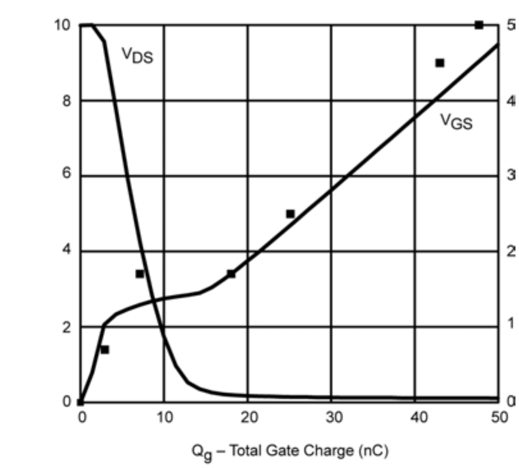












Note: Dots and squares represent measured data.