

Asymmetrical Dual P-Channel 30-V/20-V (D-S) MOSFETs

PRODUCT SUMMARY			
	V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
Channel-1	- 30	0.054 at V _{GS} = - 10 V	- 5.0
		0.100 at V _{GS} = - 4.5 V	- 3.7
Channel-2	- 20	0.027 at V _{GS} = - 4.5 V	- 7.0
		0.035 at V _{GS} = - 2.5 V	- 6.2
		0.048 at V _{GS} = - 1.8 V	- 5.2

FEATURES

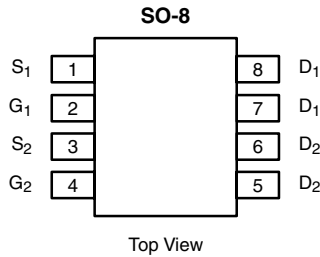
- TrenchFET® Power MOSFETs
- Low Gate Drive (2.5 V) Capability For Channel 2



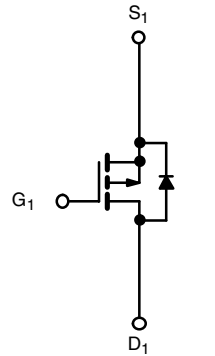
RoHS
COMPLIANT

APPLICATIONS

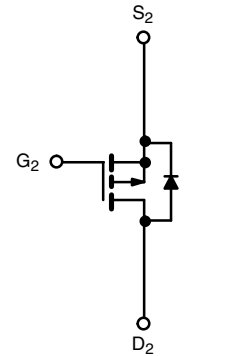
- Game Station
- Load Switch



Ordering Information: Si4955DY-T1-E3 (Lead (Pb)-free)



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		10 sec	Steady State	10 sec	Steady State		
Drain-Source Voltage	V _{DS}	- 30		- 20		V	
Gate-Source Voltage	V _{GS}	± 20		± 8			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	- 5.0	- 3.8	- 7.0	- 5.3	A
		T _A = 70 °C	- 4.0	- 3.0	- 5.6	- 4.2	
Pulsed Drain Current	I _{DM}	- 20				A	
Continuous Source Current (Diode Conduction) ^a	I _S	- 1.7	- 0.9	- 1.7	- 0.9		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.0	1.1	2	1.1	W
		T _A = 70 °C	1.3	0.7	1.3	0.7	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150				°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ	Max	Typ	Max		
Maximum Junction-to-Ambient ^a	R _{thJA}	t ≤ 10 sec	55	62.5	58	62.5	°C/W
		Steady State	90	110	91	110	
Maximum Junction-to-Foot (Drain)	R _{thJF}	33	40	34	40		

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	Ch-1	-1.0		-3	V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	Ch-2	-0.4		-1	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	Ch-1			± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$	Ch-2			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			-1	μA
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	Ch-2			-1	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$	Ch-1			-5	
		$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$	Ch-2			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5\text{ V}, V_{GS} = -10\text{ V}$	Ch-1	-20			A
		$V_{DS} \leq -5\text{ V}, V_{GS} = -10\text{ V}$	Ch-2	-20			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\text{ V}, I_D = -5.0\text{ A}$	Ch-1		0.044	0.054	Ω
		$V_{GS} = -4.5\text{ V}, I_D = -7.0\text{ A}$	Ch-2		0.022	0.027	
		$V_{GS} = -4.5\text{ V}, I_D = -3.7\text{ A}$	Ch-1		0.082	0.100	
		$V_{GS} = -2.5\text{ V}, I_D = -6.2\text{ A}$	Ch-2		0.029	0.035	
		$V_{GS} = -1.8\text{ V}, I_D = -3\text{ A}$	Ch-2		0.039	0.048	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\text{ V}, I_D = -5.0\text{ A}$	Ch-1		10		S
		$V_{DS} = -15\text{ V}, I_D = -3\text{ A}$	Ch-2		25		
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.7\text{ A}, V_{GS} = 0\text{ V}$	Ch-1		-0.80	-1.2	V
		$I_S = -1.7\text{ A}, V_{GS} = 0\text{ V}$	Ch-2		-0.80	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	Channel-1 $V_{DS} = -15\text{ V}, V_{GS} = -10\text{ V}, I_D = -5.0\text{ A}$	Ch-1		12.5	19	nC
			Ch-2		21	25	
Gate-Source Charge	Q_{gs}	Channel-2 $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -7\text{ A}$	Ch-1		2.1		
			Ch-2		2.6		
Gate-Drain Charge	Q_{gd}	Channel-2 $V_{DS} = -10\text{ V}, V_{GS} = -4.5\text{ V}, I_D = -7\text{ A}$	Ch-1		3.5		
			Ch-2		6.0		
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = -15\text{ V}, R_L = -15\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -10\text{ V}, R_G = 6\text{ }\Omega$	Ch-1		7	15	ns
			Ch-2		20	30	
Rise Time	t_r	Channel-2 $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$	Ch-1		10	15	
			Ch-2		40	60	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$	Ch-1		30	45	
			Ch-2		125	190	
Fall Time	t_f	Channel-2 $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -4.5\text{ V}, R_G = 6\text{ }\Omega$	Ch-1		22	35	
			Ch-2		85	130	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Ch-1		25	60	
		$I_F = -1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$	Ch-2		64	90	

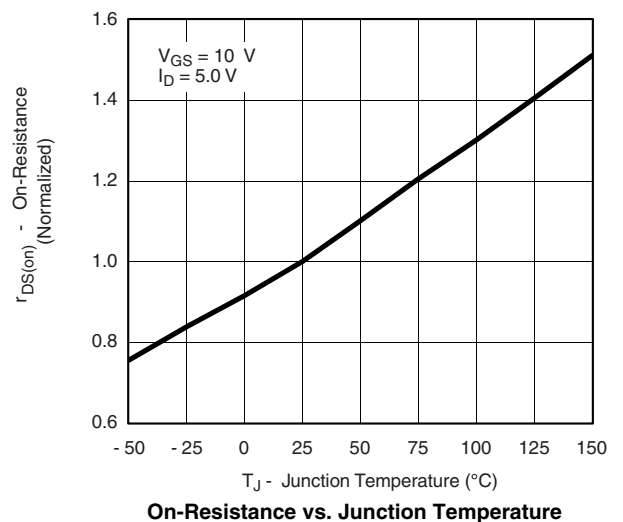
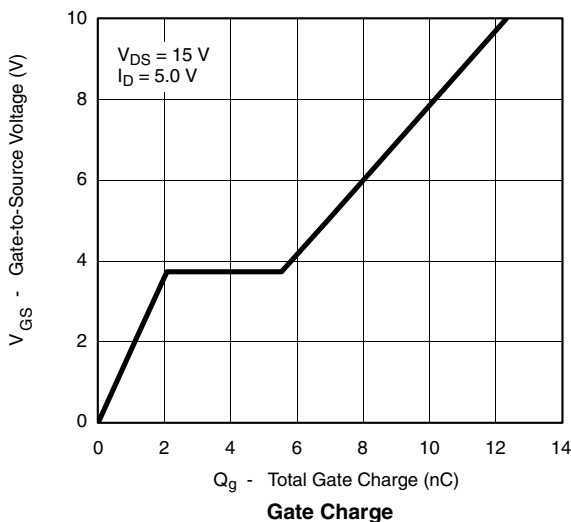
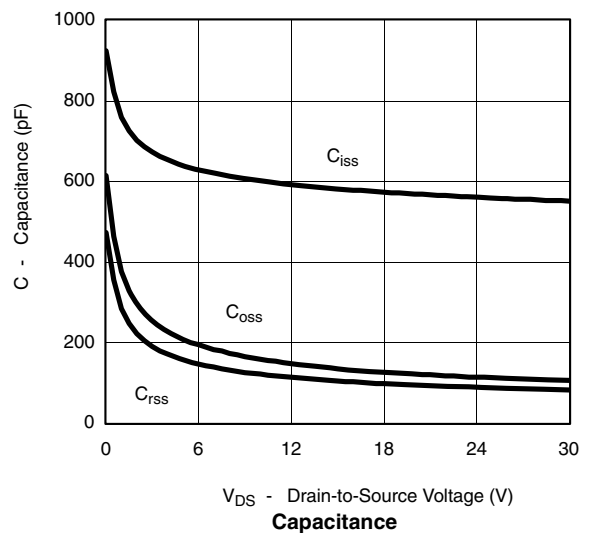
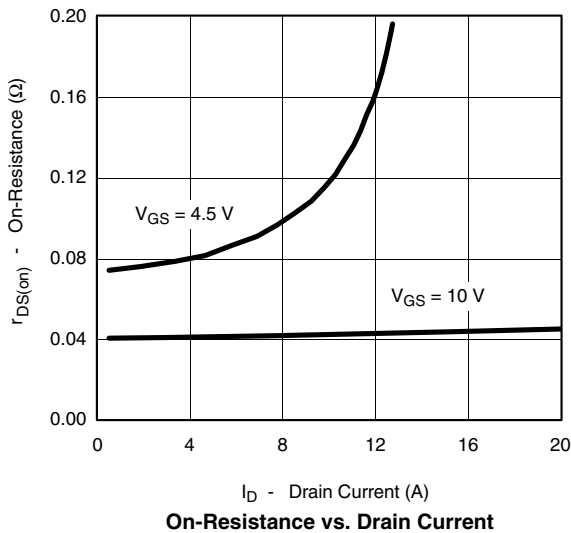
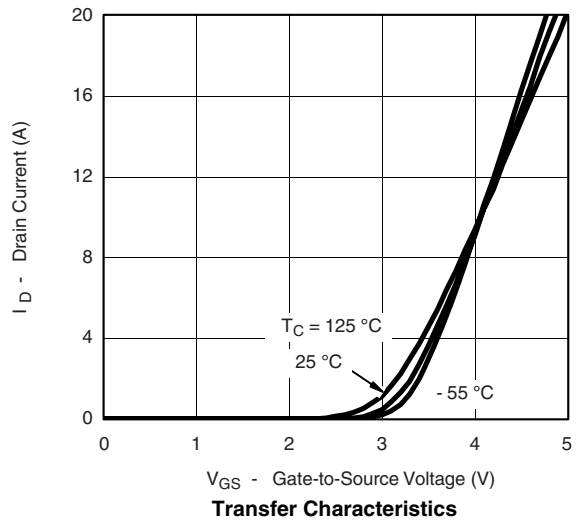
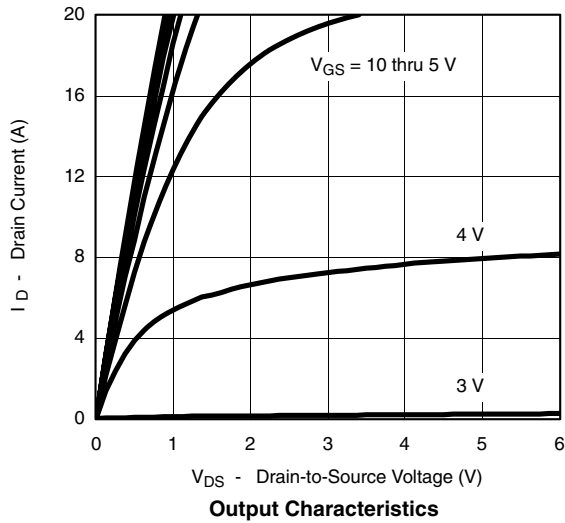
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

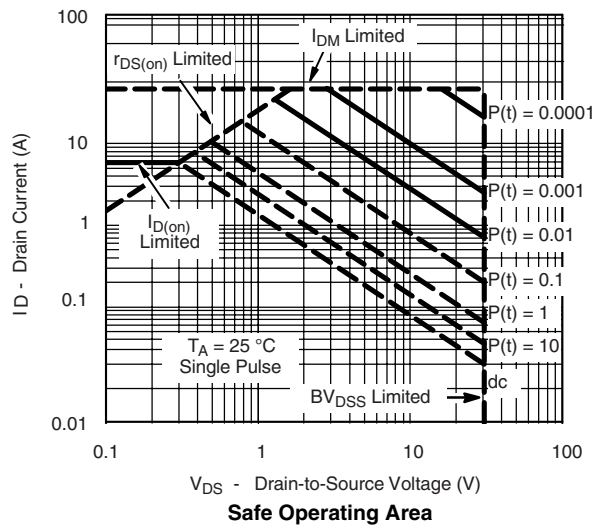
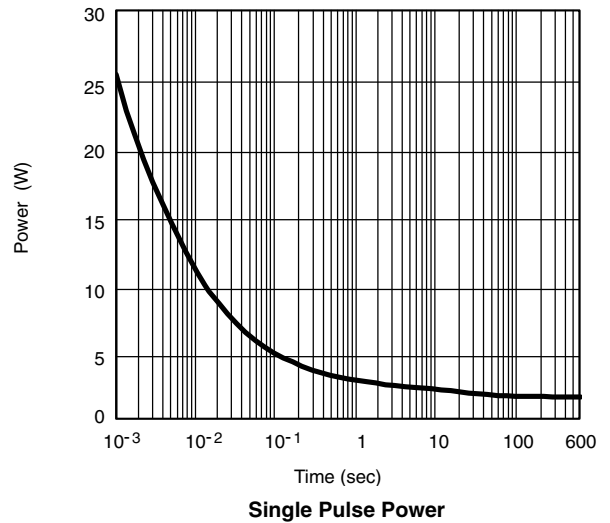
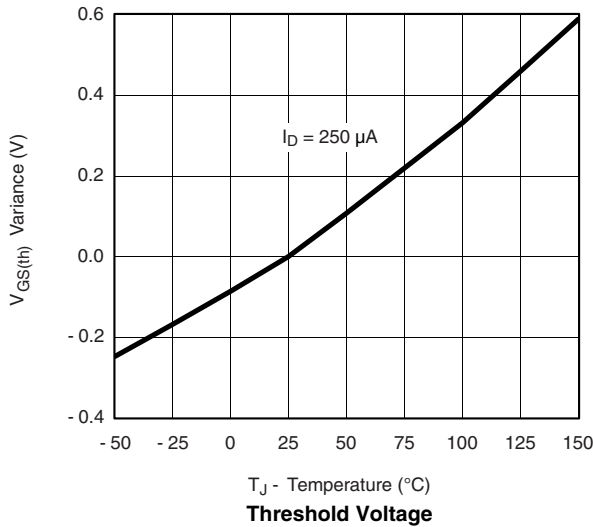
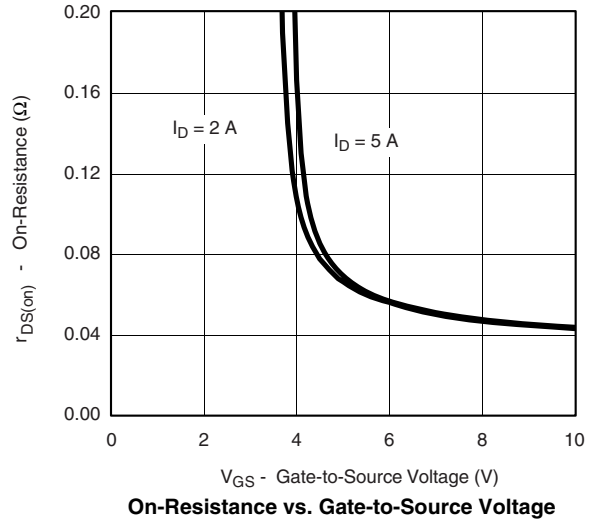
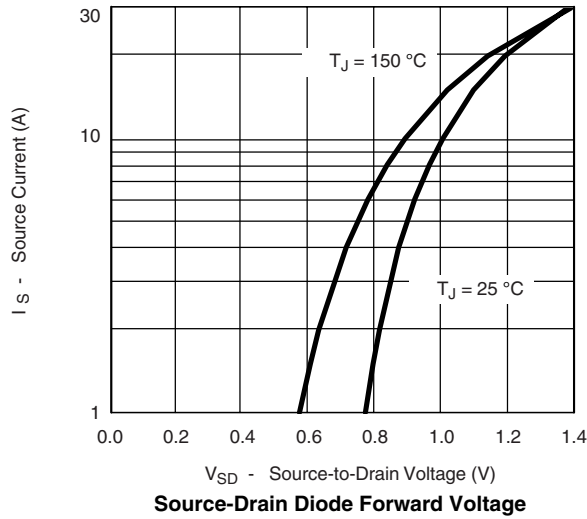
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

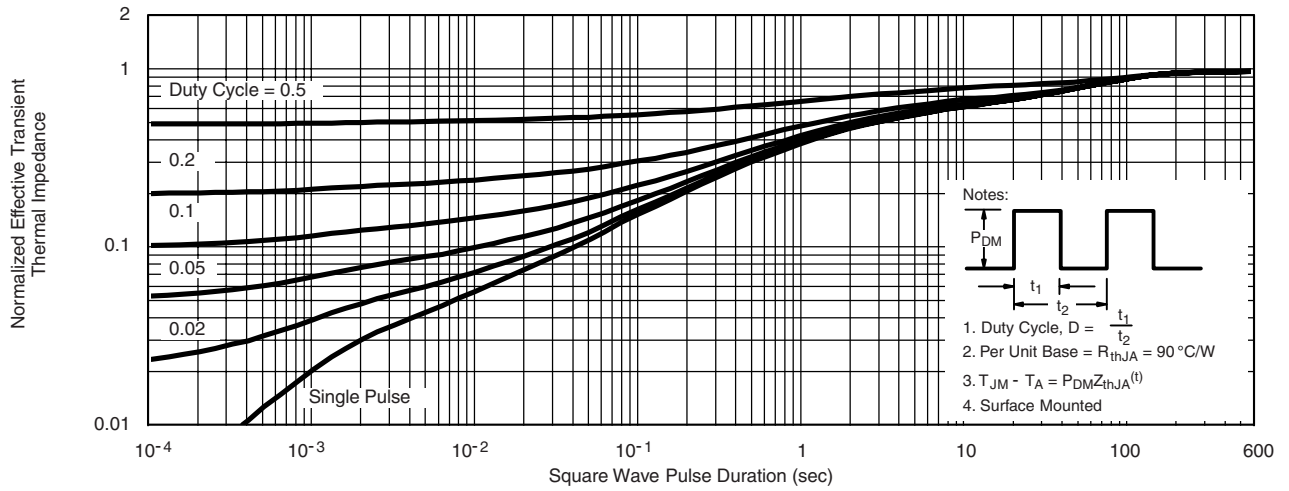
CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C unless noted



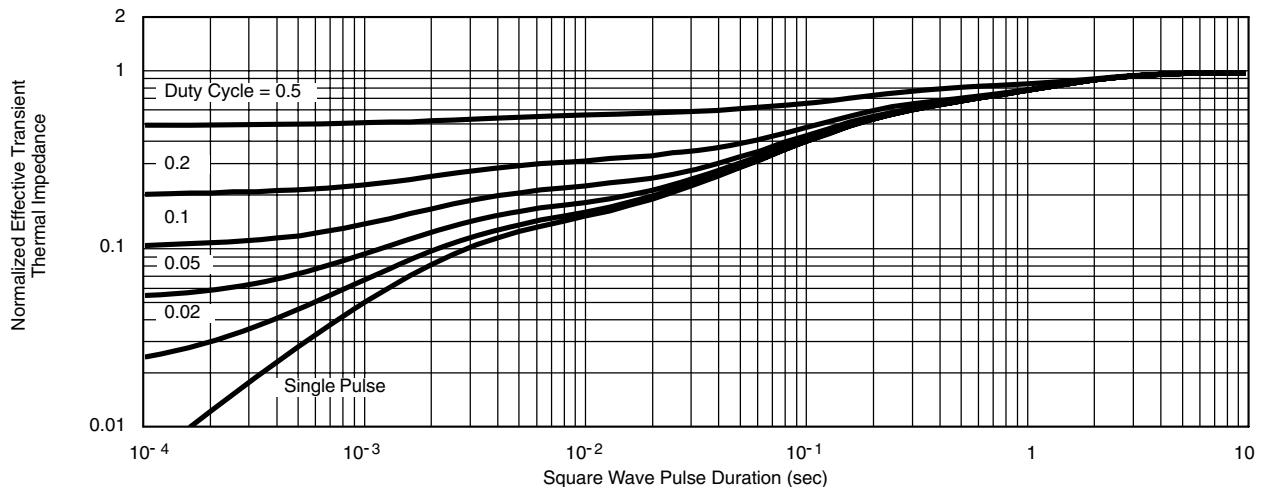
CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C unless noted



CHANNEL 1 TYPICAL CHARACTERISTICS 25 °C unless noted

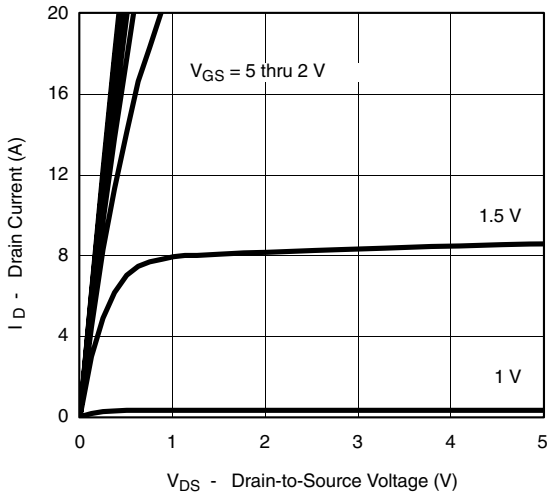


Normalized Thermal Transient Impedance, Junction-to-Ambient

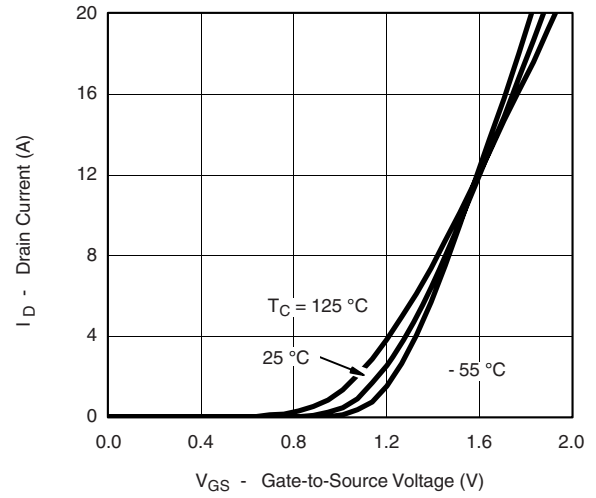


Normalized Thermal Transient Impedance, Junction-to-Foot

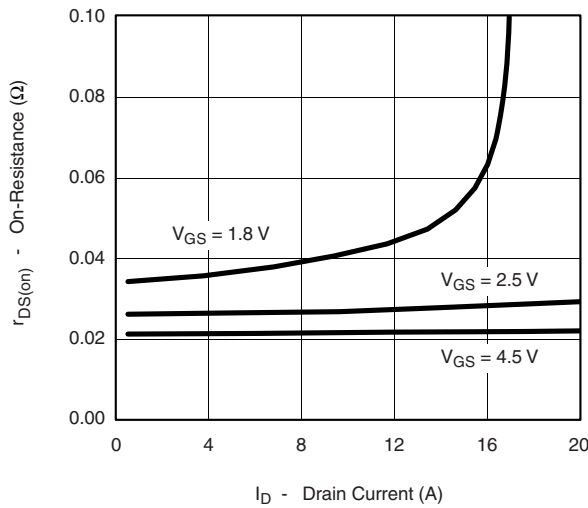
CHANNEL 2 TYPICAL CHARACTERISTICS 25 °C unless noted



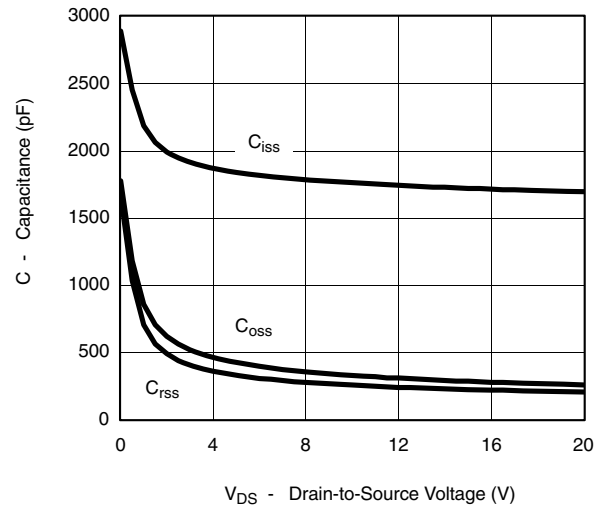
Output Characteristics



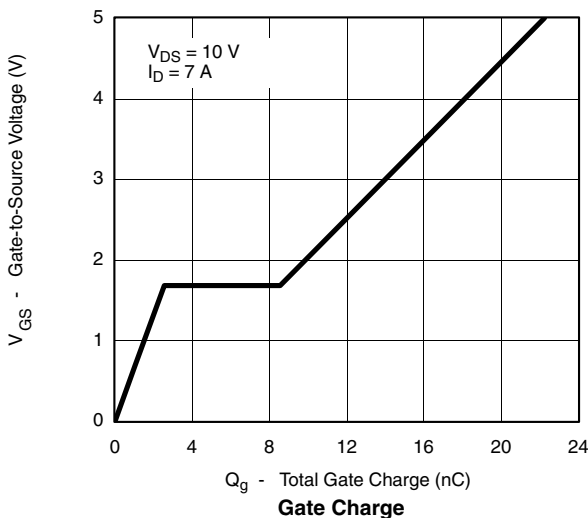
Transfer Characteristics



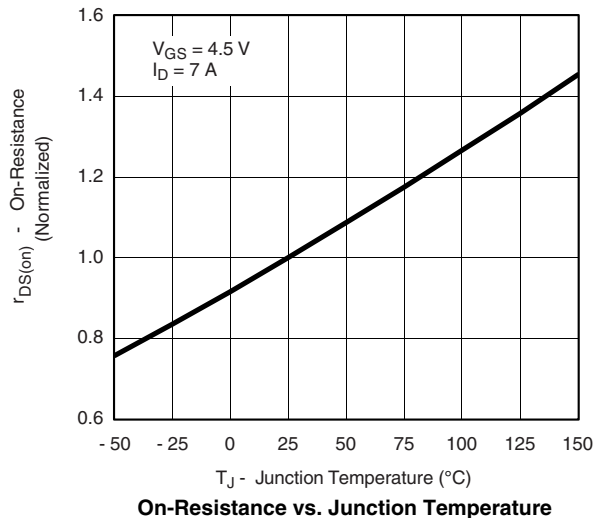
On-Resistance vs. Drain Current



Capacitance

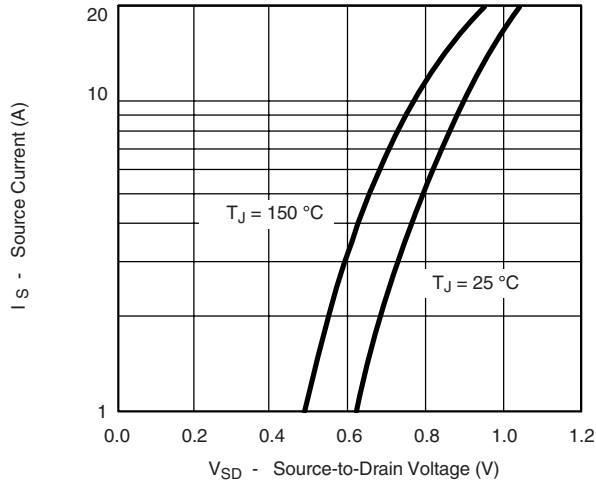


Gate Charge

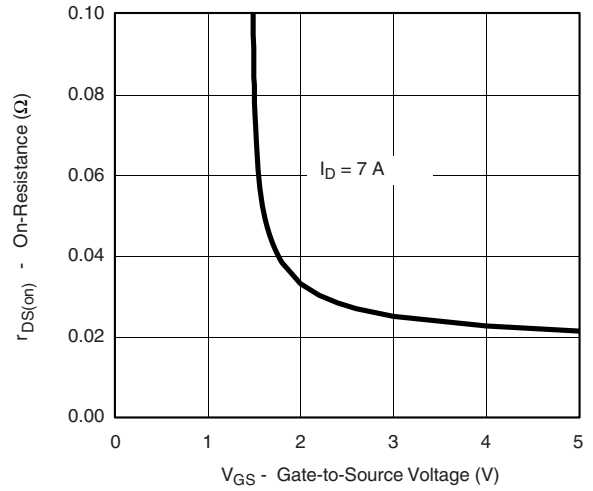


On-Resistance vs. Junction Temperature

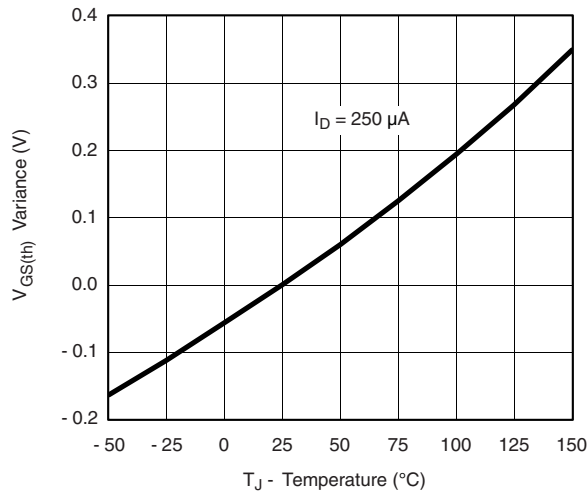
CHANNEL 2 TYPICAL CHARACTERISTICS 25 °C unless noted



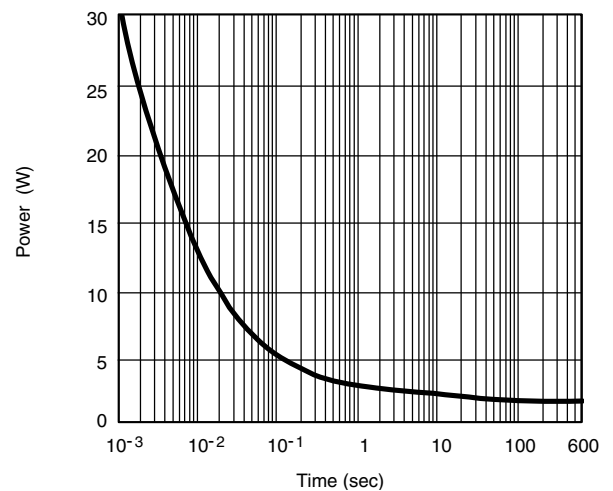
Source-Drain Diode Forward Voltage



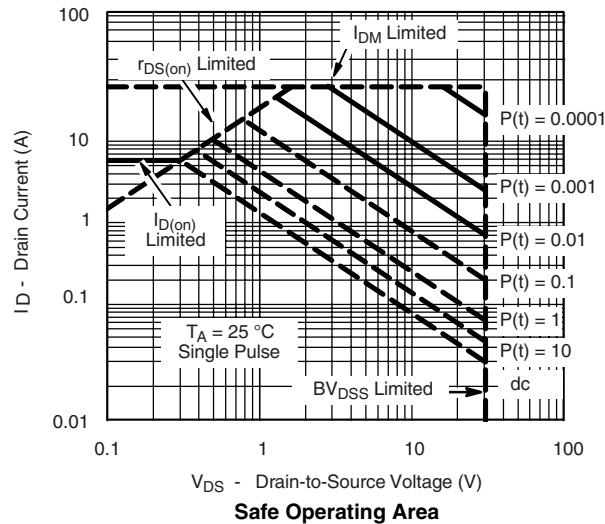
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



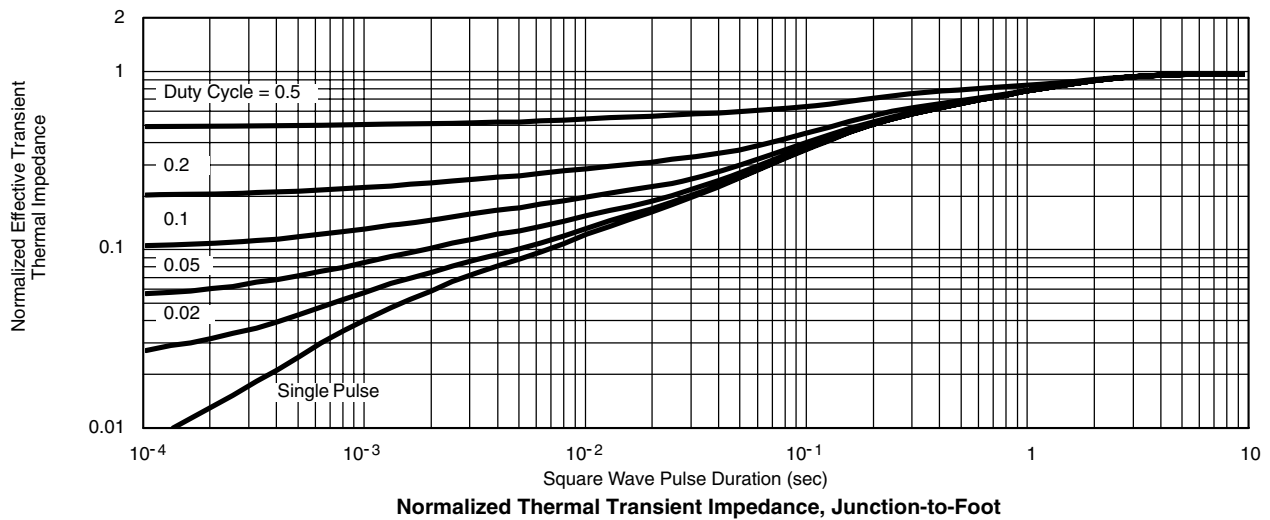
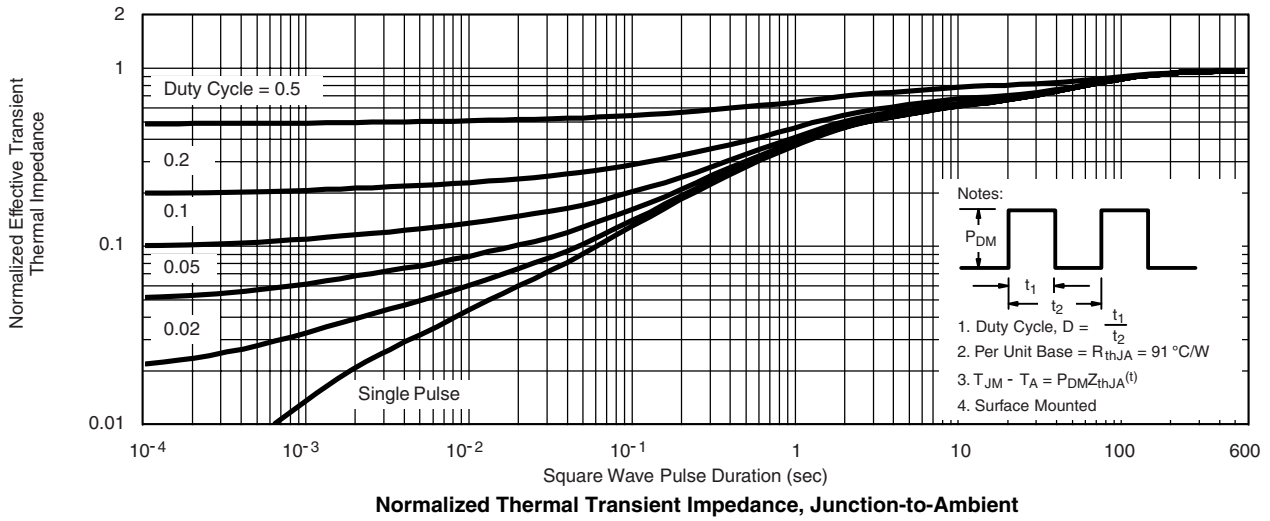
Single Pulse Power



Safe Operating Area



CHANNEL 2 TYPICAL CHARACTERISTICS 25 °C unless noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72241>.



Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.