

Dual N-Channel 100-V (D-S) MOSFET

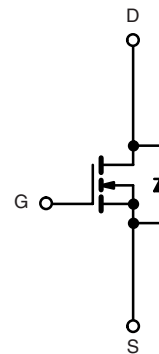
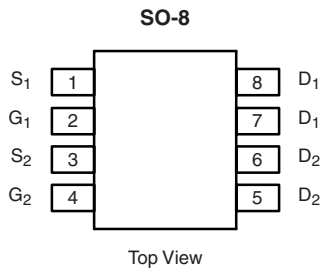
PRODUCT SUMMARY		
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
100	0.150 at V _{GS} = 10 V	2.6
	0.180 at V _{GS} = 6 V	2.4

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFETs
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE
Available



N-Channel MOSFET

Ordering Information: Si4982DY-T1-E3 (Lead (Pb)-free)
Si4982DY-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	100	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	2.6	A
		T _A = 70 °C	2.1	
Pulsed Drain Current	I _{DM}	20		
Continuous Source Current (Diode Conduction) ^a	I _S	1.7		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	2.0	W
		T _A = 70 °C	1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limit	Unit	
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W	

Notes:

a. Surface Mounted on FR4 board, t ≤ 10 s.

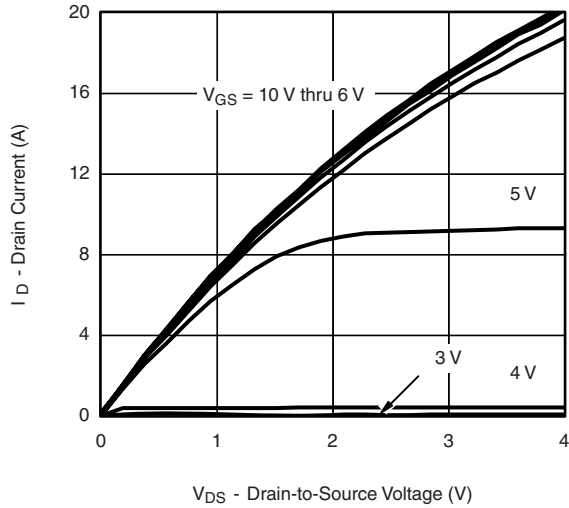
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ. ^a	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$			20	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}$, $V_{GS} = 10\text{ V}$	15			A
Drain-Source On-State Resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 2.6\text{ A}$		0.130	0.150	Ω
		$V_{GS} = 6\text{ V}$, $I_D = 2.4\text{ A}$		0.140	0.180	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 2.6\text{ A}$		11		S
Diode Forward Voltage ^b	V_{SD}	$I_S = 1.7\text{ A}$, $V_{GS} = 0\text{ V}$			1.2	V
Dynamic^a						
Gate Charge	Q_g	$V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 2.6\text{ A}$		15	30	nC
Gate-Source Charge	Q_{gs}			2.7		
Gate-Drain Charge	Q_{gd}			4.0		
Gate Resistance	R_g		1		4.4	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}$, $R_L = 50\text{ }\Omega$ $I_D \cong 1\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 6\text{ }\Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			30	60	
Fall Time	t_f			10	20	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}$		60	90	

Notes:

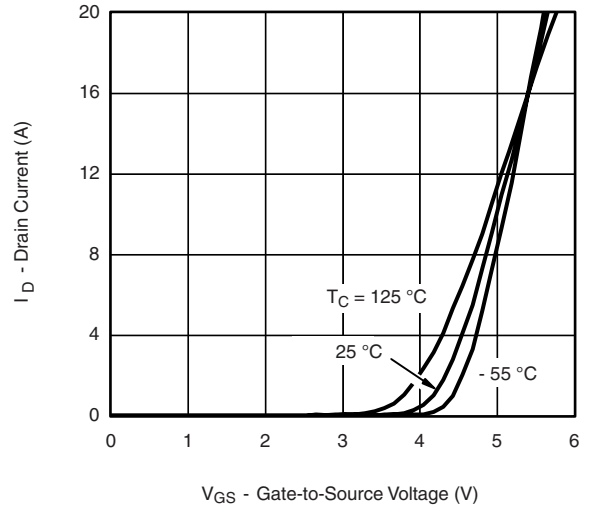
- a. For design aid only; not subject to production testing.
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

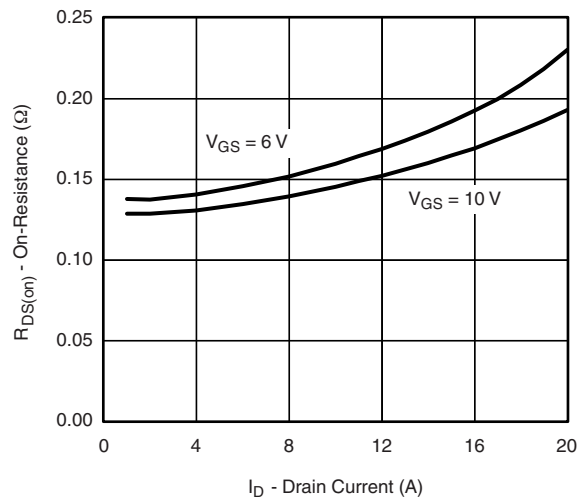
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



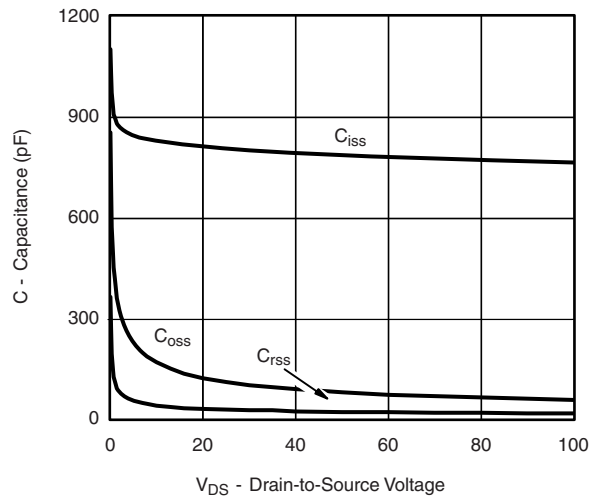
Output Characteristics



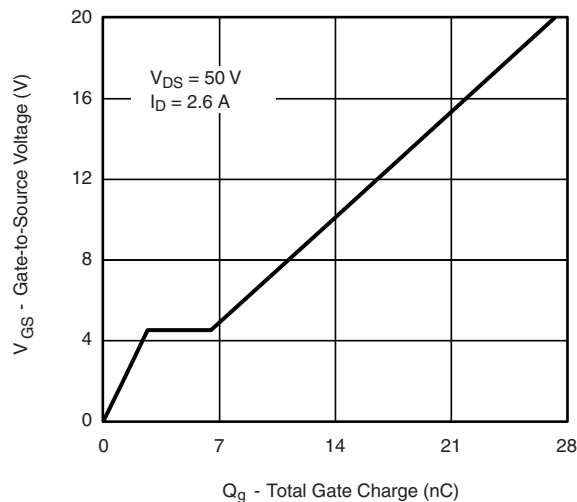
Transfer Characteristics



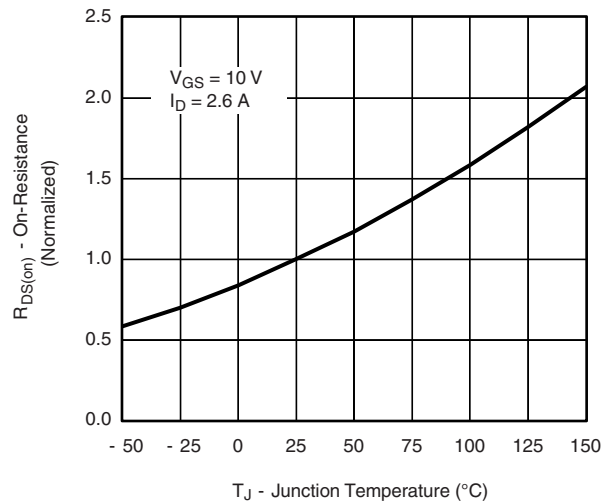
On-Resistance vs. Drain Current



Capacitance

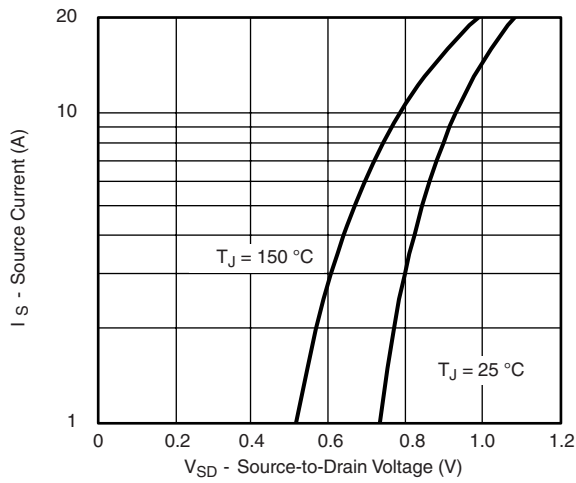


Gate Charge

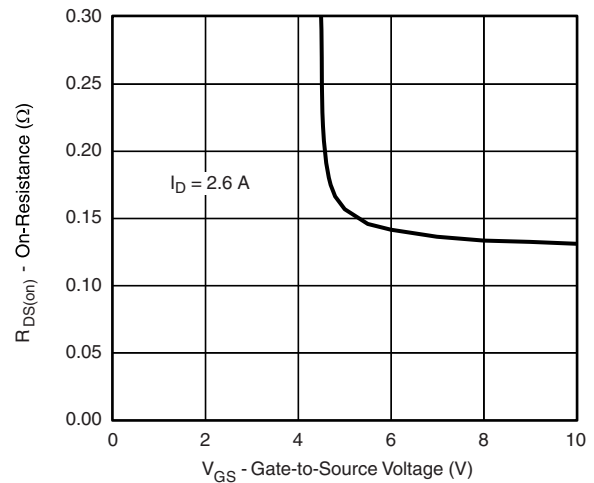


On-Resistance vs. Junction Temperature

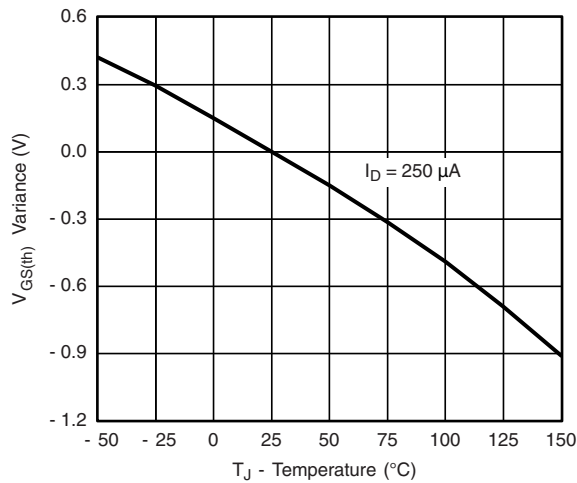
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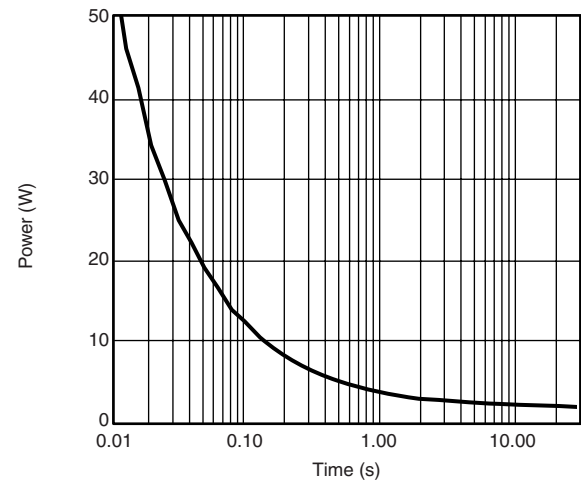
Source-Drain Diode Forward Voltage



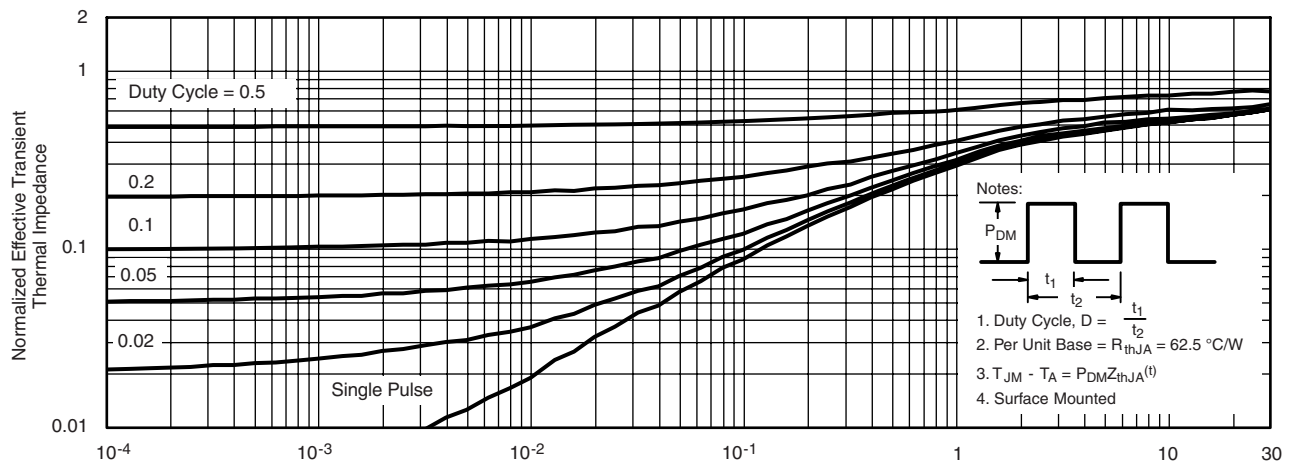
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

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