



SILICON LABS

# Si5350B-B

## FACTORY-PROGRAMMABLE ANY-FREQUENCY CMOS CLOCK GENERATOR + VCXO

### Features

- [www.silabs.com/custom-timing](http://www.silabs.com/custom-timing)
- Generates up to 8 non-integer-related frequencies from 2.5 kHz to 200 MHz
- Exact frequency synthesis at each output (0 ppm error)
- Highly linear VCXO gain (kv)
- Glitchless frequency changes
- Low output period jitter: < 70 ps pp, typ
- Configurable Spread Spectrum selectable at each output
- User-configurable control pins:
  - Output Enable (OEB\_0/1/2)
  - Power Down (PDN)
  - Frequency Select (FS\_0/1)
  - Spread Spectrum Enable (SSEN)
- Supports static phase offset
- Rise/fall time control
- Operates from a low-cost, fixed frequency AT-cut, non-pullable crystal: 25 or 27 MHz
- Separate voltage supply pins provide level translation:
  - Core VDD: 2.5 V or 3.3 V
  - Output VDDO: 1.8 V, 2.5 V, or 3.3 V
- Excellent PSRR eliminates external power supply filtering
- Very low power consumption (25 mA, core, typ)
- Available in 2 packages types:
  - 10-MSOP: 3 outputs
  - 20-QFN (4x4 mm): 8 outputs
- PCIe Gen 1 compliant
- Supports HCSL compatible swing

**10-MSOP**



**20-QFN**



**Ordering Information:**  
See page 20

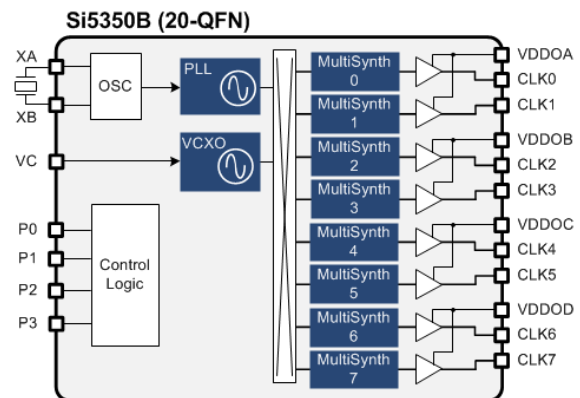
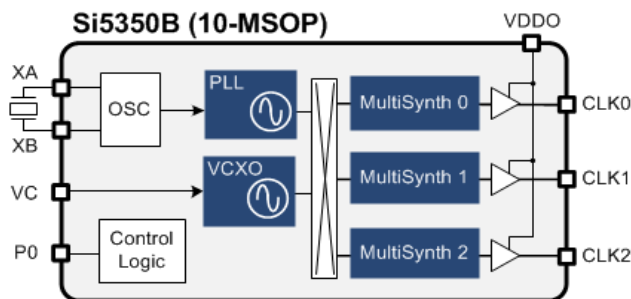
### Applications

- HDTV, DVD/Blu-ray, set-top box
- Audio/video equipment, gaming
- Printers, scanners, projectors
- Handheld instrumentation
- Residential gateways
- Networking/communication
- Servers, storage
- XO replacement

### Description

The Si5350B combines a clock generator and VCXO function into a single device. A flexible architecture enables this user definable custom timing device to generate any of the specified output frequencies from either the internal PLL or the VCXO. This allows the Si5350B to replace multiple crystals, crystal oscillators, and VCXOs. Custom pin-controlled Si5350B devices can be requested using the ClockBuilder web-based part number utility: [www.silabs.com/ClockBuilder](http://www.silabs.com/ClockBuilder).

### Functional Block Diagram



# Si5350B-B

Table 1. The Complete Si5350/51 Clock Generator Family

Part Number	I2C or Pin	Frequency Reference	Programmed?	Outputs	Datasheet
Si5351A-B-GT	I2C	XTAL only	Blank	3	Si5351-B
Si5351A-B-GM	I2C	XTAL only	Blank	8	Si5351-B
Si5351B-B-GM	I2C	XTAL and/or Voltage	Blank	8	Si5351-B
Si5351C-B-GM	I2C	XTAL and/or CLKIN	Blank	8	Si5351-B
Si5351A-Bxxxxx-GT	I2C	XTAL only	Factory Pre-Programmed	3	Si5351-B
Si5351A-Bxxxxx-GM	I2C	XTAL only	Factory Pre-Programmed	8	Si5351-B
Si5351B-Bxxxxx-GM	I2C	XTAL and/or Voltage	Factory Pre-Programmed	8	Si5351-B
Si5351C-Bxxxxx-GM	I2C	XTAL and/or CLKIN	Factory Pre-Programmed	8	Si5351-B
Si5350A-Bxxxxx-GT	Pin	XTAL only	Factory Pre-Programmed	3	Si5350A-B
Si5350A-Bxxxxx-GM	Pin	XTAL only	Factory Pre-Programmed	8	Si5350A-B
Si5350B-Bxxxxx-GT	Pin	XTAL and/or Voltage	Factory Pre-Programmed	3	Si5350B-B
Si5350B-Bxxxxx-GM	Pin	XTAL and/or Voltage	Factory Pre-Programmed	8	Si5350B-B
Si5350C-Bxxxxx-GT	Pin	XTAL and/or CLKIN	Factory Pre-Programmed	3	Si5350C-B
Si5350C-Bxxxxx-GM	Pin	XTAL and/or CLKIN	Factory Pre-Programmed	8	Si5350C-B

**Notes:**

1. XTAL = 25/27 MHz, Voltage = 0 to VDD, CLKIN = 10 to 100 MHz. "xxxxx" = unique custom code.
2. Create custom, factory pre-programmed parts at [www.silabs.com/ClockBuilder](http://www.silabs.com/ClockBuilder).

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## 1. Electrical Specifications

**Table 2. Recommended Operating Conditions**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Temperature	$T_A$		-40	25	85	°C
Core Supply Voltage	$V_{DD}$		3.0	3.3	3.60	V
			2.25	2.5	2.75	V
Output Buffer Voltage	$V_{DDOx}$		1.71	1.8	1.89	V
			2.25	2.5	2.75	
			3.0	3.3	3.60	

**Note:** All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted. VDD and VDDOx can be operated at independent voltages. Power supply sequencing for VDD and VDDOx requires that all VDDOx be powered up either before or at the same time as VDD.

**Table 3. DC Characteristics**

( $V_{DD} = 2.5\text{ V} \pm 10\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Core Supply Current*	$I_{DD}$	Enabled 3 outputs	—	20	30	mA
		Enabled 8 outputs	—	25	40	mA
		Power Down (PDN = $V_{DD}$ )	—	—	50	µA
Output Buffer Supply Current (Per Output)*	$I_{DDOx}$	$C_L = 5\text{ pF}$	—	2.2	5.6	mA
Input Current	$I_{P0-P3}$	Pins P0, P1, P2, P3 $V_{P0-P3} < 3.6\text{ V}$	—	—	10	µA
	$I_{VC}$	VC	—	—	30	µA
Output Impedance	$Z_{OI}$	3.3 V VDDO, default high drive	—	50	—	Ω

**\*Note:** Output clocks less than or equal to 100 MHz.

**Table 4. AC Characteristics** $(V_{DD} = 2.5\text{ V} \pm 10\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
VCXO Control Voltage Range	V <sub>c</sub>		0	V <sub>DD</sub> /2	V <sub>DD</sub>	V
VCXO Gain (configurable)	k <sub>v</sub>	V <sub>c</sub> = 10–90% of V <sub>DD</sub>	18	—	150	ppm/V
VCXO Control Voltage Linearity	KVL	V <sub>c</sub> = 10–90% of V <sub>DD</sub>	–5	—	+5	%
VCXO Pull Range (configurable)*	PR	V <sub>DD</sub> = 3.3 V V <sub>c</sub> = 10–90% of V <sub>DD</sub>	±30	0	±240	ppm
VCXO Modulation Bandwidth			—	10	—	kHz
Power-Up Time	TRDY	From V <sub>DD</sub> = V <sub>DDmin</sub> to valid output clock, C <sub>L</sub> = 5 pF, f <sub>CLKn</sub> > 1 MHz	—	2	10	ms
Power-Up Time, PLL Bypass Mode	TBYP	From V <sub>DD</sub> = V <sub>DDmin</sub> to valid output clock, C <sub>L</sub> = 5 pF, f <sub>CLKn</sub> > 1 MHz	—	0.5	1	ms
Output Enable Time	T <sub>OE</sub>	From OEB assertion to valid clock output, C <sub>L</sub> = 5 pF, f <sub>CLKn</sub> > 1 MHz	—	—	10	µs
Output Frequency Transition Time	T <sub>FREQ</sub>	f <sub>CLKn</sub> > 1 MHz	—	—	10	µs
Spread Spectrum Frequency Deviation	SS <sub>DEV</sub>	Down spread. Selectable in 0.1% steps.	–0.1	—	–2.5	%
Spread Spectrum Modulation Rate	SS <sub>MOD</sub>		30	31.5	33	kHz

\*Note: Contact Silicon Labs for VCXO operation at 2.5 V.

**Table 5. Input Characteristics** $(V_{DD} = 2.5\text{ V} \pm 10\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $85^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Crystal Frequency	f <sub>XTAL</sub>		25	—	27	MHz
VC Input Resistance			100	—	—	kΩ
P0-P3 Input Low Voltage	V <sub>IL_P0-3</sub>		–0.1	—	0.3 x V <sub>DD</sub>	V
P0-P3 Input High Voltage	V <sub>IH_P0-3</sub>		0.7 x V <sub>DD</sub>	—	3.60	V

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**Table 6. Output Characteristics**

( $V_{DD} = 2.5\text{ V} \pm 10\%$ , or  $3.3\text{ V} \pm 10\%$ ,  $T_A = -40\text{ to }85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Frequency Range <sup>1</sup>	FCLK		0.0025	—	200	MHz
Load Capacitance	$C_L$	$F_{CLK} < 100\text{ MHz}$	—	—	15	pF
Duty Cycle	DC	$F_{CLK} \leq 160\text{ MHz}$ , measured at $V_{DD}/2$	45	50	55	%
		$F_{CLK} > 160\text{ MHz}$ , measured at $V_{DD}/2$	40	50	60	%
Rise/Fall Time	$t_r/t_f$	20% - 80%, $C_L = 5\text{ pF}$	—	1	1.5	ns
Output High Voltage	VOH		$V_{DD} - 0.6$	—	—	V
Output Low Voltage	VOL		—	—	0.6	V
Period Jitter <sup>2,3</sup>	JPER	20-QFN, 4 outputs running, 1 per VDDO	—	40	95	ps pk-pk
		10-MSOP or 20-QFN, all outputs running	—	70	155	
Cycle-to-Cycle Jitter <sup>2,3</sup>	JCC	20-QFN, 4 outputs running, 1 per VDDO	—	50	90	ps pk
		10-MSOP or 20-QFN, all outputs running	—	70	150	
Period Jitter, VCXO <sup>2,3</sup>	JPER_VCXO	20-QFN, 4 outputs running, 1 per VDDO	—	50	95	ps pk-pk
		10-MSOP or 20-QFN, all outputs running	—	70	155	
Cycle-to-Cycle Jitter, VCXO <sup>2,3</sup>	JCC_VCXO	20-QFN, 4 outputs running, 1 per VDDO	—	50	90	ps pk
		10-MSOP or 20-QFN, all outputs running	—	70	150	

**Notes:**

1. Only two unique frequencies above 112.5 MHz can be simultaneously output.
2. Measured over 10k cycles. Jitter is only specified at the default high drive strength (50  $\Omega$  output impedance).
3. Jitter is highly dependent on device frequency configuration. Specifications represent a “worst case, real world” frequency plan; actual performance may be substantially better. Three-output 10MSOP package measured with clock outputs of 74.25, 24.576, and 48 MHz. Eight-output 20QFN package measured with clock outputs of 33.33, 74.25, 27, 24.576, 22.5792, 28.322, 125, and 48 MHz.

Table 7. 25 MHz Crystal Requirements<sup>1,2</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	$f_{XTAL}$	—	25	—	MHz
Load Capacitance	$C_L$	6	—	12	pF
Equivalent Series Resistance	$r_{ESR}$	—	—	150	$\Omega$
Crystal Max Drive Level	$d_L$	100	—	—	$\mu W$

**Notes:**

- Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitance in addition to external 2 pF load capacitance (e.g., by using 4 pF capacitors on XA and XB).
- Refer to "AN551: Crystal Selection Guide" for more details.

Table 8. 27 MHz Crystal Requirements<sup>1,2</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Crystal Frequency	$f_{XTAL}$	—	27	—	MHz
Load Capacitance	$C_L$	6	—	12	pF
Equivalent Series Resistance	$r_{ESR}$	—	—	150	$\Omega$
Crystal Max Drive Level Spec	$d_L$	100	—	—	$\mu W$

**Notes:**

- Crystals which require load capacitances of 6, 8, or 10 pF should use the device's internal load capacitance for optimum performance. See register 183 bits 7:6. A crystal with a 12 pF load capacitance requirement should use a combination of the internal 10 pF load capacitance in addition to external 2 pF load capacitance (e.g., by using 4 pF capacitors on XA and XB).
- Refer to "AN551: Crystal Selection Guide" for more details.

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Table 9. Thermal Conditions

Parameter	Symbol	Test Condition	Package	Value	Unit
Thermal Resistance Junction to Ambient	$\theta_{JA}$	Still Air	10-MSOP	131	°C/W
			20-QFN	119	°C/W
Thermal Resistance Junction to Case	$\theta_{JC}$	Still Air	20-QFN	16	°C/W

Table 10. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Value	Unit
DC Supply Voltage	$V_{DD\_max}$		-0.5 to 3.8	V
Input Voltage	VIN_P0-3	Pins P0, P1, P2, P3	-0.5 to 3.8	V
	VIN_VC	VC	-0.5 to (VDD+0.3)	V
	VIN_XA/ B	Pins XA, XB	-0.5 to 1.3 V	V
Temperature Range	$T_J$		-55 to 150	°C

**Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



## 2. Typical Application

### 2.1. Si5350B Replaces Multiple Clocks and XOs

The Si5350B is a clock generation device that provides both synchronous and free-running clocks for applications where power, board size, and cost are critical. An application where both free-running and synchronous clocks are required is shown in Figure 1.

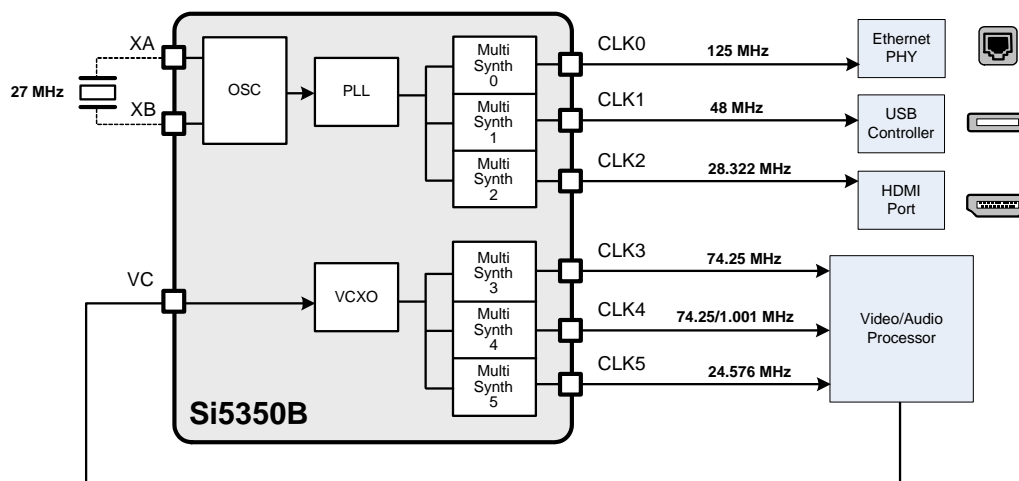


Figure 1. Example of an Si5350B in an Audio/Video Application

### 2.2. Applying a Reference Clock at XTAL Input

The Si5350B can be driven with a clock signal through the XA input pin.

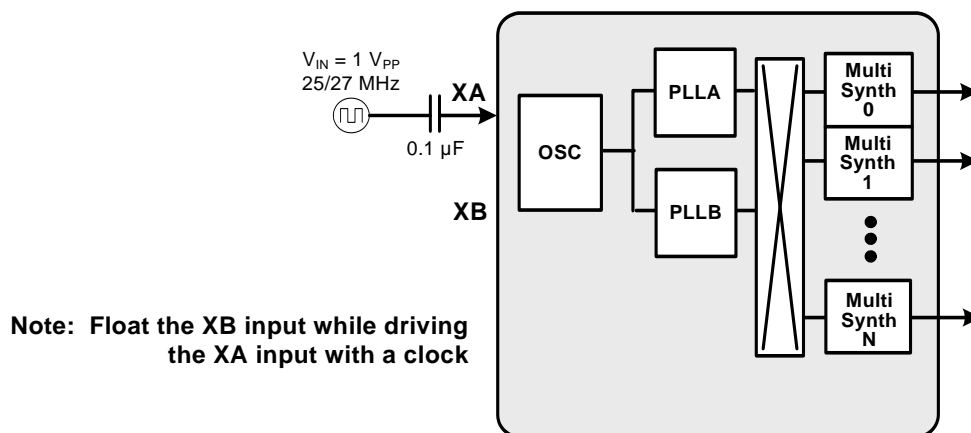


Figure 2. Si5350B Driven by a Clock Signal

## 2.3. HCSL Compatible Outputs

The Si5350B can be configured to support HCSL compatible swing when the VDDO of the output pair of interest is set to 2.5 V (i.e., VDDOA must be 2.5 V when using CLK0/1; VDDOB must be 2.5 V for CLK2/3 and so on).

The circuit in the figure below must be applied to each of the two clocks used, and one of the clocks in the pair must also be inverted to generate a differential pair.

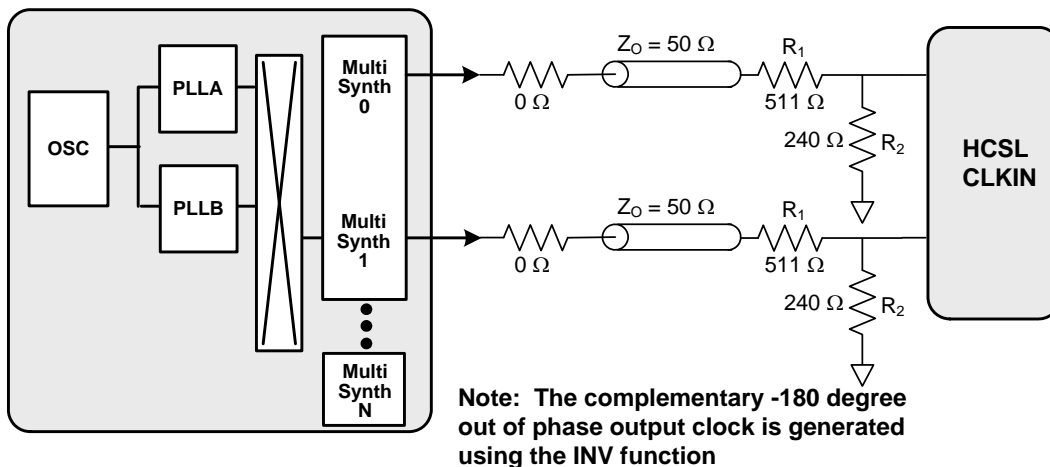


Figure 3. Si5350B Output is HCSL Compatible

### 3. Functional Description

The Si5350B features a high-frequency PLL, a high-frequency VCXO and a high-resolution fractional MultiSynth™ divider on each output. A block diagram of both the 3-output and the 8-output clock generators are shown in Figure 4. Free-running clocks are generated from the on-chip oscillator + PLL, and a separate voltage controlled oscillator (VCXO) is used to generate synchronous clocks. A fixed-frequency non-pullable standard AT-cut crystal provides frequency stability for both the internal oscillator and VCXO. The flexible synthesis architecture of the Si5350B generates up to eight non-integer related frequencies and any combination of free-running and/or synchronous clocks.

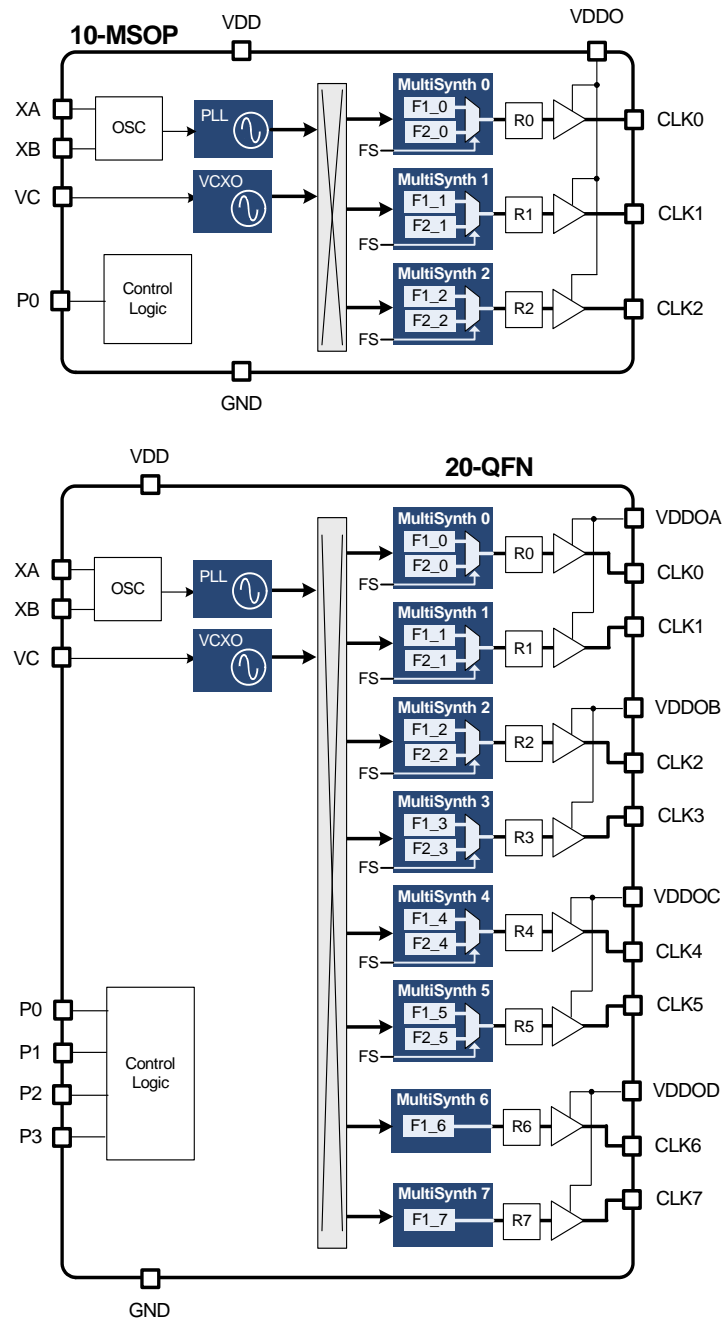


Figure 4. Block Diagram of the 3 and 8 Output Si5350B Devices

## 4. Configuring the Si5350B

The Si5350B is a factory-programmed custom clock generator that is user definable with a simple to use web-based utility ([www.silabs.com/ClockBuilder](http://www.silabs.com/ClockBuilder)). The ClockBuilder utility provides a simple graphical interface that allows the user to enter input and output frequencies along with other custom features as described in the following sections. All synthesis calculations are automatically performed by ClockBuilder to ensure an optimum configuration. A unique part number is assigned to each custom configuration.

### 4.1. Crystal Inputs (XA, XB)

The Si5350B uses a fixed-frequency non-pullable standard AT-cut crystal as a reference to synthesize its output clocks and to provide the frequency stability for the VCXO.

#### 4.1.1. Crystal Frequency

The Si5350B can operate using either a 25 MHz or a 27 MHz crystal.

#### 4.1.2. Internal XTAL Load Capacitors

Internal load capacitors are provided to eliminate the need for external components when connecting a XTAL to the Si5350B. The total internal XTAL load capacitance ( $C_L$ ) can be selected to be 0, 6, 8, or 10 pF. XTALs with alternate load capacitance requirements are supported using additional external load capacitance  $\leq 2$  pF (e.g., by using  $\leq 4$  pF capacitors on XA and XB) as shown in Figure 5.

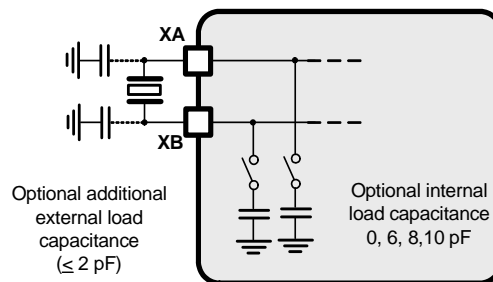


Figure 5. External XTAL with Optional Load Capacitors

### 4.2. Output Clocks (CLK0–CLK7)

The Si5350B is orderable as a 3-output (10-MSOP) or 8-output (20-QFN) clock generator. Output clocks CLK0 to CLK5 can be ordered with two clock frequencies (F1\_x, F2\_x) which are selectable with the optional frequency select pins (FS0/1). See “4.3.3. Frequency Select (FS\_0, FS\_1)” for more details on the operation of the frequency select pins. Each output clock can select its reference either from the PLL or from the VCXO.

#### 4.2.1. Output Clock Frequency

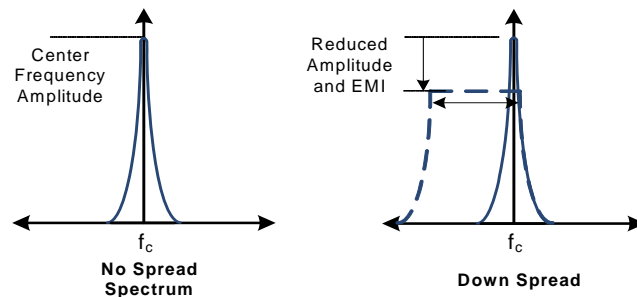
Outputs can be configured at any frequency from 2.5 kHz up to 200 MHz. However, only two unique frequencies above 112.5 MHz can be simultaneously output. For example, 125 MHz (CLK0), 130 MHz (CLK1), and 150 MHz (CLKx) is not allowed. Note that multiple copies of frequencies above 112.5 MHz can be provided, for example, 125 MHz could be provided on four outputs (CLKS0-3) simultaneously with 130 MHz on four different outputs (CLKs4-7).

#### 4.2.2. Spread Spectrum

Spread spectrum can be enabled on any of the clock outputs that use PLLA as its reference. Spread spectrum is useful for reducing electromagnetic interference (EMI). Enabling spread spectrum on an output clock modulates its frequency, which effectively reduces the overall amplitude of its radiated energy. Note that spread spectrum is not available on clocks synchronized to PLLB or to the VCXO.

The Si5350B supports several levels of spread spectrum allowing the designer to choose an ideal compromise between system performance and EMI compliance. An optional spread spectrum enable pin (SSEN) is configurable to enable or disable the spread spectrum feature. See “4.3.1. Spread Spectrum Enable (SSEN)” for

details.



**Figure 6. Available Spread Spectrum Profiles**

#### 4.2.3. Invert/Non-Invert

By default, each of the output clocks are generated in phase (non-inverted) with respect to each other. An option to invert any of the clock outputs is also available.

#### 4.2.4. Output State When Disabled

There are up to three output enable pins configurable on the Si5350B as described in “4.3.4. Output Enable (OEB\_0, OEB\_1, OEB\_2)”. The output state when disabled for each of the outputs is configurable as one of the following: disable low, disable high, or disable in high-impedance.

#### 4.2.5. Powering Down Unused Outputs

Unused clock outputs can be completely powered down to conserve power.

### 4.3. Programmable Control Pins (P0–P3) Options

Up to four programmable control pins (P0-P3) are configurable allowing direct pin control of the following features:

#### 4.3.1. Spread Spectrum Enable (SSEN)

An optional control pin allows disabling the spread spectrum feature for all outputs that were configured with spread spectrum enabled. Hold SSEN low to disable spread spectrum. The SSEN pin provides a convenient method of evaluating the effect of using spread spectrum clocks during EMI compliance testing.

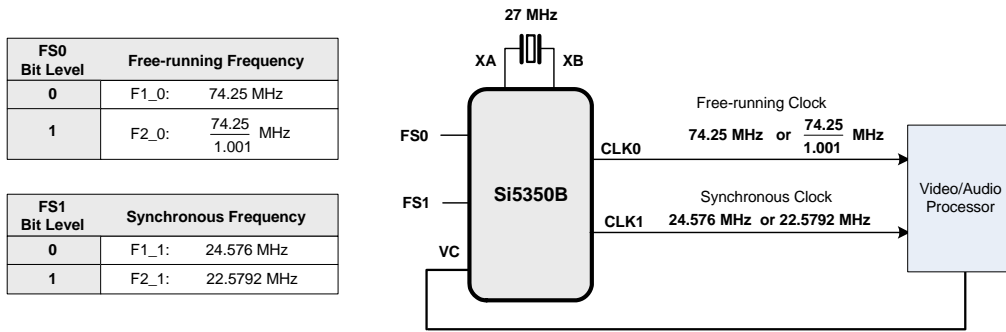
#### 4.3.2. Power Down (PDN)

An optional power down control pin allows a full shutdown of the Si5350B to minimize power consumption when its output clocks are not being used. The Si5350B is in normal operation when the PDN pin is held low and is in power down mode when held high. Power consumption when the device is in power down mode is indicated in Table 3 on page 4.

#### 4.3.3. Frequency Select (FS\_0, FS\_1)

The Si5350B offers the option of configuring up to two frequencies per clock output (CLK0-CLK5) for either free-running or synchronous clocks. This is a useful feature for applications that need to support more than one free-running or synchronous clock rate on the same output. An example of this is shown in Figure 7. The FS pins select which frequency is generated from the clock output. In this example FS0 selects the output frequency on CLK0, and FS1 selects the frequency on CLK1.

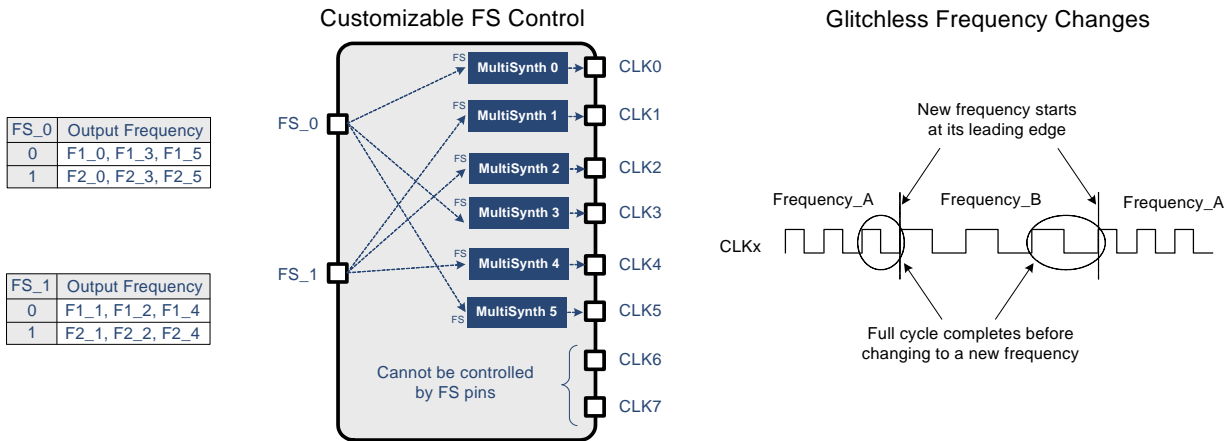
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**Figure 7. Example of Generating Two Clock Frequencies from the Same Clock Output**

Up to two frequency select pins are available on the Si5350B. Each of the frequency select pins can be linked to any of the clock outputs as shown in Figure 8. For example, FS\_0 can be linked to control clock frequency selection on CLK0, CLK3, and CLK5; FS\_1 can be used to control clock frequency selection on CLK1, CLK2, and CLK4. Any other combination is also possible. The frequency select feature is not available for CLKs 6 and 7.

The Si5350B uses control circuitry to ensure that frequency changes are glitchless. This ensures that the clock always completes its last cycle before starting a new clock cycle of a different frequency.

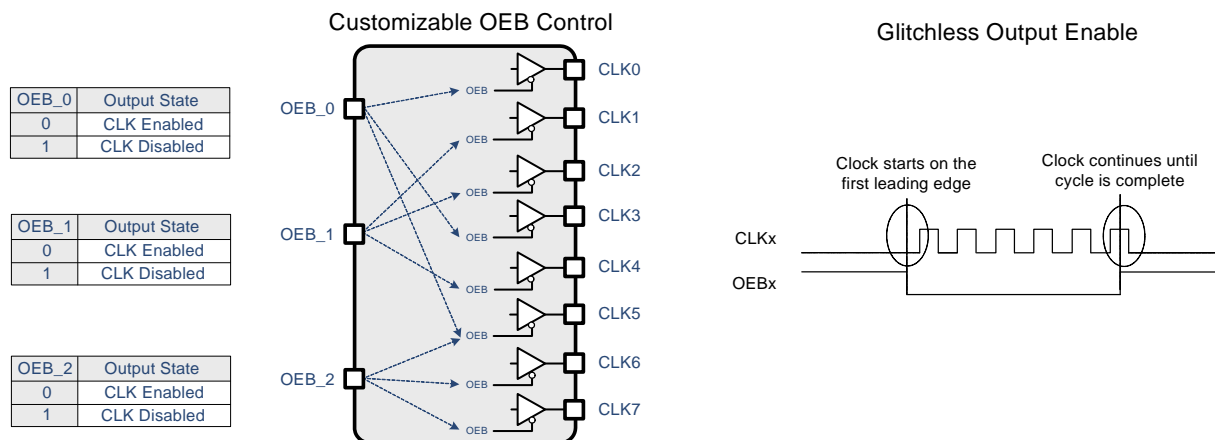


**Figure 8. Example Configuration of a Pin-Controlled Frequency Select (FS)**

#### 4.3.4. Output Enable (OEB\_0, OEB\_1, OEB\_2)

Up to three output enable pins (OEB\_0/1/2) are available on the Si5350B. Similar to the FS pins, each OEB pin can be linked to any of the output clocks. In the example shown in Figure 9, OEB\_0 is linked to control CLK0, CLK3, and CLK5; OEB\_1 is linked to control CLK6 and CLK7, and OEB\_2 is linked to control CLK1, CLK2, CLK4, and CLK5. Any other combination is also possible. If more than one OEB pin is linked to the same CLK output, the pin forcing a disable state will be dominant. Clock outputs are enabled when the OEB pin is held low.

The output enable control circuitry ensures glitchless operation by starting the output clock cycle on the first leading edge after OEB is asserted (OEB = low). When OEB is released (OEB = high), the clock is allowed to complete its full clock cycle before going into a disabled state. This is shown in Figure 9. When disabled, the output state is configurable as disabled high, disabled low, or disabled in high-impedance.



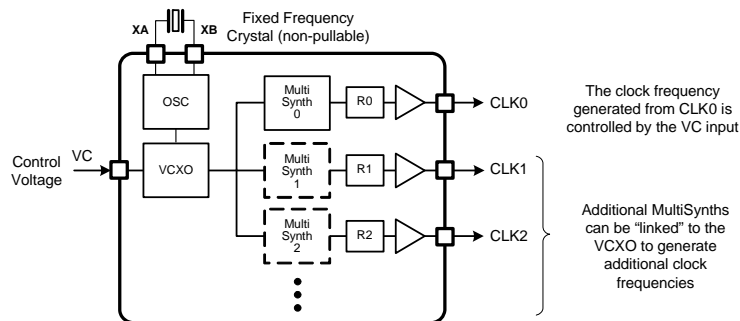
**Figure 9. Example Configuration of a Pin-Controlled Output Enable**

## 4.4. Voltage Control Input (VC)

The VCXO architecture of the Si5350B eliminates the need for an external pullable crystal. Only a standard, low-cost, fixed-frequency (25 or 27 MHz) AT-cut crystal is required.

The tuning range of the VCXO is configurable allowing for a wide variety of applications. Key advantages of the VCXO design in the Si5350B include high linearity, a wide operating range (linear from 10 to 90% of VDD), and reliable startup and operation. Refer to Table 4 on page 5 for VCXO specification details.

A unique feature of the Si5350B is its ability to generate multiple output frequencies controlled by the same control voltage applied to the VC pin. This replaces multiple PLLs or VCXOs that would normally be locked to the same reference. An example is illustrated in Figure 10.

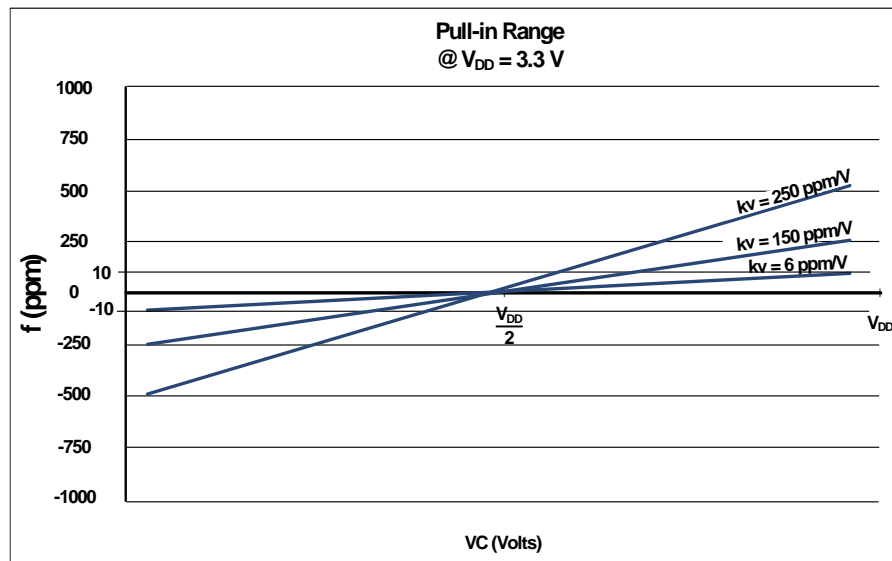


**Figure 10. Using the Si5350B as a Multi-Output VCXO**

### 4.4.1. Control Voltage Gain (kV)

The voltage level on the VC pin directly controls the output frequency. The rate of change in output clock frequency (kV) is configurable from 18 ppm/V up to 150 ppm/V. This allows a configurable pull range from  $\pm 30$  ppm to  $\pm 240$  ppm @  $V_{DD} = 3.3$  V as shown in Figure 11. Consult the factory for other pull range values.

A key advantage of the VCXO design in the Si5350B is its highly linear tuning range. This allows better control of PLL stability and jitter performance over the entire control voltage range.



**Figure 11. User-definable VCXO Pull Range**



## 4.5. Design Considerations

The Si5350B is a self-contained clock generator that requires very few external components. The following general guidelines are recommended to ensure optimum performance.

### 4.5.1. Power Supply Decoupling/Filtering

The Si5350B has built-in power supply filtering circuitry to help keep the number of external components to a minimum. All that is recommended is one 0.1 to 1.0  $\mu\text{F}$  decoupling capacitor per power supply pin. This capacitor should be mounted as close to the VDD and VDDO pins as possible without using vias.

### 4.5.2. Power Supply Sequencing

The VDD and VDDOx (i.e., VDDO0, VDDO1, VDDO2, VDDO3) power supply pins have been separated to allow flexibility in output signal levels. Power supply sequencing for VDD and VDDOx requires that all VDDOx be powered up either before or at the same time as VDD. Unused VDDOx pins should be tied to VDD.

### 4.5.3. External Crystal

The external crystal should be mounted as close to the pins as possible using short PCB traces. The XA and XB traces should be kept away from other high-speed signal traces. See “AN551: Crystal Selection Guide” for more details.

### 4.5.4. External Crystal Load Capacitors

The Si5350B provides the option of using internal and external crystal load capacitors. If external load capacitors are used, they should be placed as close to the XA/XB pads as possible. See “AN551: Crystal Selection Guide” for more details.

### 4.5.5. Unused Pins

Unused control pins (P0–P4) should be tied to GND.

Unused voltage control pin should be tied to GND.

Unused output pins (CLK0–CLK7) should be left floating.

### 4.5.6. Trace Characteristics

The Si5350B features various output drive strength settings. It is recommended to configure the trace characteristics as shown in Figure 12 when the default high output drive setting is used.

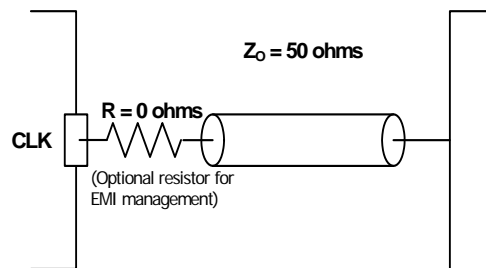


Figure 12. Recommended Trace Characteristics with Default Drive Strength Setting

# Si5350B-B

## 5. Pin Descriptions

### 5.1. 20-pin QFN

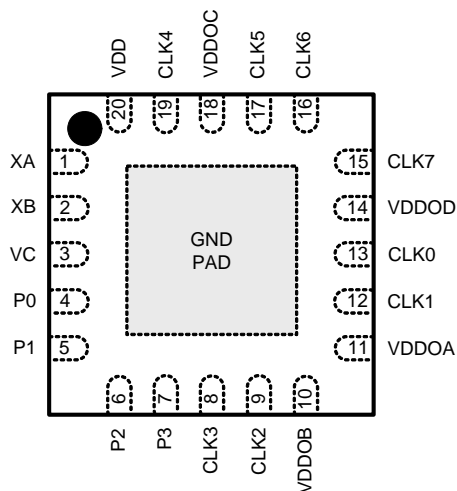


Figure 13. Si5350B 20-QFN Top View

Table 11. Si5350B 20-QFN Pin Descriptions

Pin Name	Pin Number	Pin Type*	Function
XA	1	I	Input pin for external XTAL
XB	2	I	Input pin for external XTAL
VC	3	I	VCXO control voltage input
CLK0	13	O	Output clock 0
CLK1	12	O	Output clock 1
CLK2	9	O	Output clock 2
CLK3	8	O	Output clock 3
CLK4	19	O	Output clock 4
CLK5	17	O	Output clock 5
CLK6	16	O	Output clock 6
CLK7	15	O	Output clock 7
P0	4	I	User configurable input pin 0
P1	5	I	User configurable input pin 1
P2	6	I	User configurable input pin 2
P3	7	I	User configurable input pin 3
VDD	20	P	Core voltage supply pin
VDDOA	11	P	Output voltage supply pin for CLK0 and CLK1
VDDOB	10	P	Output voltage supply pin for CLK2 and CLK3
VDDOC	18	P	Output voltage supply pin for CLK4 and CLK5
VDDOD	14	P	Output voltage supply pin for CLK6 and CLK7
GND	Center Pad	P	Ground

\*Note: Pin Types: I = Input, O = Output, P = Power.

## 5.2. 10-Pin MSOP

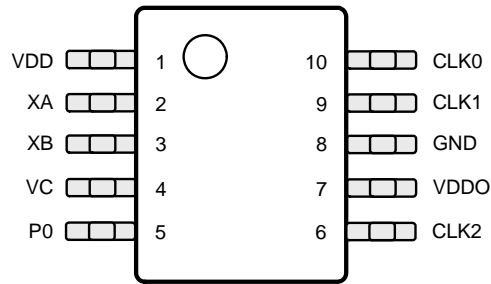


Figure 14. Si5350B 10-MSOP Top View

Table 12. Si5350B 10-MSOP Pin Descriptions

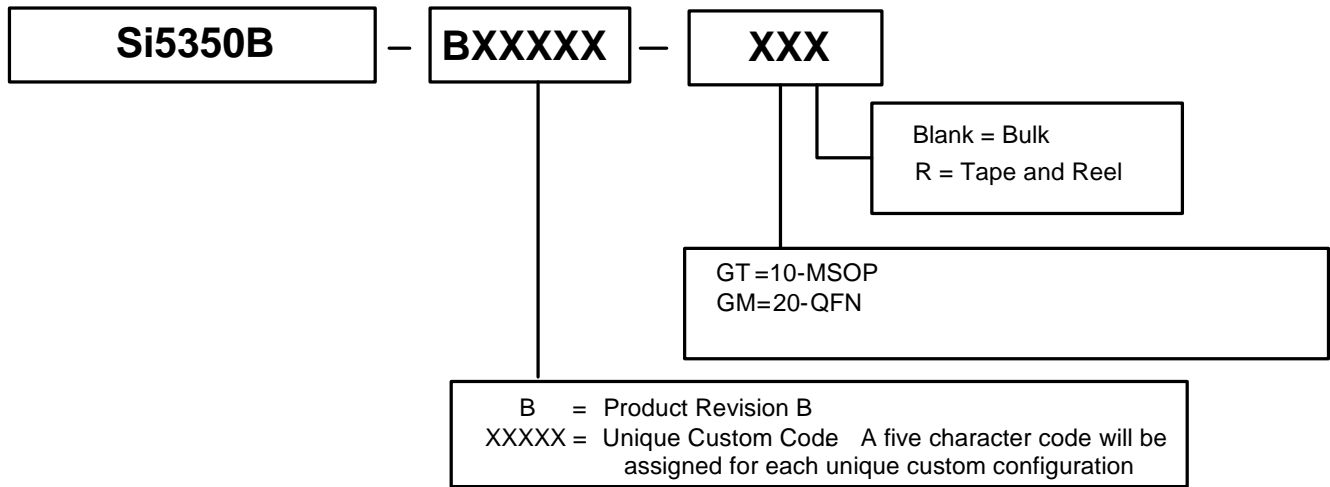
Pin Name	Pin Number	Pin Type*	Function
XA	2	I	Input pin for external XTAL
XB	3	I	Input pin for external XTAL
Vc	4	I	VCXO control voltage input
CLK0	10	O	Output clock 0
CLK1	9	O	Output clock 1
CLK2	6	O	Output clock 2
P0	5	I	User configurable input pin 0
VDD	1	P	Core voltage supply pin
VDDO	7	P	Output supply pin for CLK0, CLK1, and CLK2
GND	8	P	Ground

\*Note: Pin Types: I = Input, O = Output, P = Power.

# Si5350B-B

## 6. Ordering Information

Factory programmed Si5350B devices can be requested using the ClockBuilder web-based utility available at: [www.silabs.com/ClockBuilder](http://www.silabs.com/ClockBuilder). A unique part number is assigned to each custom configuration as indicated in Figure 15.



### Evaluation Boards

**Si535x-B20QFN-EVB**

For evaluation of  
Si5350B-Bxxxxx-GM (20 QFN)

Figure 15. Custom Clock Part Numbers

## 7. Package Outline

### 7.1. 20-pin QFN

Figure 16 illustrates the package details for the Si5350B-B. Table 13 lists the values for the dimensions shown in the illustration.

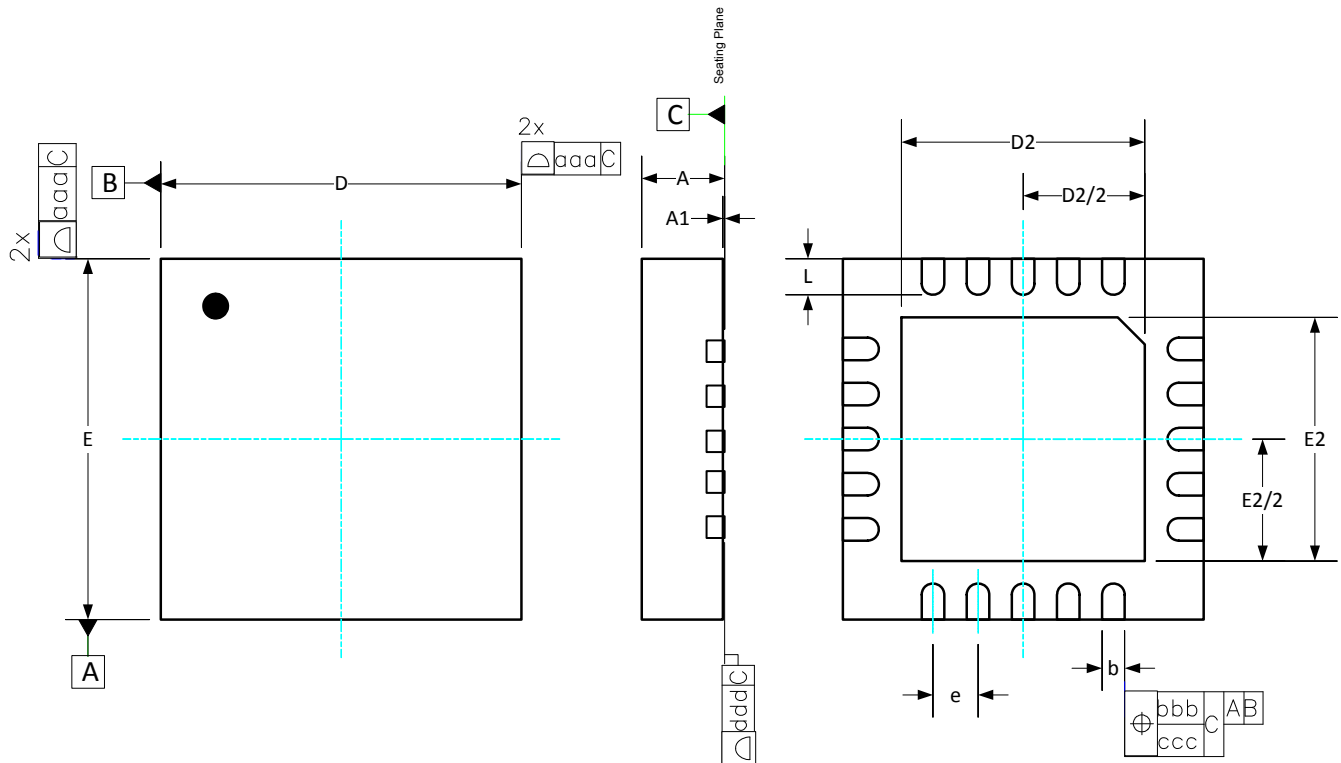


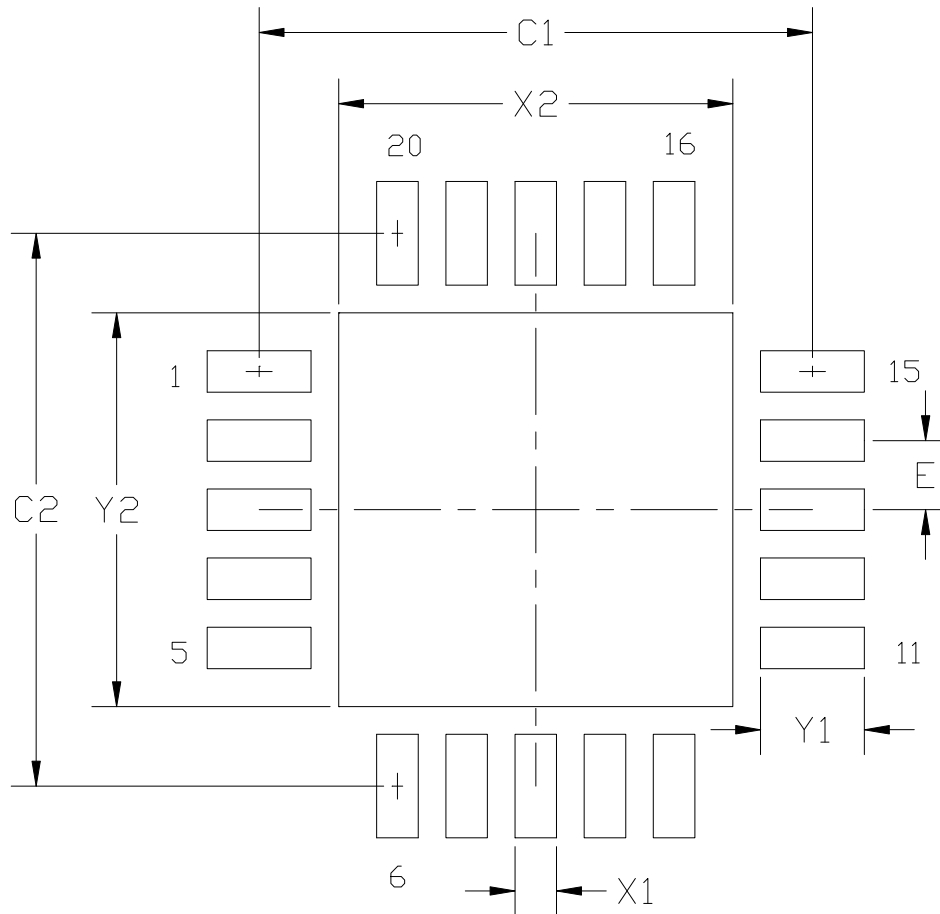
Figure 16. 20-pin QFN Package Drawing

**Table 13. Package Dimensions**

<b>Dimension</b>	<b>Min</b>	<b>Nom</b>	<b>Max</b>
A	0.80	0.85	0.90
A1	0.00	—	0.05
b	0.20	0.25	0.30
D	4.00 BSC		
D2	2.65	2.70	2.75
e	0.50 BSC		
E	4.00 BSC		
E2	2.65	2.70	2.75
L	0.35	0.40	0.45
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
<b>Notes:</b> <ol style="list-style-type: none"><li>1. All dimensions shown are in millimeters (mm) unless otherwise noted.</li><li>2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.</li><li>3. This drawing conforms to JEDEC Outline MO-220, variation VGGD-5.</li><li>4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.</li></ol>			

## 8. Land Pattern: 20-Pin QFN

Figure 17 shows the recommended land pattern details for the Si5350 in a 20-Pin QFN package. Table 14 lists the values for the dimensions shown in the illustration.



**Figure 17. 20-Pin QFN Land Pattern**

**Table 14. PCB Land Pattern Dimensions**

<b>Symbol</b>	<b>Millimeters</b>
C1	4.0
C2	4.0
E	0.50 BSC
X1	0.30
X2	2.70
Y1	0.80
Y2	2.70

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on IPC-7351 guidelines.

**Solder Mask Design**

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60  $\mu$ m minimum, all the way around the pad.

**Stencil Design**

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

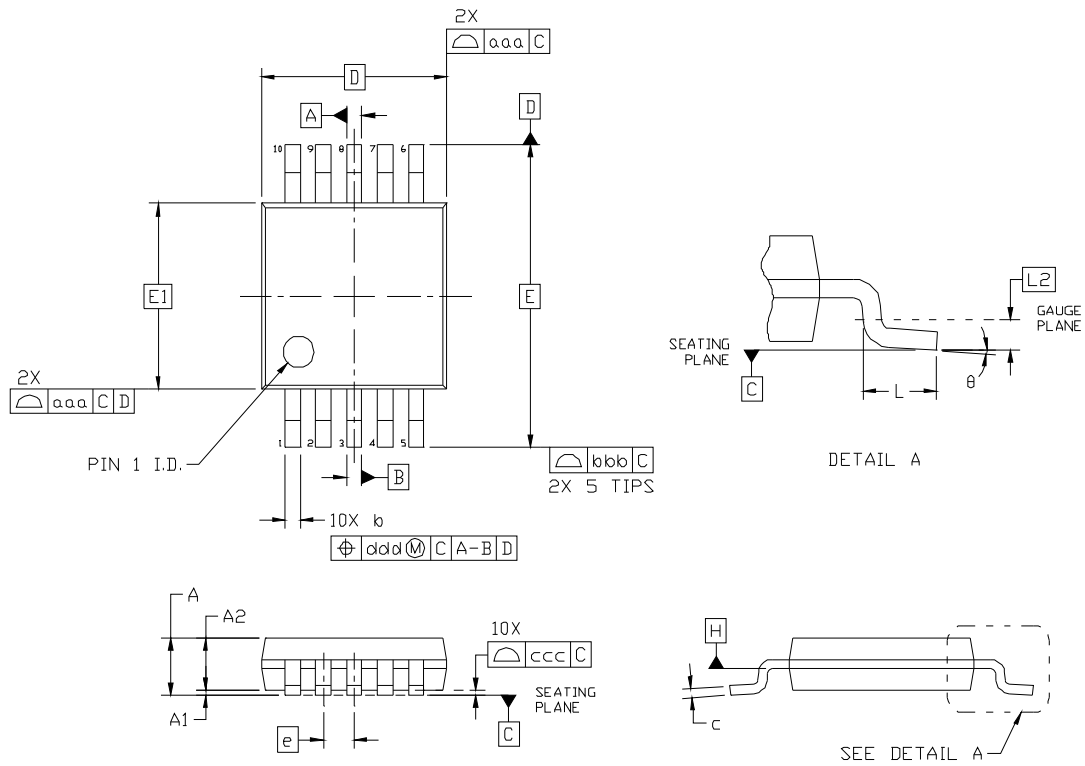
**Card Assembly**

8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body components.



## 8.1. 10-pin MSOP

Figure 18 illustrates the package details for the Si5350B-B. Table 15 lists the values for the dimensions shown in the illustration.



**Figure 18. 10-pin MSOP Package Drawing**

**Table 15. 10-MSOP Package Dimensions**

<b>Dimension</b>	<b>Min</b>	<b>Nom</b>	<b>Max</b>
A	—	—	1.10
A1	0.00	—	0.15
A2	0.75	0.85	0.95
b	0.17	—	0.33
c	0.08	—	0.23
D	3.00 BSC		
E	4.90 BSC		
E1	3.00 BSC		
e	0.50 BSC		
L	0.40	0.60	0.80
L2	0.25 BSC		
q	0	—	8
aaa	—	—	0.20
bbb	—	—	0.25
ccc	—	—	0.10
ddd	—	—	0.08

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-137, Variation C
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 9. Land Pattern: 10-Pin MSOP

Figure 19 shows the recommended land pattern details for the Si5350B-B in a 10-Pin MSOP package. Table 16 lists the values for the dimensions shown in the illustration.

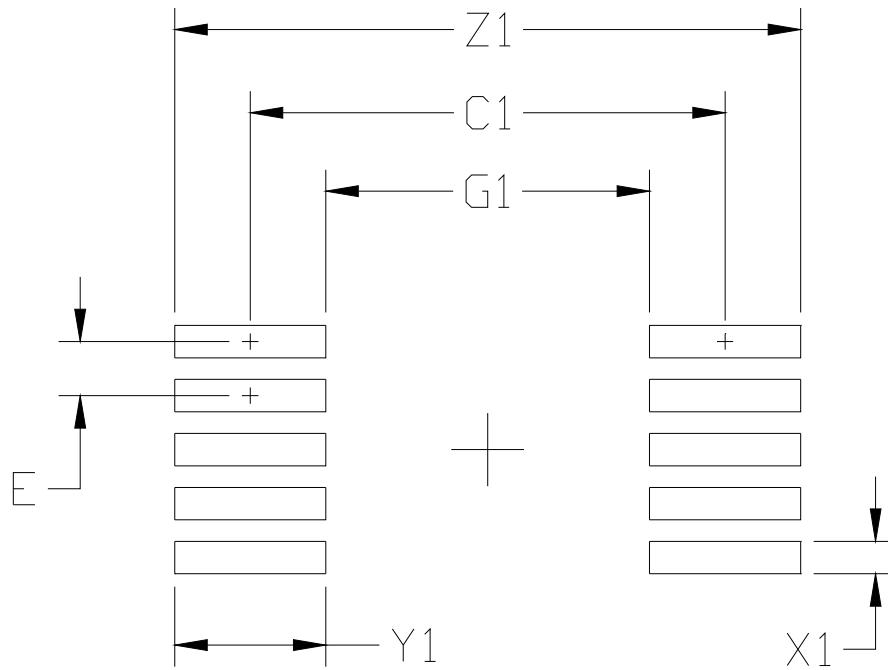


Figure 19. 10-Pin MSOP Land Pattern

**Table 16. PCB Land Pattern Dimensions**

Symbol	Millimeters	
	Min	Max
C1	4.40 REF	
E	0.50 BSC	
G1	3.00	—
X1	—	0.30
Y1	1.40 REF	
Z1	—	5.80

**Notes:**

**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ASME Y14.5M-1994.
3. This Land Pattern Design is based on the IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05mm.

**Solder Mask Design**

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

**Stencil Design**

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1.

**Card Assembly**

9. A No-Clean, Type-3 solder paste is recommended.
10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body components.

## 10. Top Marking

### 10.1. 20-Pin QFN Top Marking

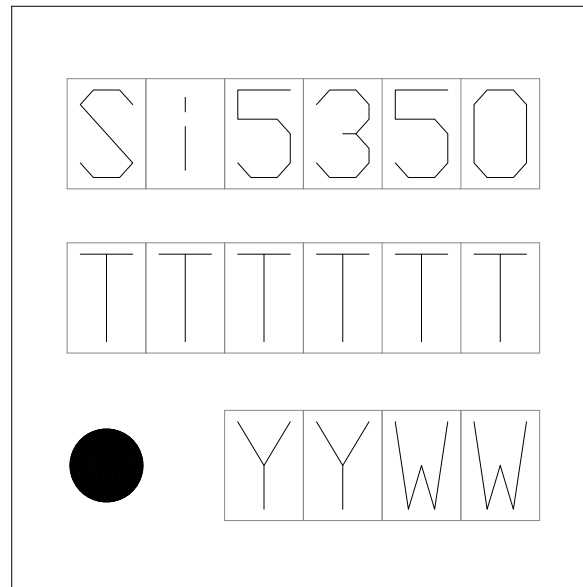


Figure 20. 20-Pin QFN Top Marking

### 10.2. Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Pin 1 Mark:</b>	Filled Circle = 0.50 mm Diameter (Bottom-Left Corner)	
<b>Font Size:</b>	0.60 mm (24 mils)	
<b>Line 1 Mark Format</b>	Device Part Number	Si5350
<b>Line 2 Mark Format:</b>	TTTTTT = Mfg Code*	Manufacturing Code from the Assembly Purchase Order Form.
<b>Line 3 Mark Format:</b>	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly date.
*Note: The code shown in the “TTTTTT” line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.		

## 10.3. 10-Pin MSOP Top Marking

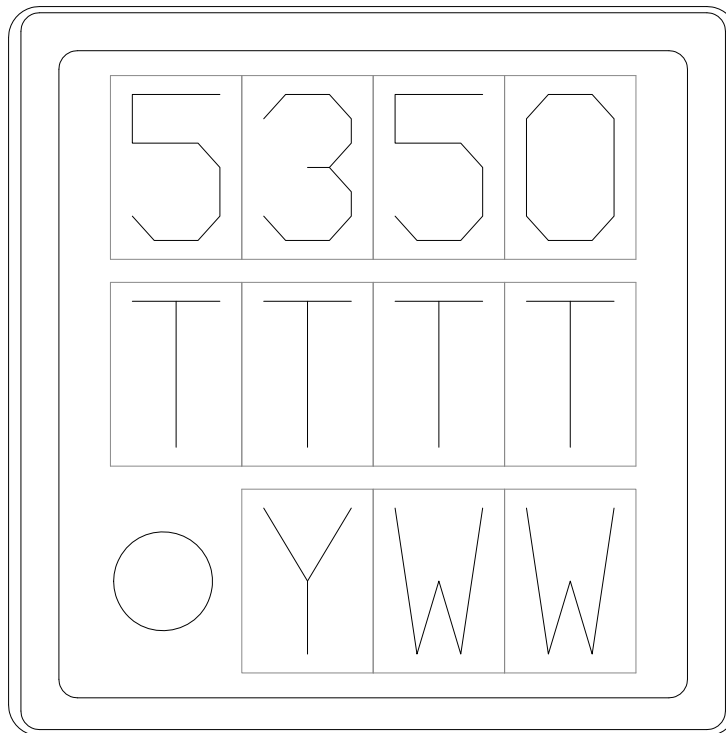


Figure 21. 10-Pin MSOP Top Marking

## 10.4. Top Marking Explanation

<b>Mark Method:</b>	Laser	
<b>Pin 1 Mark:</b>	Mold Dimple (Bottom-Left Corner)	
<b>Font Size:</b>	0.60 mm (24 mils)	
<b>Line 1 Mark Format</b>	Device Part Number	Si5350
<b>Line 2 Mark Format:</b>	TTTT = Mfg Code*	Line 2 from the “Markings” section of the Assembly Purchase Order form.
<b>Line 3 Mark Format:</b>	YWW = Date Code	Assigned by the Assembly House. Y = Last Digit of Current Year (Ex: 2013 = 3) WW = Work Week of Assembly Date.
<p><b>*Note:</b> The code shown in the “TTTT” line does not correspond to the orderable part number or frequency plan. It is used for package assembly quality tracking purposes only.</p>		

## DOCUMENT CHANGE LIST

### Revision 0.75 to Revision 1.0

- Extended frequency range from 8 MHz–160 MHz to 2.5 MHz–200 MHz.
- Updated block diagrams for clarity.
- Added complete Si5350/1 family table, Table 1.
- Added top mark information.
- Added land pattern drawings.
- Added PowerUp Time, PLL Bypass mode, Table 4.
- Clarified Down Spread step sizes in Table 4.
- Updated max jitter specs (typ unchanged) in Table 6.
- Clarified power supply sequencing requirement, Section 4.5.2.



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