



### P-Channel 30-V (D-S) MOSFET

#### CHARACTERISTICS

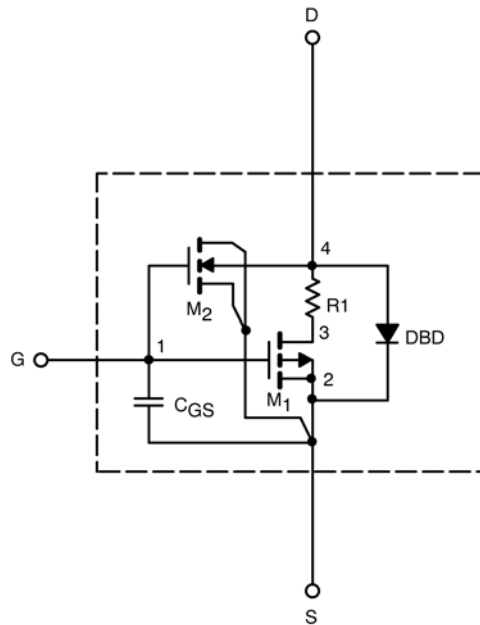
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the  $-55$  to  $125^{\circ}\text{C}$  Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the  $-55$  to  $125^{\circ}\text{C}$  temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

#### SUBCIRCUIT MODEL SCHEMATIC



# SPICE Device Model Si5435BDC

## Vishay Siliconix



SPECIFICATIONS ( $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	2.2		V
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -10\ \text{V}$	109		A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -4.3\ \text{A}$	0.036	0.035	$\Omega$
		$V_{GS} = -4.5\ \text{V}, I_D = -1.3\ \text{A}$	0.067	0.067	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = -15\ \text{V}, I_D = -4.3\ \text{A}$	9	8	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = -1.1\ \text{A}, V_{GS} = 0\ \text{V}$	-0.78	-0.80	V
<b>Dynamic<sup>b</sup></b>					
Total Gate Charge	$Q_g$	$V_{DS} = -15\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -4.3\ \text{A}$	13	16	nC
Gate-Source Charge	$Q_{gs}$		2.7	2.7	
Gate-Drain Charge	$Q_{gd}$		4.1	4.1	

### Notes

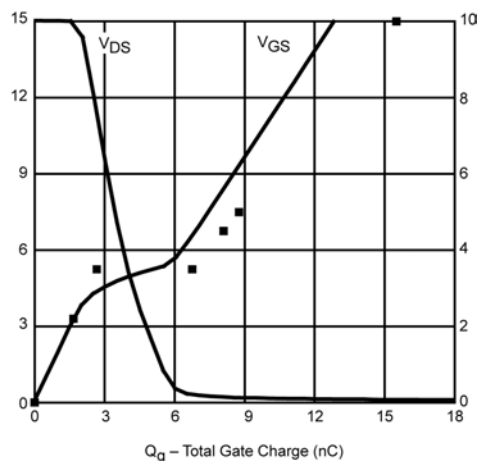
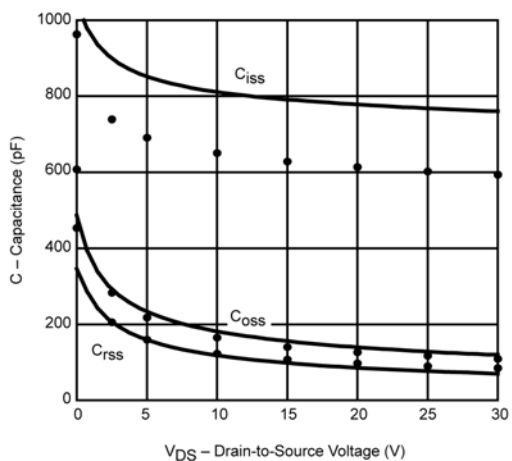
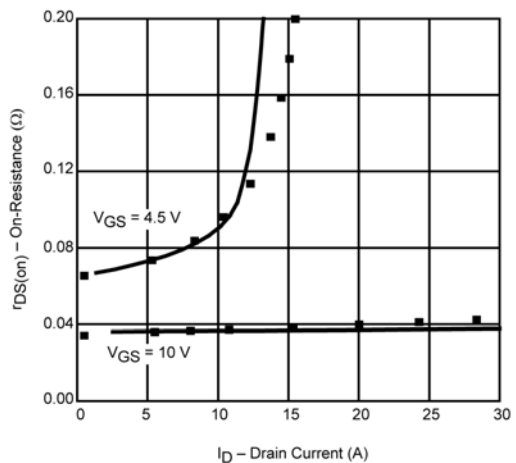
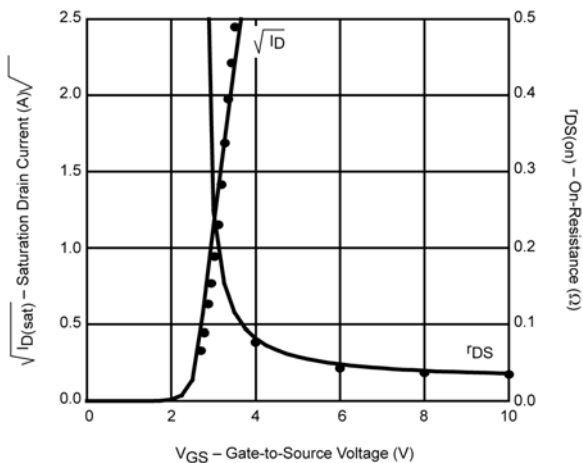
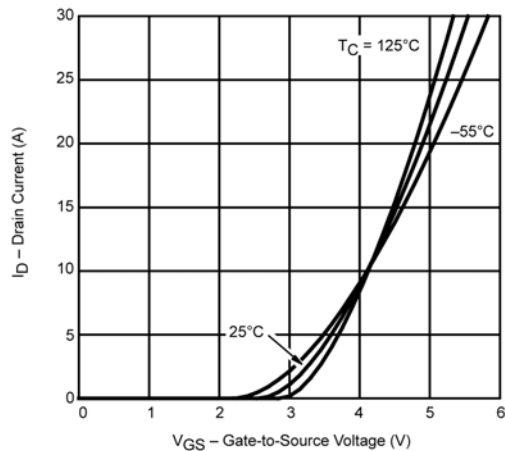
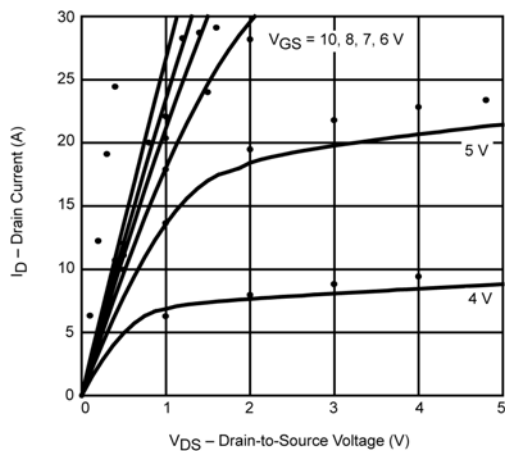
- a. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.



# SPICE Device Model Si5435BDC

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COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$  UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.



### Disclaimer

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