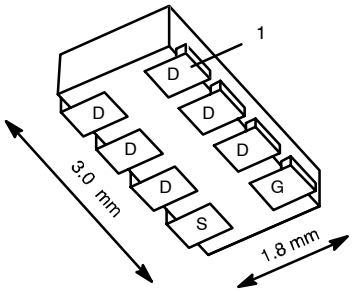
P-Channel 1.8-V (G-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-8	0.035 @ V_{GS} = -4.5 V	±7.1
	0.047 @ V_{GS} = -2.5 V	±6.2
	0.062 @ V_{GS} = -1.8 V	±5.7

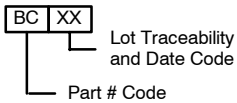
TrenchFET® Power MOSFETs
1.8-V Rated

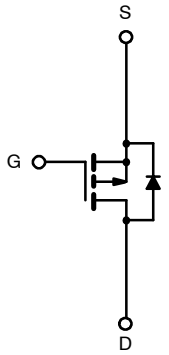
1206-8 ChipFET™



Bottom View

Marking Code





P-Channel MOSFET

Ordering Information: Si5445DC-T1

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**5 secs**	**Steady State**	**Unit**
Drain-Source Voltage		V_{DS}	-8		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±7.1	±5.2	A
	T_A = 85°C		±5.2	±3.7	
Pulsed Drain Current		I_{DM}	±20		
Continuous Source Current[a]		I_S	-2.1	-1.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	1.3	W
	T_A = 85°C		1.3	0.7	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Soldering Recommendations (Peak Temperature)[b, c]			260		

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 5 sec	R_{thJA}	40	50	°C/W
	Steady State		80	95	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	15	20	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
b. See Reliability Manual for profile. The ChipFET is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

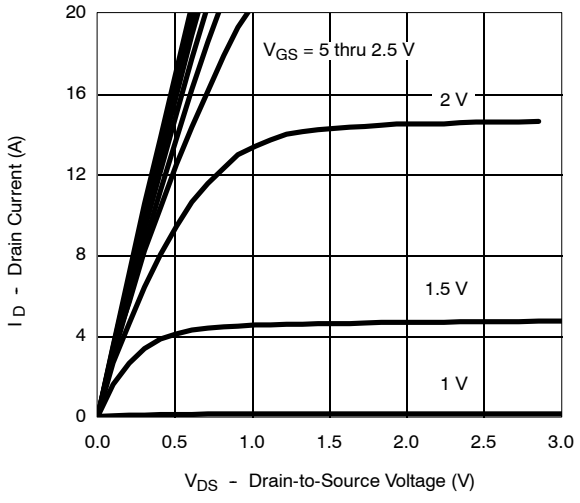
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.45			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −6.4 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −6.4 V, V_{GS} = 0 V, T_J = 85°C			−5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ −5 V, V_{GS} = −4.5 V	−20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = −4.5 V, I_D = −5.2 A		0.030	0.035	Ω
		V_{GS} = −2.5 V, I_D = −4.5 A		0.040	0.047	
		V_{GS} = −1.8 V, I_D = −2 A		0.052	0.062	
Forward Transconductance[a]	g_{fs}	V_{DS} = −5 V, I_D = −5.2 A		18		S
Diode Forward Voltage[a]	V_{SD}	I_S = −1.1 A, V_{GS} = 0 V		−0.8	−1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = −4 V, V_{GS} = −4.5 V, I_D = −5.2 A		17	26	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			2.6		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = −4 V, R_L = 4 Ω I_D ≅ −1 A, V_{GEN} = −4.5 V, R_G = 6 Ω		15	25	ns
Rise Time	t_r			45	70	
Turn-Off Delay Time	$t_{d(off)}$			110	165	
Fall Time	t_f			65	100	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = −1.1 A, di/dt = 100 A/μs		30	60	

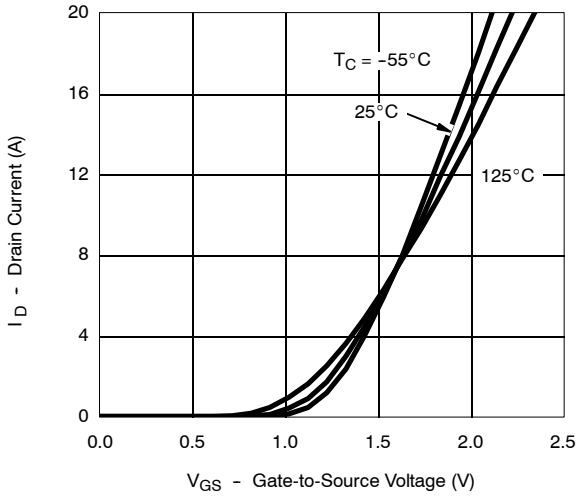
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics



Transfer Characteristics



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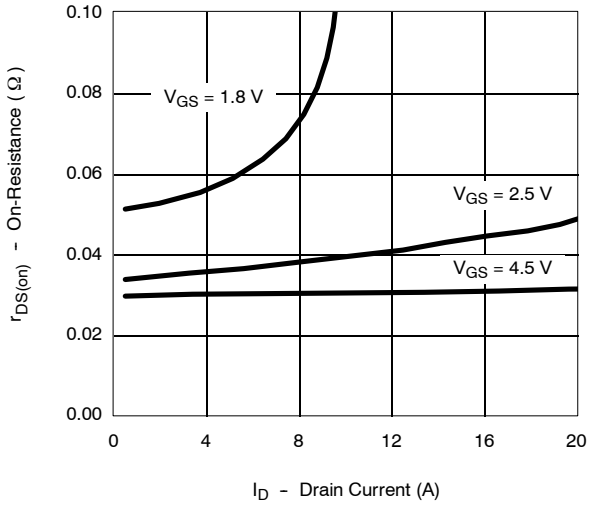
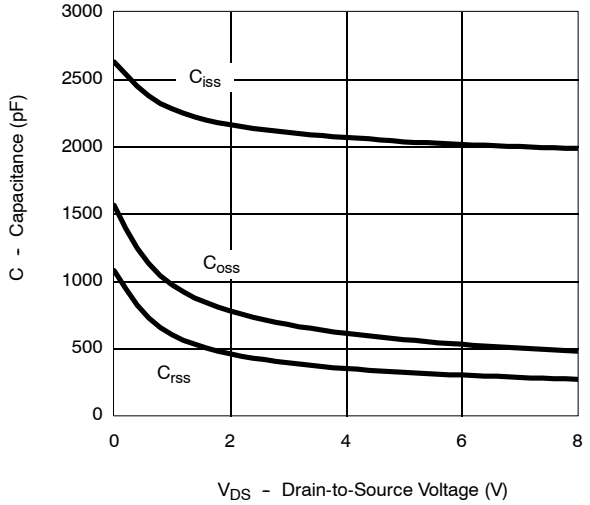
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

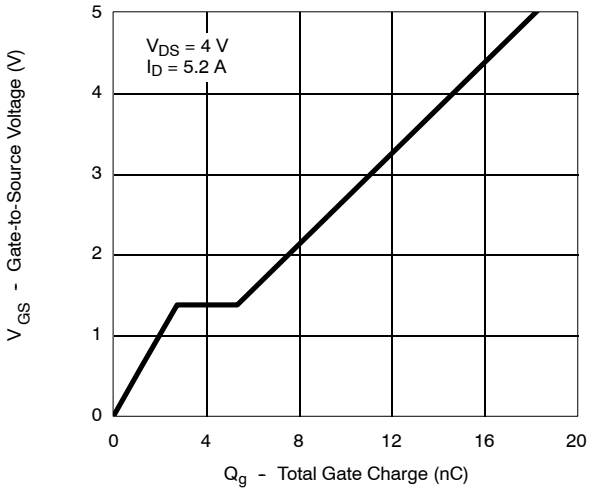
On-Resistance vs. Drain Current



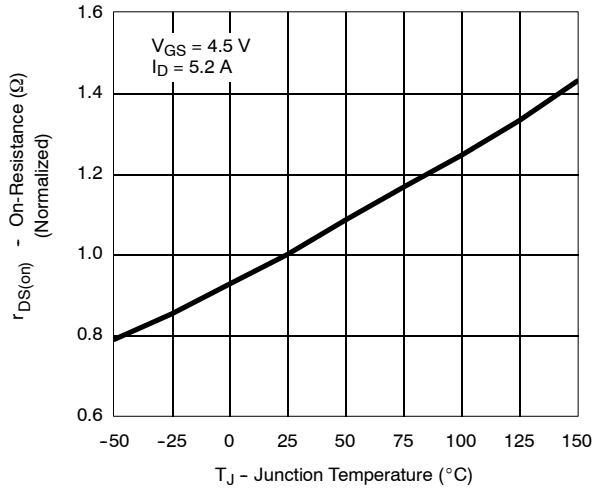
Capacitance



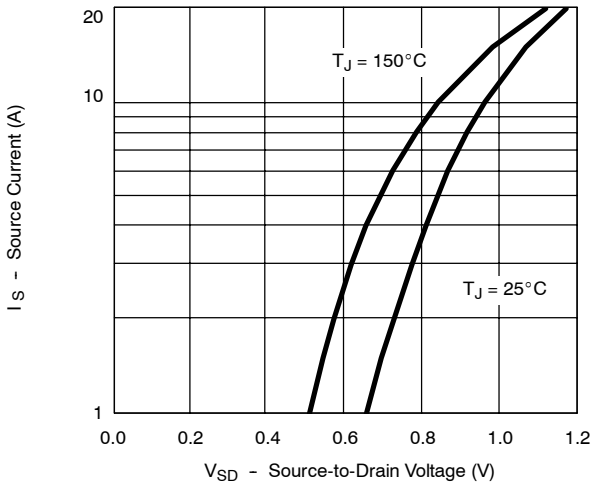
Gate Charge



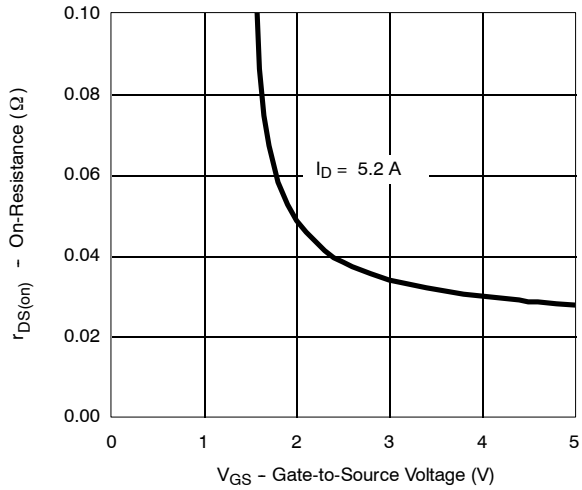
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

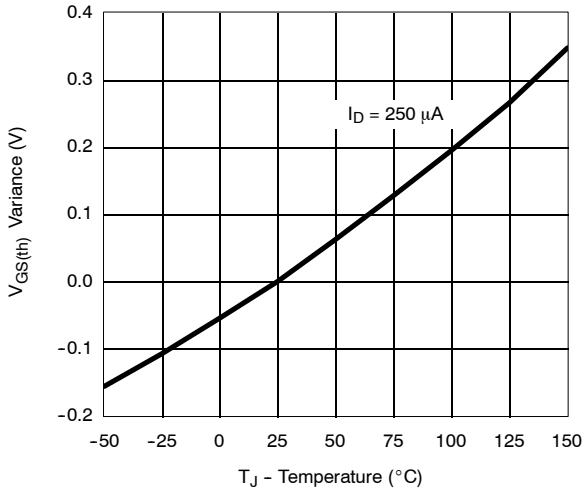


On-Resistance vs. Gate-to-Source Voltage

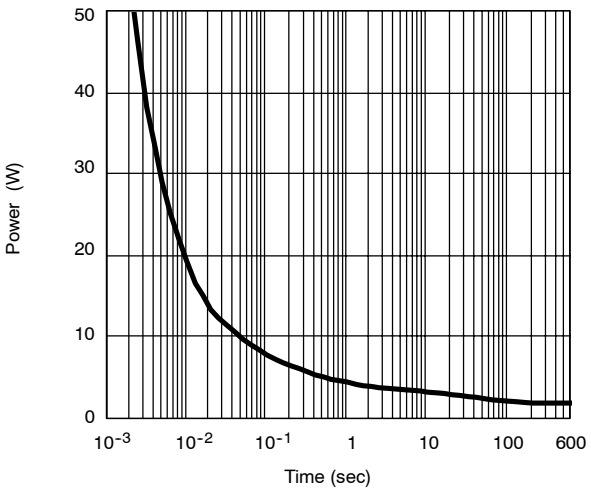


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

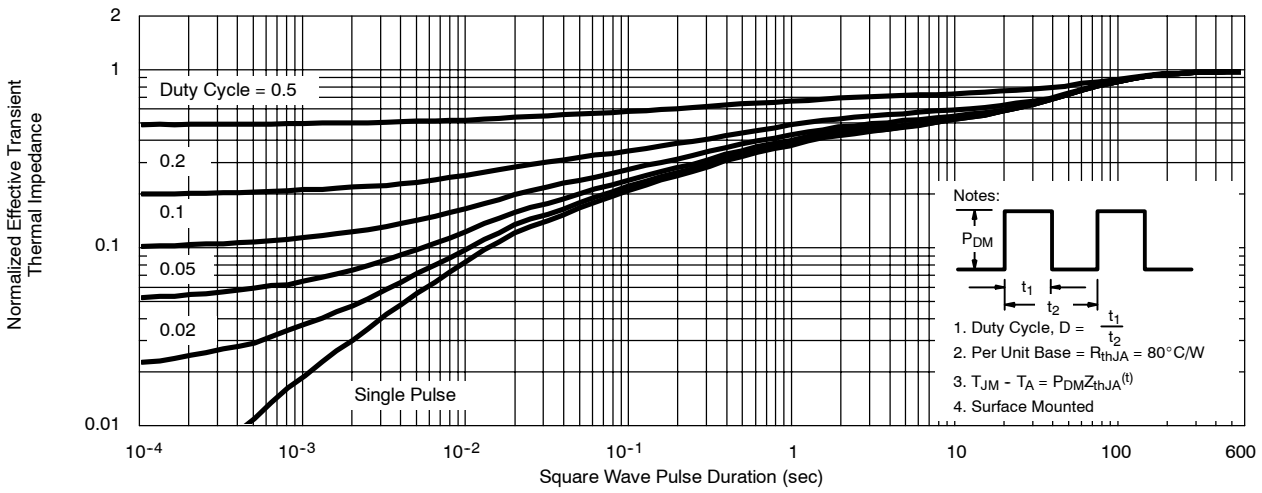
Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot