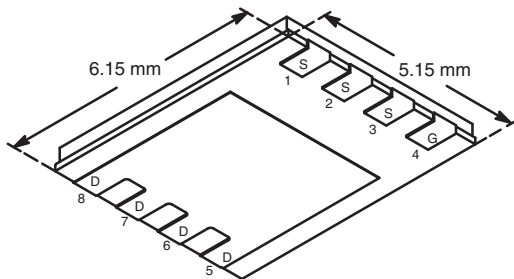


N-Channel Reduced Q_g , Fast Switching MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
30	0.0075 at $V_{GS} = 10$ V	30	12
	0.0115 at $V_{GS} = 4.5$ V	30	

PowerPAK SO-8



Bottom View

Ordering Information: Si7392ADP-T1-E3 (Lead (Pb)-free)
Si7392ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

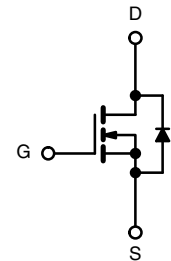
- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Low Switching Losses
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07 mm Profile
- 100 % R_g Tested
- Complaint to RoHS Directive 2002/95/EC

APPLICATIONS

- High-Side DC/DC Conversion
 - Notebook
 - Server



RoHS
COMPLIANT
HALOGEN
FREE
Available



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150$ °C) ^a	I_D	$T_C = 25$ °C	A
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Pulsed Drain Current	I_{DM}	50	A
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	
		$T_A = 25$ °C	
Avalanche Current	I_{AS}	25	mJ
Single Pulse Avalanche Energy	E_{AS}	30	
Maximum Power Dissipation ^a	P_D	$T_C = 25$ °C	W
		$T_C = 70$ °C	
		$T_A = 25$ °C	
		$T_A = 70$ °C	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	20	25	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	3.5	4.5	

Notes:

- Based on $T_C = 25$ °C.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- See solder profile (www.vishay.com/ppg?73461). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 70 °C/W.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 1 mA	30			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 1 μA to 250 μA		30		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 6		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.0		2.5	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C			10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	30			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 12.5 A		0.006	0.0075	Ω
		V _{GS} = 4.5 V, I _D = 10 A		0.009	0.0115	
Forward Transconductance	g _{fs}	V _{DS} = 15 V, I _D = 12.5 A		46		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		1465		pF
Output Capacitance	C _{oss}			360		
Reverse Transfer Capacitance	C _{rss}			150		
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 12.5 A		25	38	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 12.5 A		12	18	
Gate-Source Charge	Q _{gs}			3.7		
Gate-Drain Charge	Q _{gd}			3.1		
Gate Resistance	R _g	f = 1 MHz		1.9	2.9	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 4.5 V, R _g = 1 Ω		16	25	ns
Rise Time	t _r			50	75	
Turn-Off DelayTime	t _{d(off)}			21	32	
Fall Time	t _f			8	15	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 3 Ω I _D ≅ 5 A, V _{GEN} = 10 V, R _g = 1 Ω		8	15	
Rise Time	t _r			35	55	
Turn-Off DelayTime	t _{d(off)}			23	35	
Fall Time	t _f			8	15	
Drain-Source Body Diode Characteristics						
Continous Source-Drain Diode Current	I _S	T _C = 25 °C			30	A
Pulse Diode Forward Current ^a	I _{SM}				50	
Body Diode Voltage	V _{SD}	I _S = 2.7 A		0.73	1.1	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = 10 A, dI/dt = 100 A/μs, T _J = 25 °C		26	40	nC
Body Diode Reverse Recovery Charge	Q _{rr}			19	30	ns
Reverse Recovery Fall Time	t _a			13		
Reverse Recovery Rise Time	t _b			13		

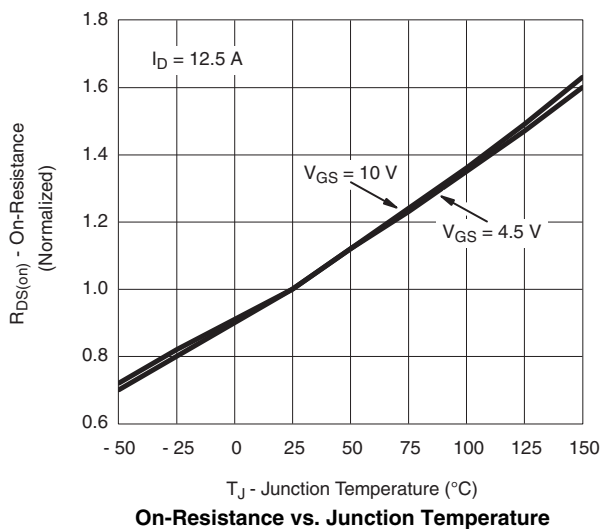
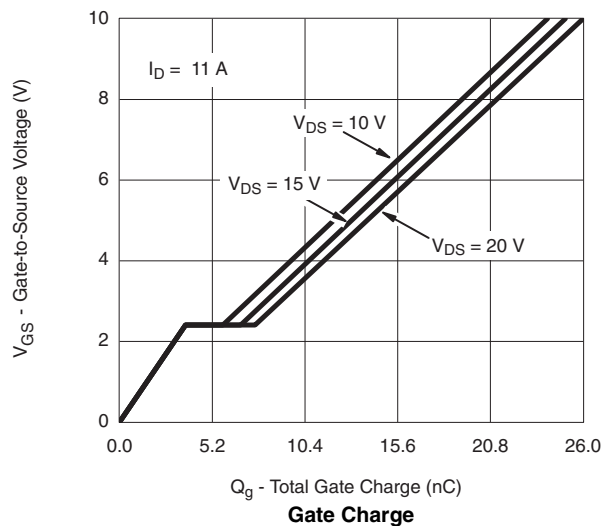
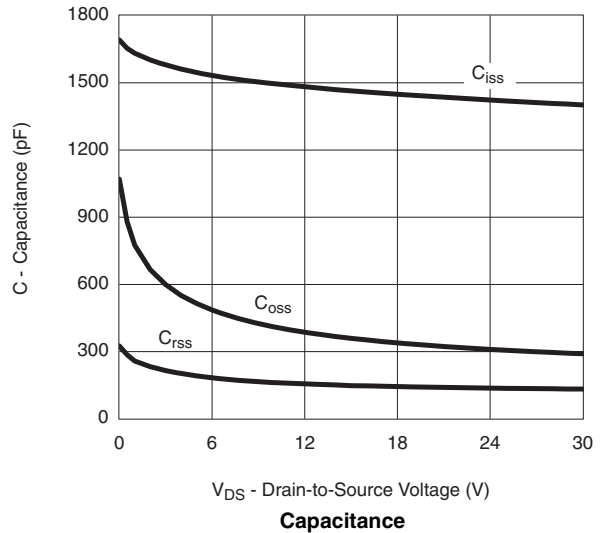
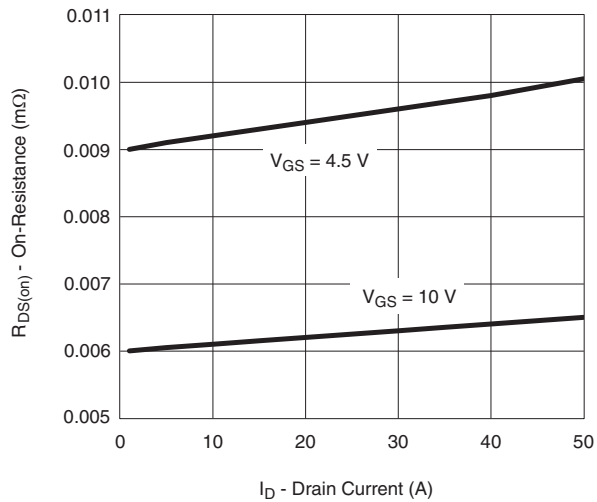
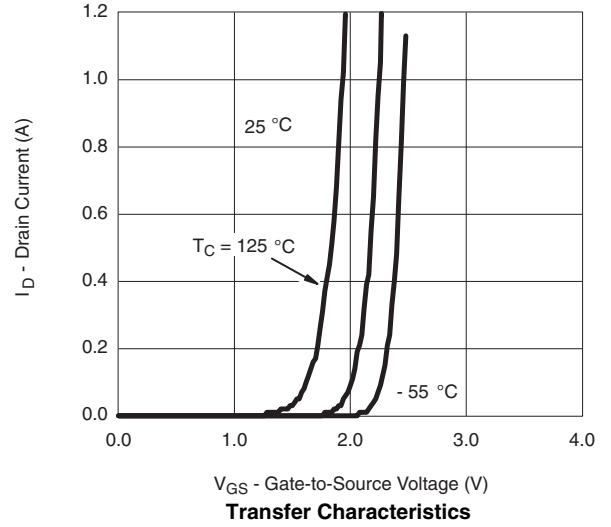
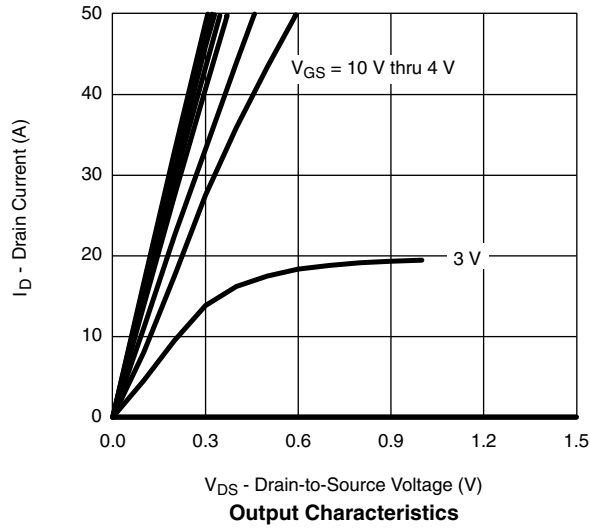
Notes:

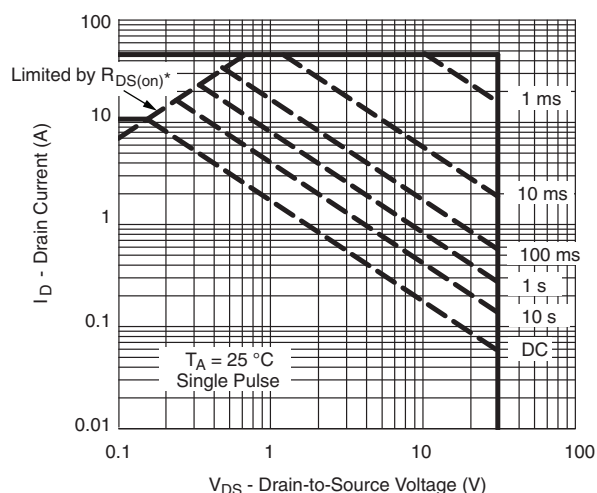
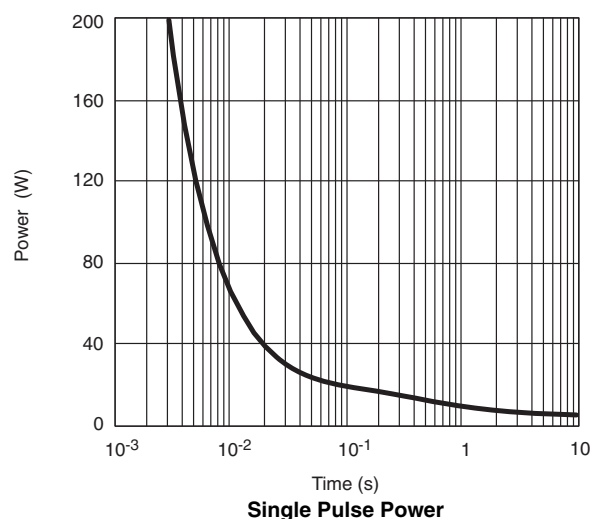
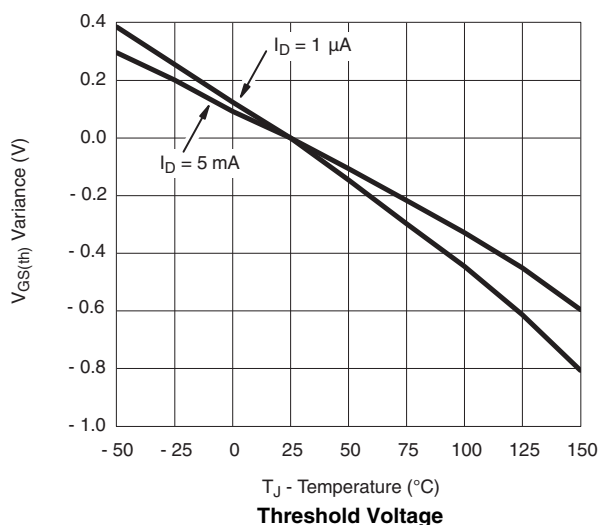
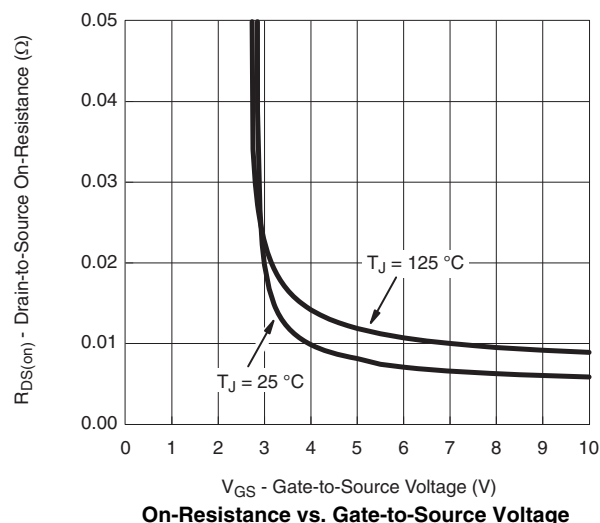
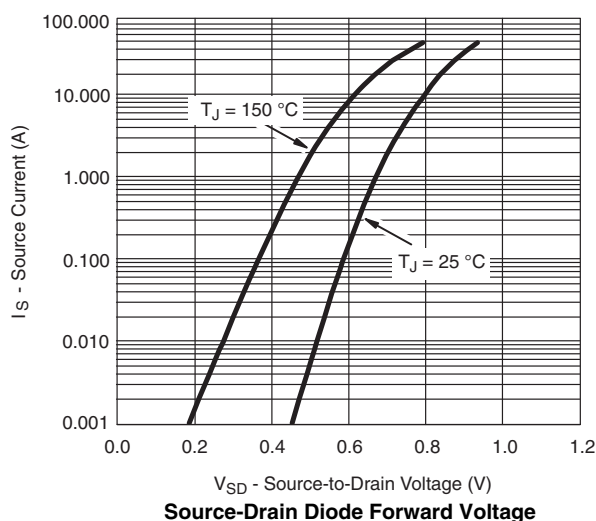
a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted)

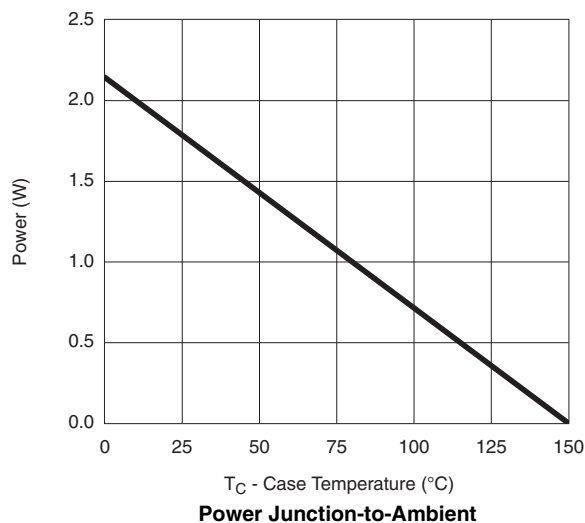
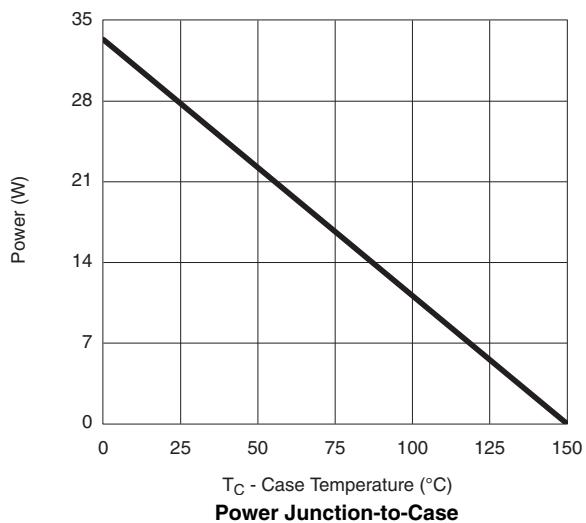
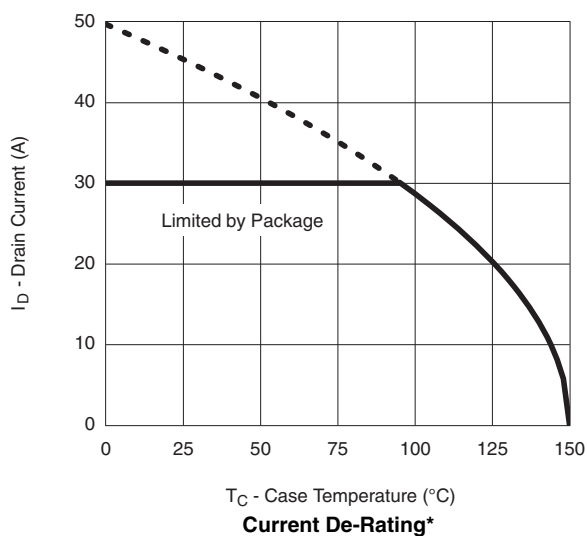


TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

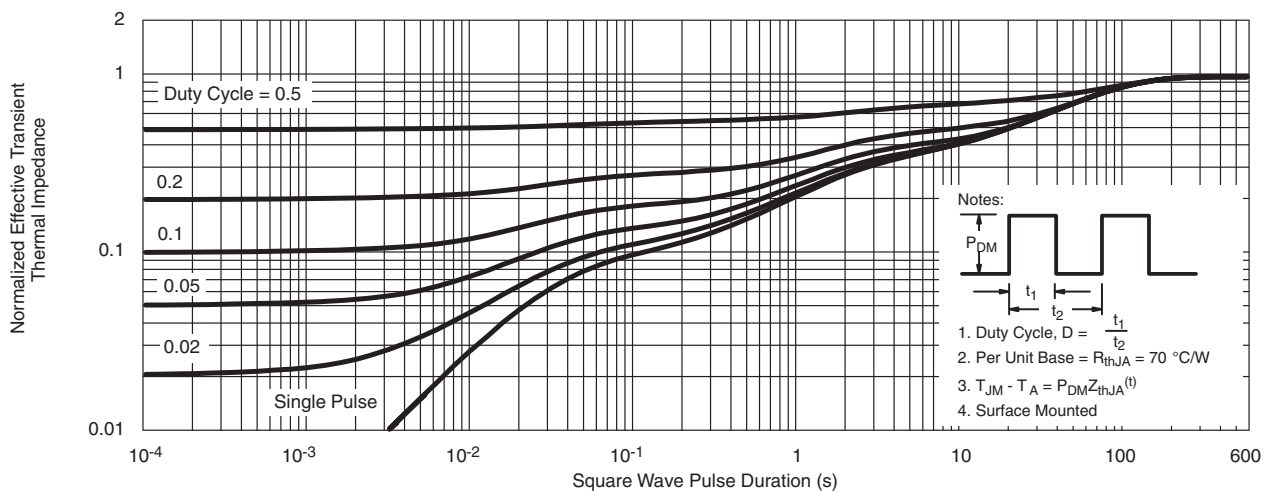
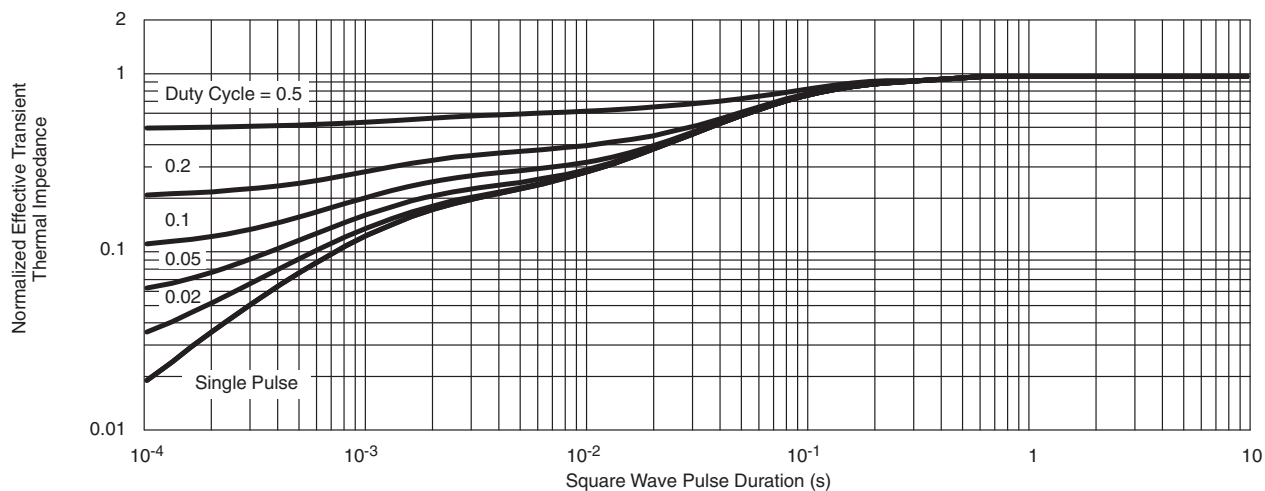
* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)



* The power dissipation PD is based on $T_{J(max)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Foot

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