

SPICE Device Model Si7452DP Vishay Siliconix

N-Channel 60-V (D-S) Fast Switching MOSFET

CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS

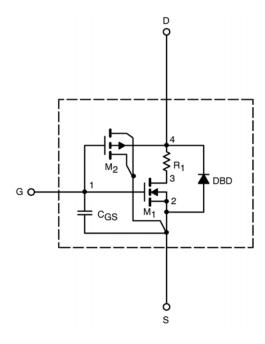
- · Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125° C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{\rm gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Condition	Simulated Data	Measured Data	Unit
Static			_ -		•
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3.7		V
On-State Drain Current ^a	I _{D(on)}	$V_{DS}~\geq 5~V,~V_{GS}$ = 10 V	651		Α
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 19.3 A	0.0063	0.007	Ω
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 19.3 A	57	51	S
Forward Voltage ^a	V_{SD}	$I_S = 4.5 \text{ A}, V_{GS} = 0 \text{ V}$	0.84	0.80	V
Dynamic ^b			- -		-
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_{D} = 19.3 A	112	105	nC
Gate-Source Charge	Q_{gs}		40	40	
Gate-Drain Charge	Q_gd		21	21	
Turn-On Delay Time	t _{d(on)}	$V_{DD} = 30 \text{ V}, \text{ R}_{L} = 30 \Omega$ $I_{D} \cong \text{ 1 A, V}_{GEN} = 10 \text{ V}, \text{ R}_{G} = 6 \Omega$	65	45	ns ns
Rise Time	t _r		19	15	
Turn-Off Delay Time	$t_{\text{d(off)}}$		82	90	
Fall Time	t _f		26	40	

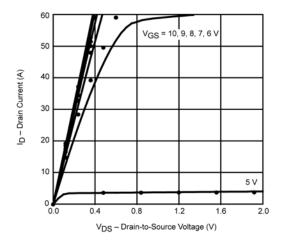
Notes

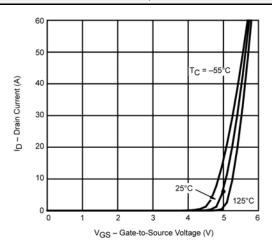
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2%. b. Guaranteed by design, not subject to production testing.

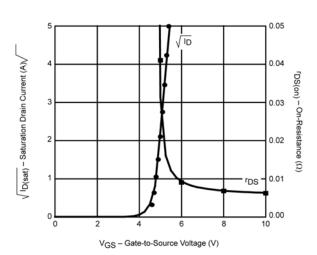


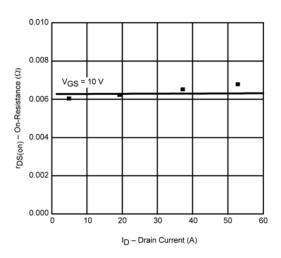
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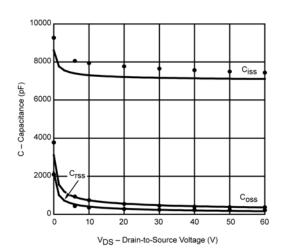
COMPARISON OF MODEL WITH MEASURED DATA (TJ=25°C UNLESS OTHERWISE NOTED)

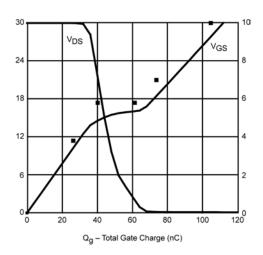












Note: Dots and squares represent measured data.