

P-Channel 40-V (D-S) MOSFET

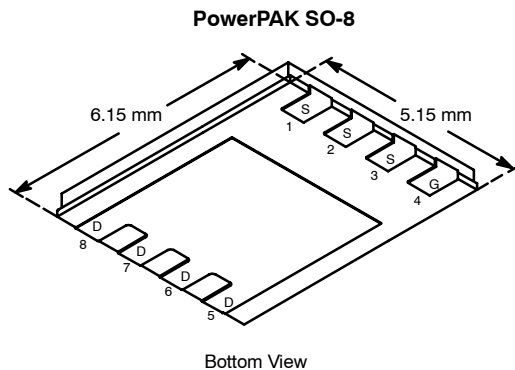
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-40	0.0092 @ $V_{GS} = -10$ V	-18.6
	0.014 @ $V_{GS} = -4.5$ V	-15

FEATURES

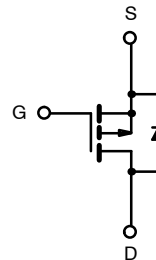
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

APPLICATIONS

- Automotive
 - 12-V Boardnet
 - High-Side Switches
 - Motor Drives



Ordering Information: Si7463DP-T1—E3



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	V_{DS}	-40		V	
Gate-Source Voltage	V_{GS}	± 20			
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	-18.6	-11	A
		$T_A = 70^\circ\text{C}$	-15	-8.9	
Pulsed Drain Current	I_{DM}	-60			
continuous Source Current (Diode Conduction) ^a	I_S	-4.5	-1.6		
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	5.4	1.9	W
		$T_A = 70^\circ\text{C}$	3.4	1.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	18	23	$^\circ\text{C}/\text{W}$
		Steady State	52	65	
Maximum Junction-to-Case (Drain)	R_{thJC}	1.0	1.3		

Notes

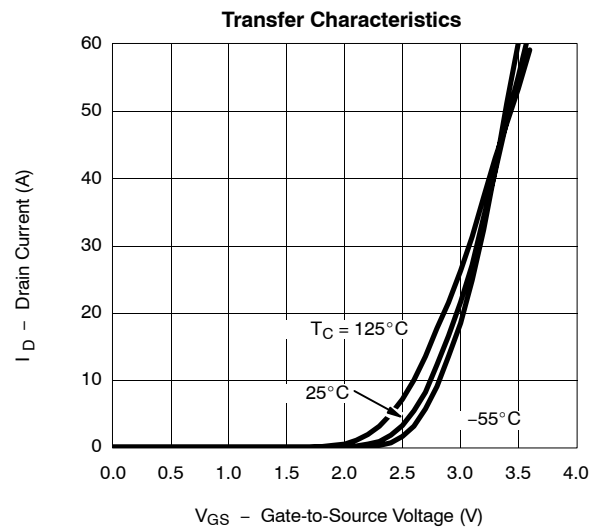
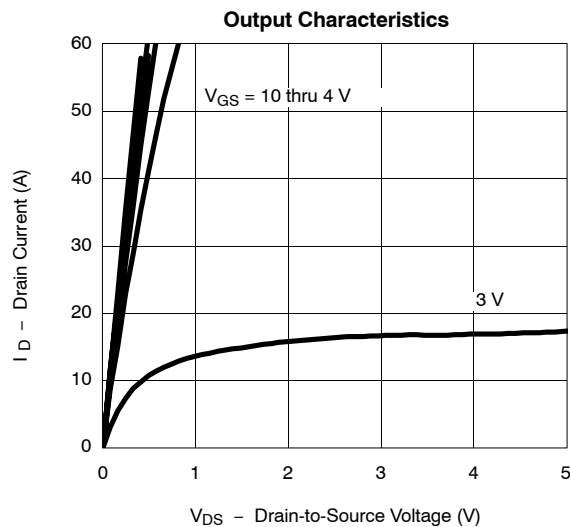
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1		-3	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -40 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -40 V, V _{GS} = 0 V, T _J = 70 °C			-10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-40			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = -10 V, I _D = -18.6 A		0.0075	0.0092	Ω
		V _{GS} = -4.5 V, I _D = -15 A		0.011	0.014	
Forward Transconductance ^a	g _{fs}	V _{DS} = -15 V, I _D = -18.6 A		50		S
Diode Forward Voltage ^a	V _{SD}	I _S = -4.5 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -20 V, V _{GS} = -10 V, I _D = -18.6 A		121	140	nC
Gate-Source Charge	Q _{gs}			19.2		
Gate-Drain Charge	Q _{gd}			30.3		
Gate-Resistance	R _g			2.7		Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = -20 V, R _L = 20 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		20	30	ns
Rise Time	t _r			25	40	
Turn-Off Delay Time	t _{d(off)}			200	300	
Fall Time	t _f			100	150	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = -4.5 A, di/dt = 100 A/μs		45	70	

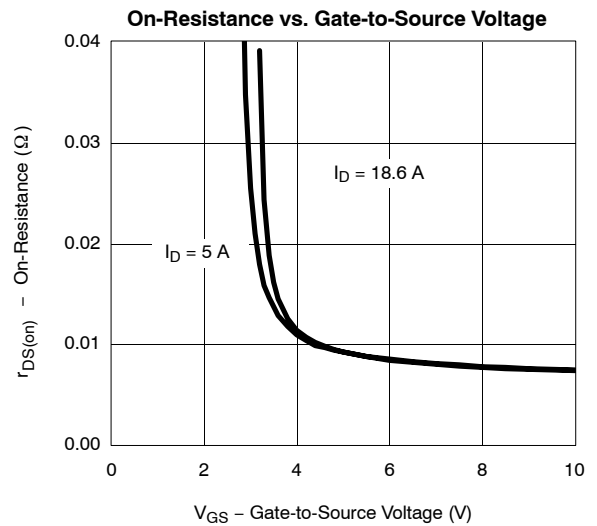
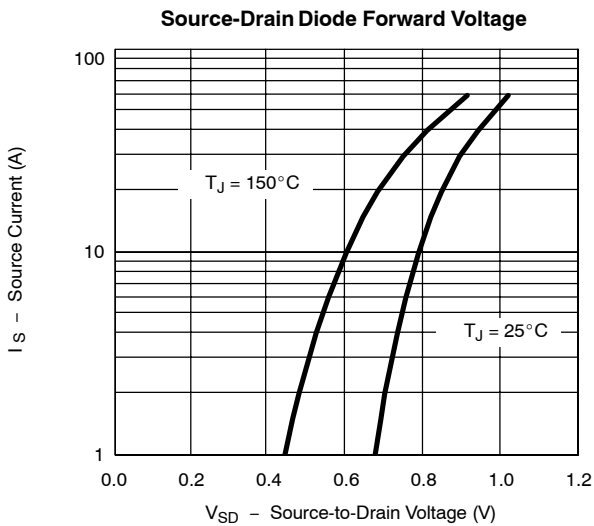
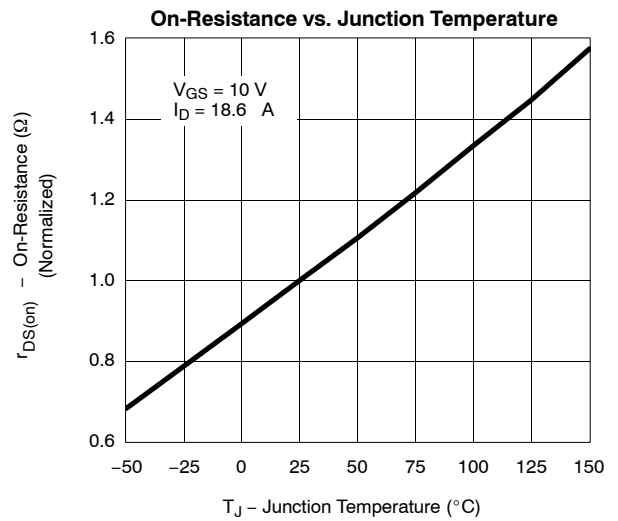
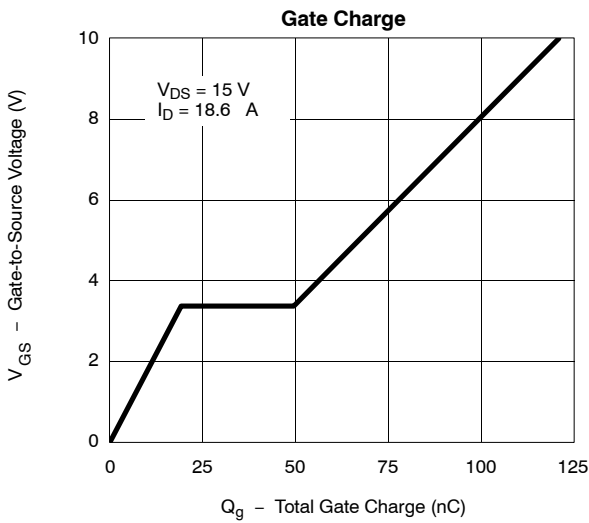
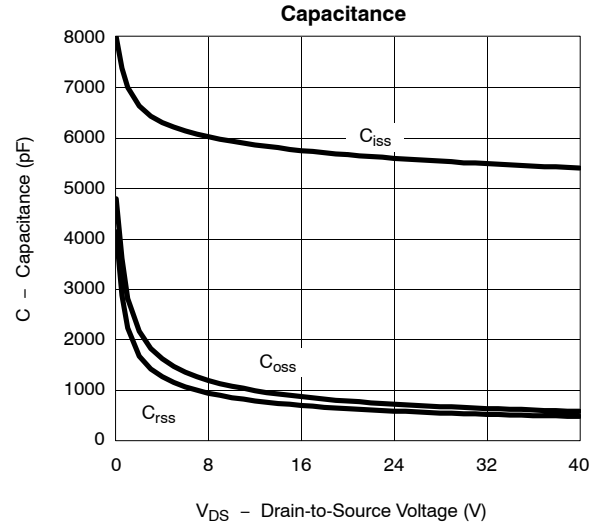
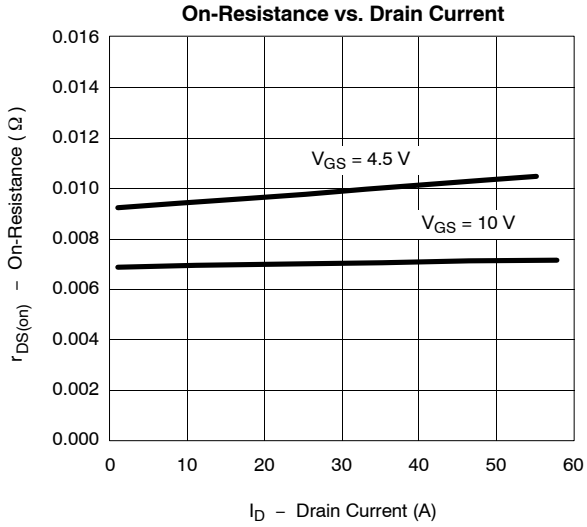
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

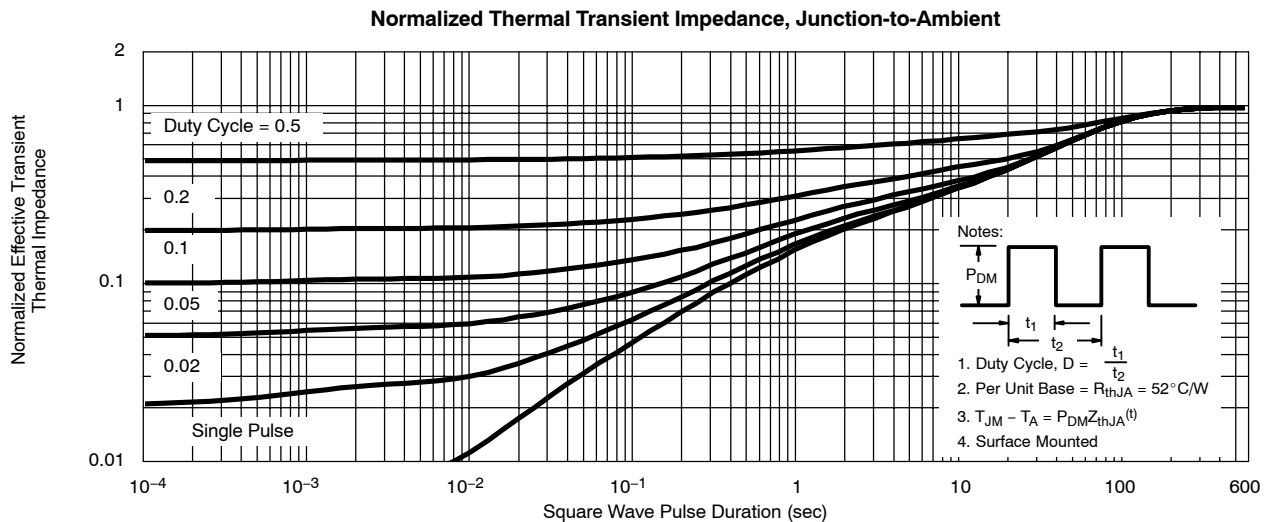
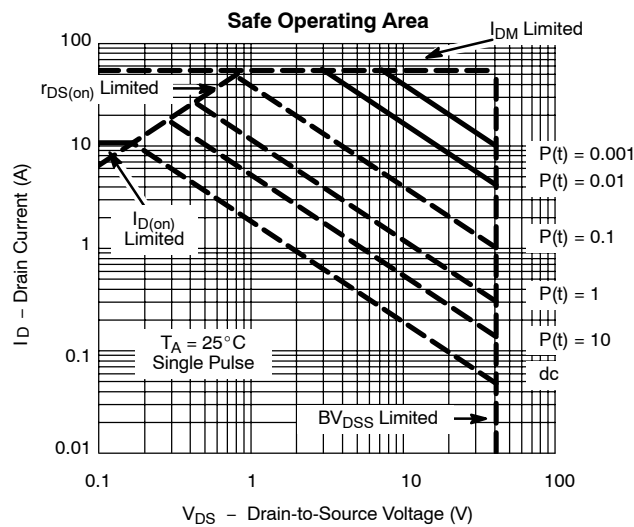
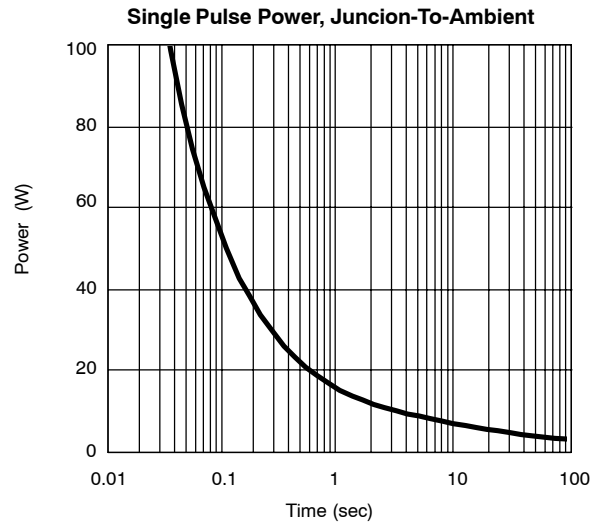
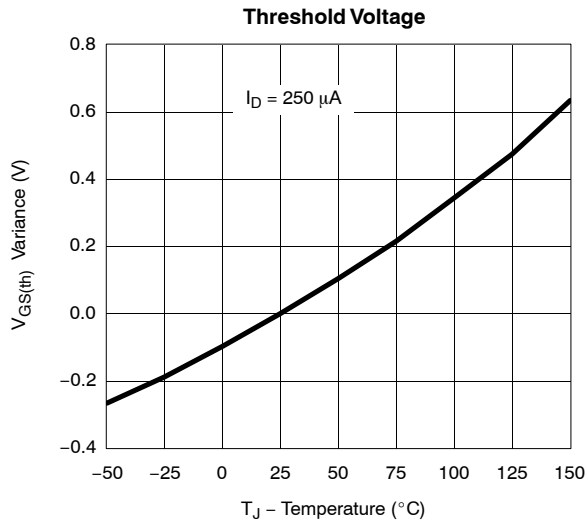
TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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