

N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

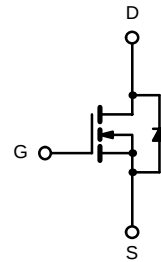
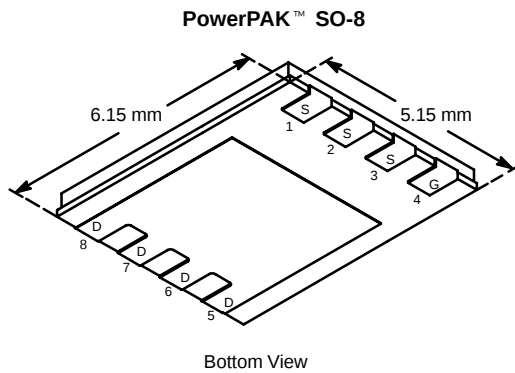
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.003 @ $V_{GS} = 10$ V	29
	0.00425 @ $V_{GS} = 4.5$ V	25

FEATURES

- TrenchFET® Power MOSFET
- PWM Optimized
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile

APPLICATIONS

- DC/DC Converters
 - Low-Side MOSFET in Synchronous Buck in Desktops
- Secondary Synchronous Rectifier



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25 °C	I _D	29	18	A
	T _A = 70 °C		25	14	
Pulsed Drain Current (10 μs Pulse Width)		I _{DM}	60		
Avalanche Current	L = 0.1 mH	I _{AS}	50		
Continuous Source Current (Diode Conduction) ^a		I _S	4.5	1.6	
Maximum Power Dissipation ^a	T _A = 25 °C	P _D	5.4	1.9	W
	T _A = 70 °C		3.4	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	18	23	$^\circ\text{C/W}$
	Steady State		50	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.5	

Notes

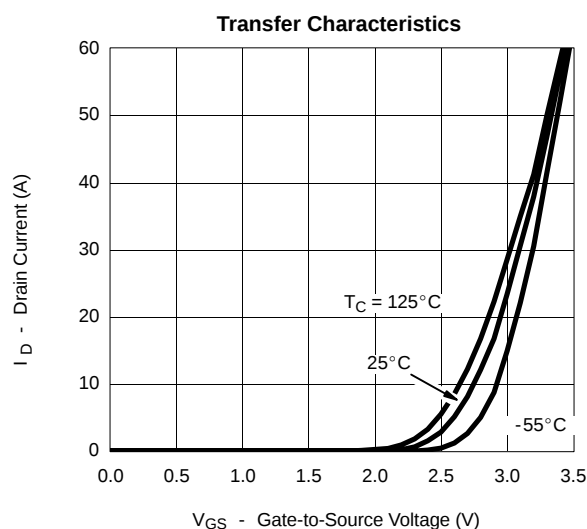
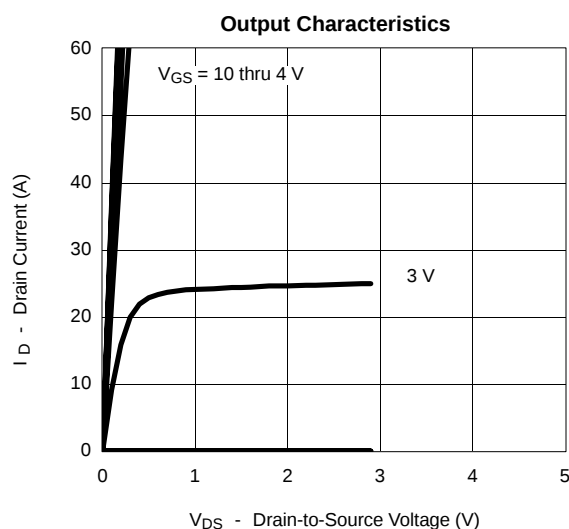
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

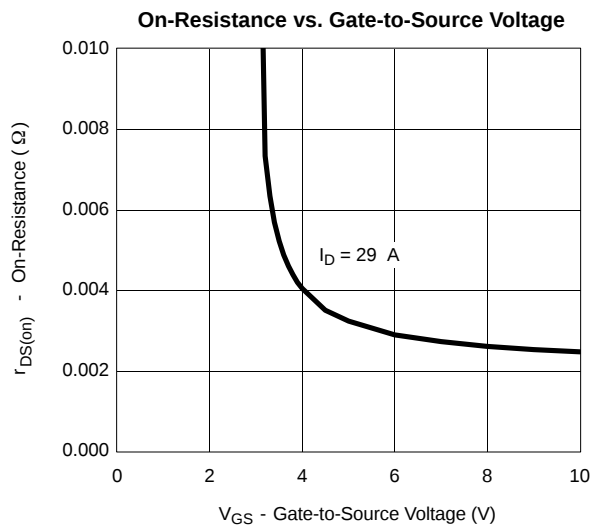
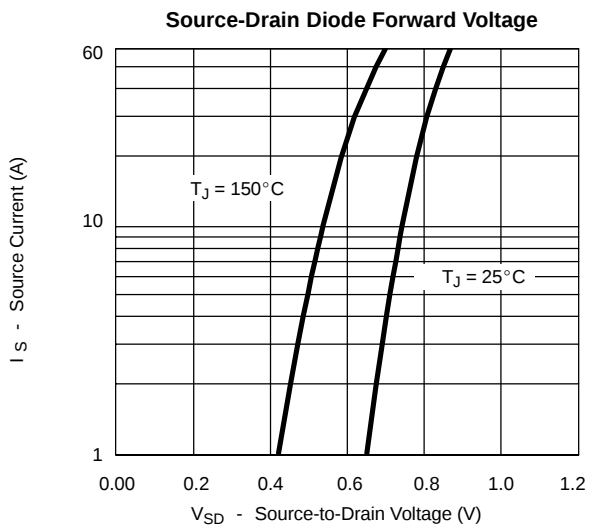
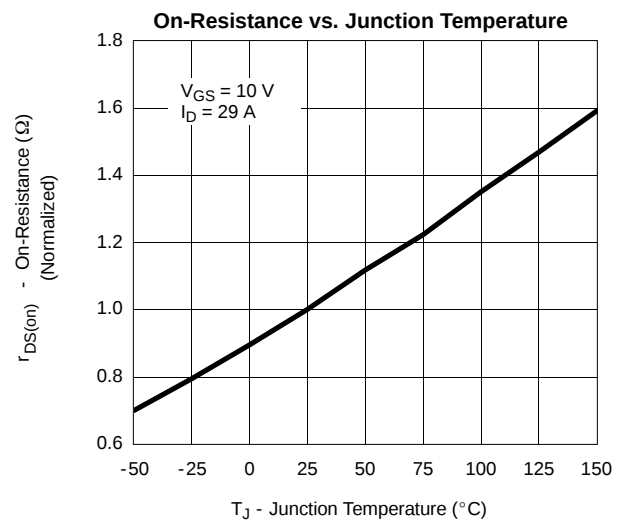
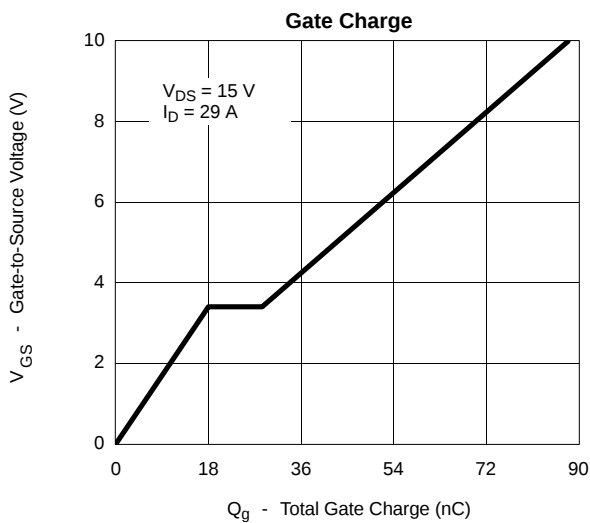
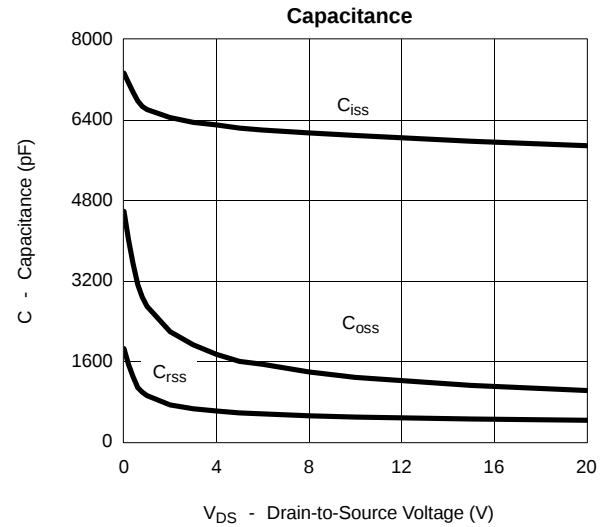
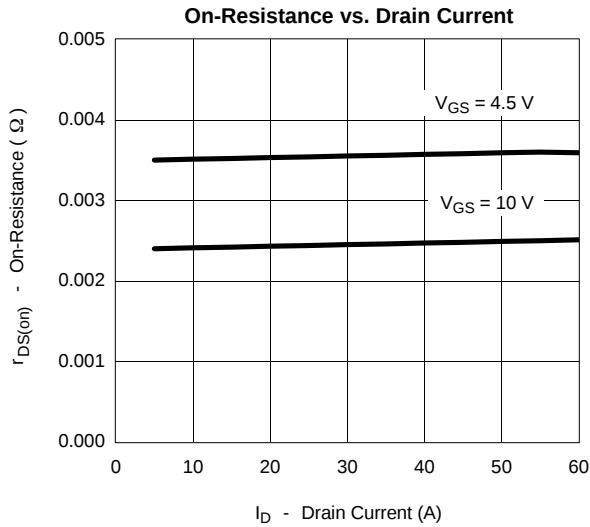
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0		3.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 29\ \text{A}$		0.0025	0.0030	Ω
		$V_{GS} = 4.5\ \text{V}, I_D = 25\ \text{A}$		0.0035	0.00425	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 6\ \text{V}, I_D = 29\ \text{A}$		90		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 4.5\ \text{A}, V_{GS} = 0\ \text{V}$		0.68	1.1	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}, V_{GS} = 4.5\ \text{V}, I_D = 29\ \text{A}$		40.5	60	nC
Gate-Source Charge	Q_{gs}			18		
Gate-Drain Charge	Q_{gd}			10.5		
Gate Resistance	R_g			1.2		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		30	50	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			110	200	
Fall Time	t_f			35	60	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		55	80	

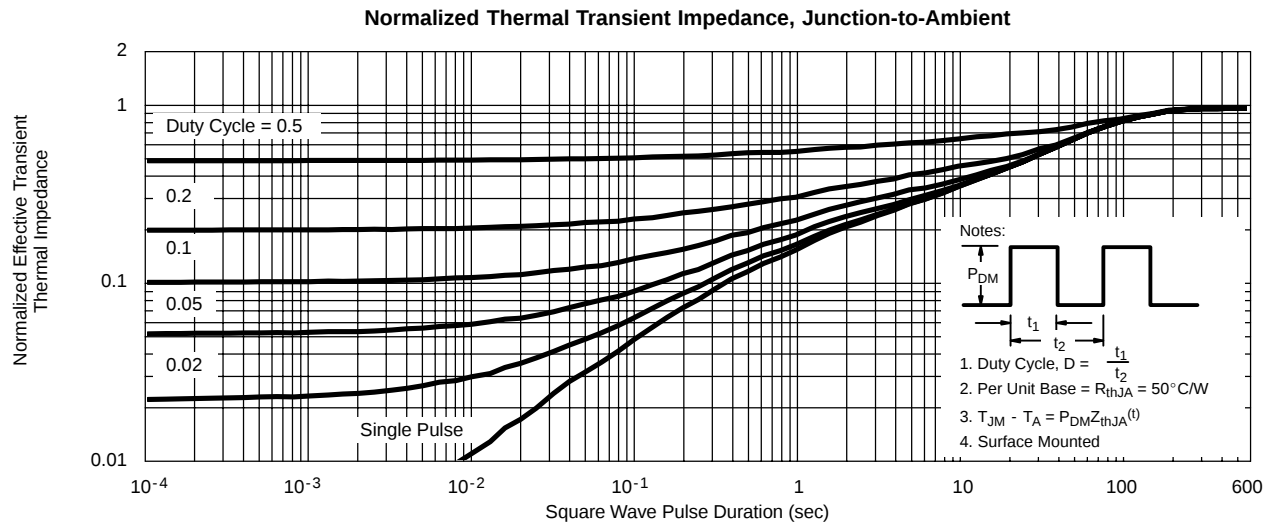
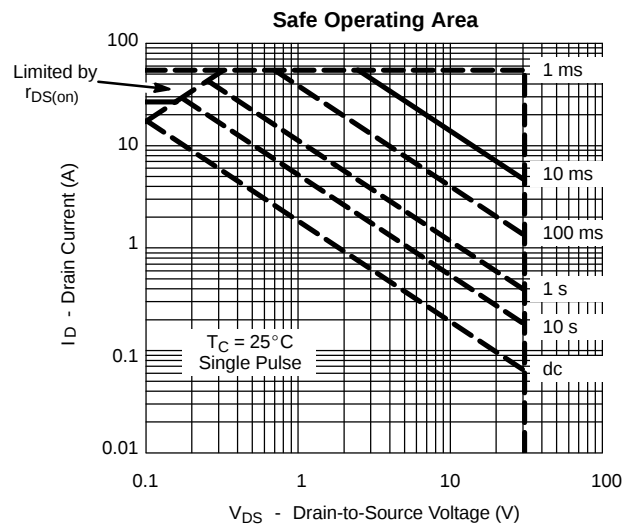
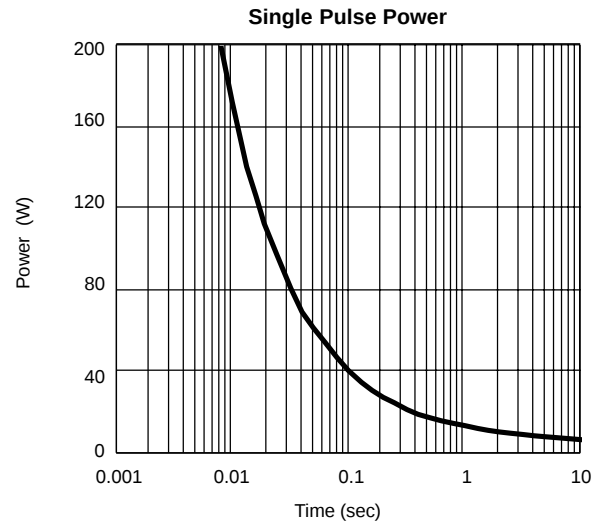
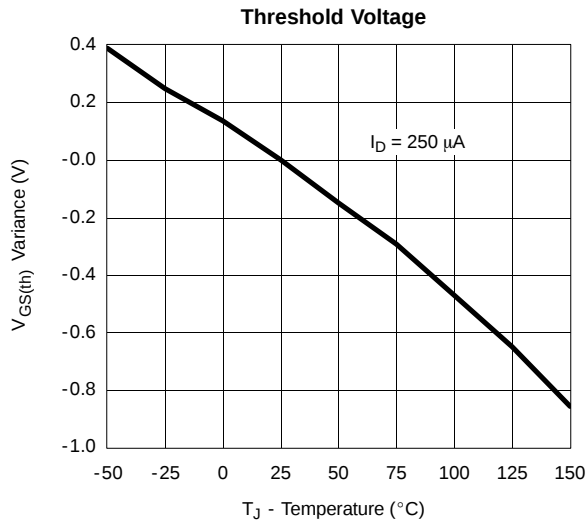
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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