Dual N-Channel 30-V (D-S) MOSFET, Common Drain

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.028 @ V_{GS} = 4.5 V	8.3
	0.030 @ V_{GS} = 3.7 V	8.0
	0.043 @ V_{GS} = 2.5 V	6.7

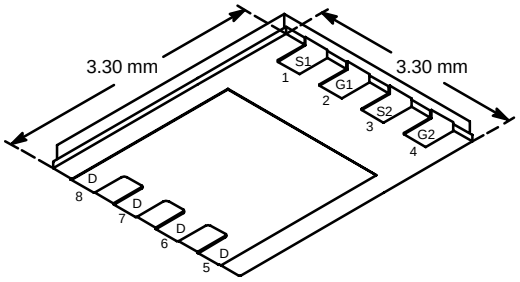
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK™ Package with Low 1.07-mm Profile
- 3000-V ESD Protection

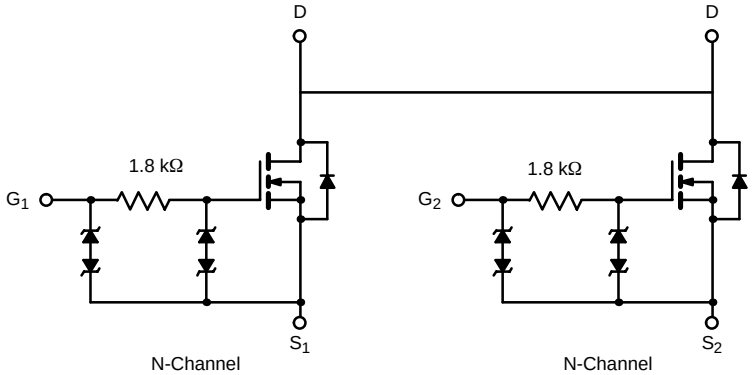
APPLICATIONS

- Protection Switch for 1-2 Li-ion/LiP Batteries

PowerPAK™ 1212-8



Bottom View



N-Channel N-Channel

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	8.3	5.6	A
	T_A = 85°C		6.0	4.0	
Pulsed Drain Current		I_{DM}	40		
Continuous Source Current (Diode Conduction)[a]		I_S	2.7	1.3	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.2	1.5	W
	T_A = 85°C		1.7	0.79	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	30	38	°C/W
	Steady State		65	82	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.
This data sheet contains preliminary specifications that are subject to change.

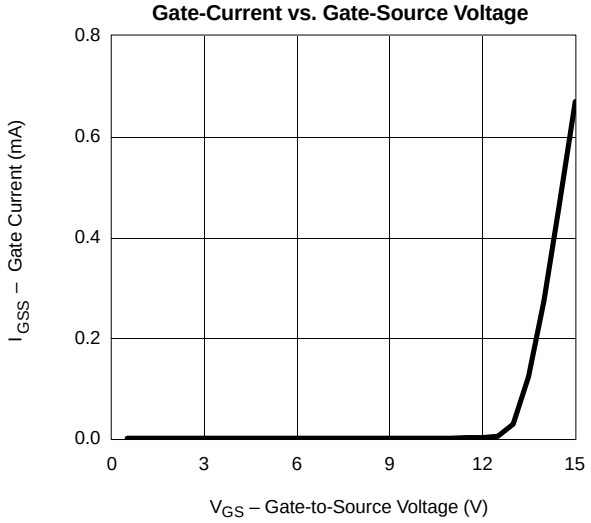
MOSFET SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	0.60			V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V			±1	μA
		V_{DS} = 0 V, V_{GS} = ±12 V			±10	mA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			1	μA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 85°C			20	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 4.5 V	30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 4.5 V, I_D = 8.3 A		0.023	0.028	Ω
		V_{GS} = 3.7 V, I_D = 8.0 A		0.025	0.030	
		V_{GS} = 2.5 V, I_D = 3.0 A		0.035	0.043	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 8.3 A		26		S
Diode Forward Voltage[a]	V_{SD}	I_S = 2.7 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 8.3 A		10	15	nC
Gate-Source Charge	Q_{gs}			2.3		
Gate-Drain Charge	Q_{gd}			2.4		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 15 V, R_L = 15 Ω I_D ≅ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		0.9	1.5	μs
Rise Time	t_r			1.5	2.5	
Turn-Off Delay Time	$t_{d(off)}$			2.5	4.0	
Fall Time	t_f			2.5	4.0	

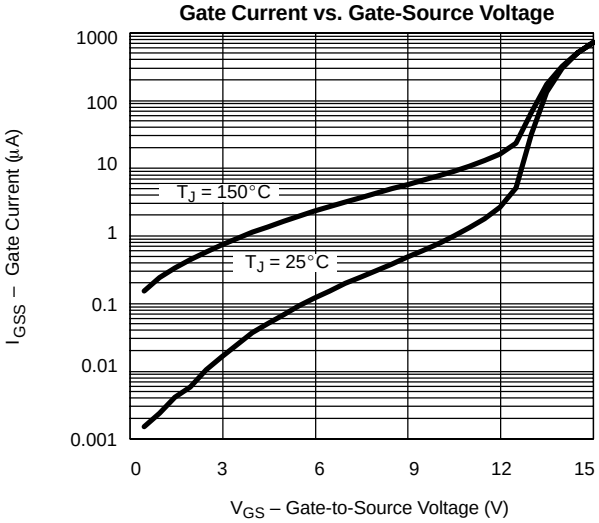
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Gate-Current vs. Gate-Source Voltage

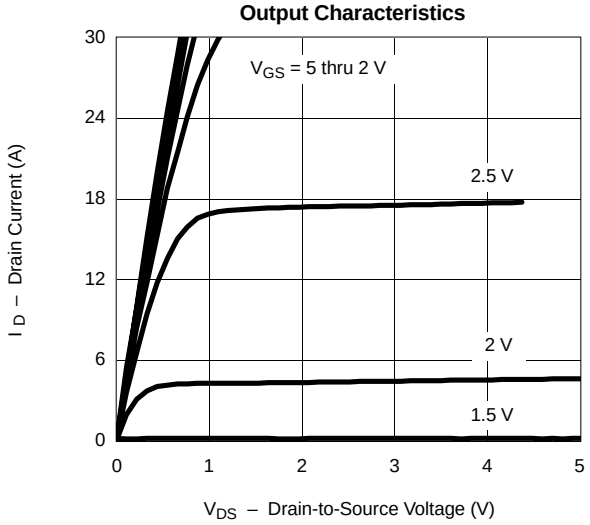


Gate Current vs. Gate-Source Voltage

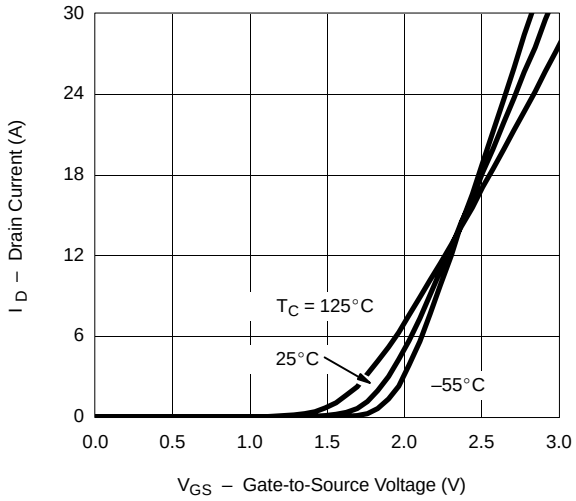


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

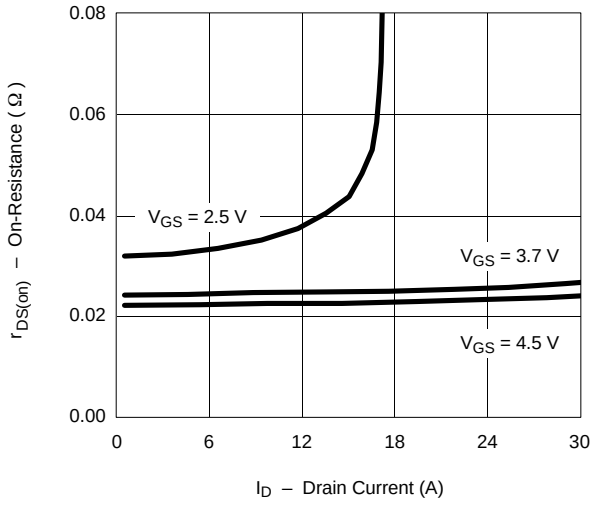
Output Characteristics



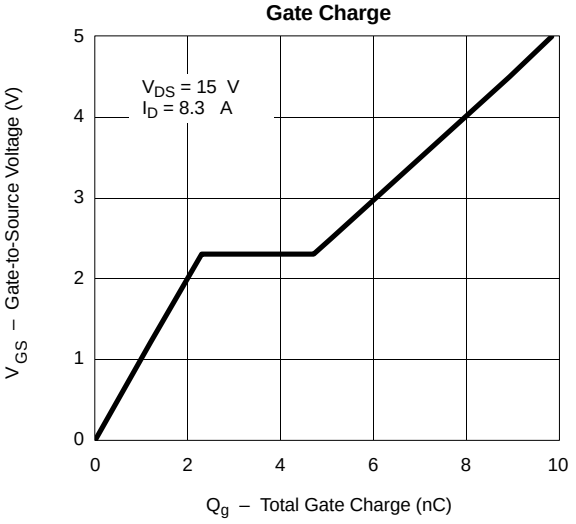
Transfer Characteristics



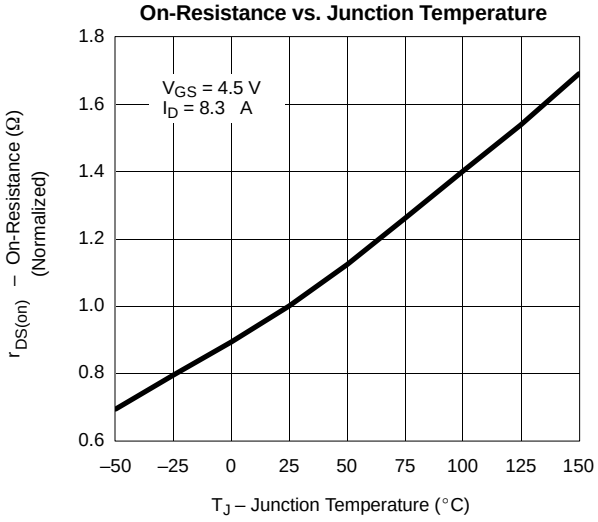
On-Resistance vs. Drain Current



Gate Charge

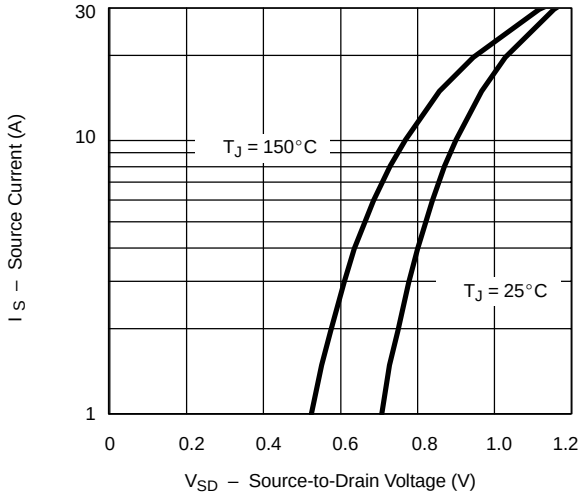


On-Resistance vs. Junction Temperature

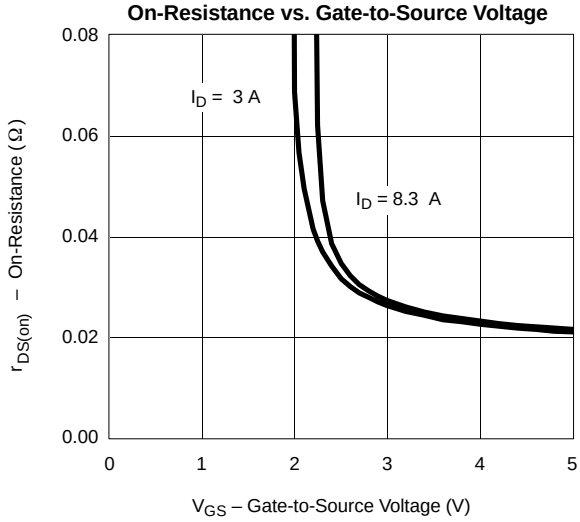


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

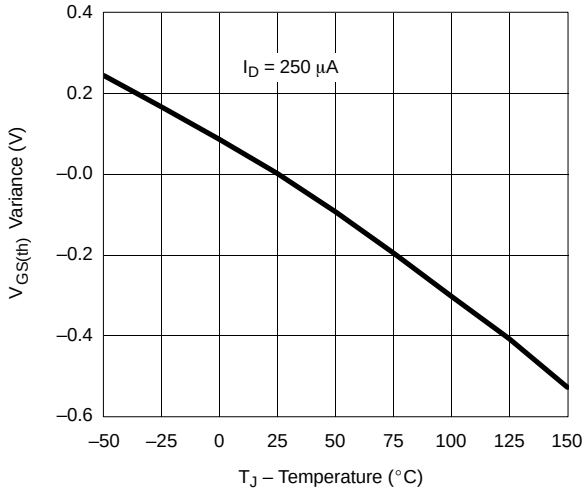
Source-Drain Diode Forward Voltage



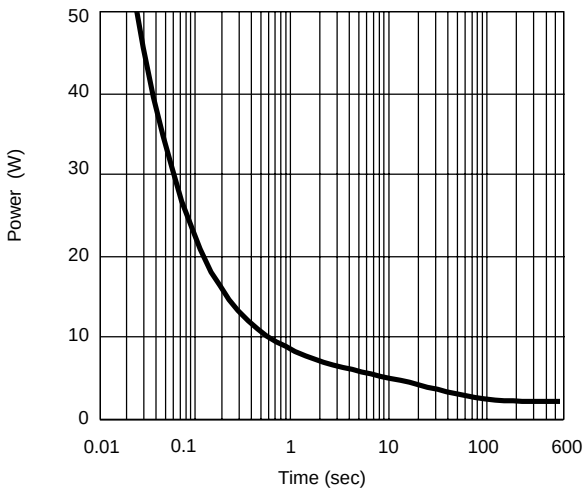
On-Resistance vs. Gate-to-Source Voltage



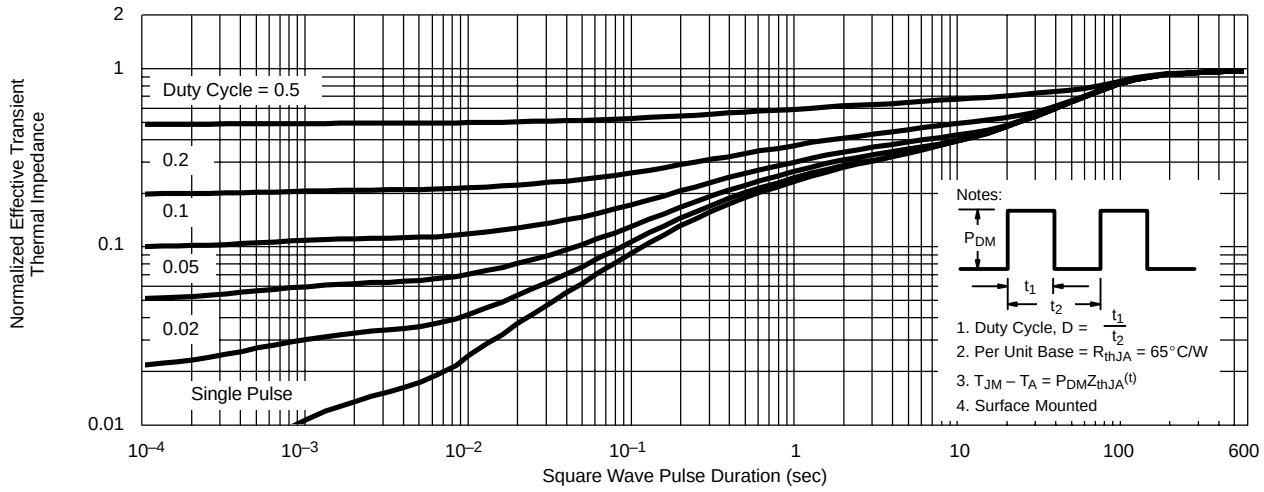
Threshold Voltage



Single Pulse Power, Juncion-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Case