Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.051 @ V_{GS} = -4.5 V	-5.7
	0.067 @ V_{GS} = -2.5 V	-5.0
	0.094 @ V_{GS} = -1.8 V	-4.2

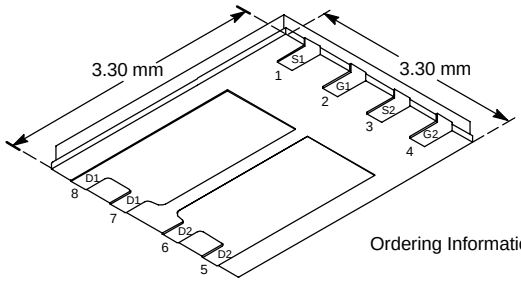
FEATURES

- TrenchFET® Power MOSFETS: 1.8-V Rated
- New Low Thermal Resistance PowerPAK® Package

APPLICATIONS

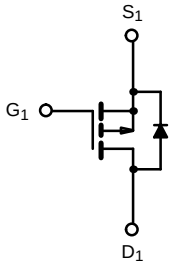
- Portable
  - PA Switch
  - Battery Switch
  - Load Switch

PowerPAK 1212-8

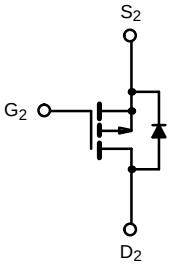


Bottom View

Ordering Information: Si7911DN-T1



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	-20		V
Gate-Source Voltage		V_{GS}	±8		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	-5.7	-4.2	A
	T_A = 85°C		-4.1	-3.0	
Pulsed Drain Current		I_{DM}	-20		
continuous Source Current (Diode Conduction)[a]		I_S	-2.1	-1.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	1.3	W
	T_A = 85°C		1.3	0.85	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	40	50	°C/W
	Steady State		75	94	
Maximum Junction-to-Case	Steady State	R_{thJC}	5.6	7	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

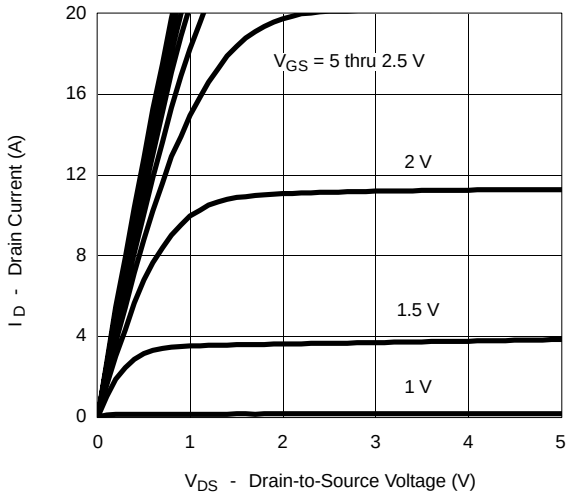
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA	-0.40		-1.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -16 V, V_{GS} = 0 V, T_J = 85°C			-5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≤ -5 V, V_{GS} = -4.5 V	-20			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = -4.5 V, I_D = -5.7 A		0.040	0.051	Ω
		V_{GS} = -2.5 V, I_D = -5.0 A		0.054	0.067	
		V_{GS} = -1.8 V, I_D = -1.1 A		0.075	0.094	
Forward Transconductance[a]	g_{fs}	V_{DS} = -6 V, I_D = -5.7 A		14		S
Diode Forward Voltage[a]	V_{SD}	I_S = -2.3 A, V_{GS} = 0 V		-0.8	-1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -6 V, V_{GS} = -4.5 V, I_D = -5.7 A		9.5	15	nC
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			2.5		
Gate Resistance	R_g			7.2		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -10 V, R_L = 10 Ω I_D ≅ -1 A, V_{GEN} = -4.5 V, R_G = 6 Ω		20	30	ns
Rise Time	t_r			35	55	
Turn-Off Delay Time	$t_{d(off)}$			70	105	
Fall Time	t_f			40	60	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = -2.1 A, di/dt = 100 A/µs		25	50	

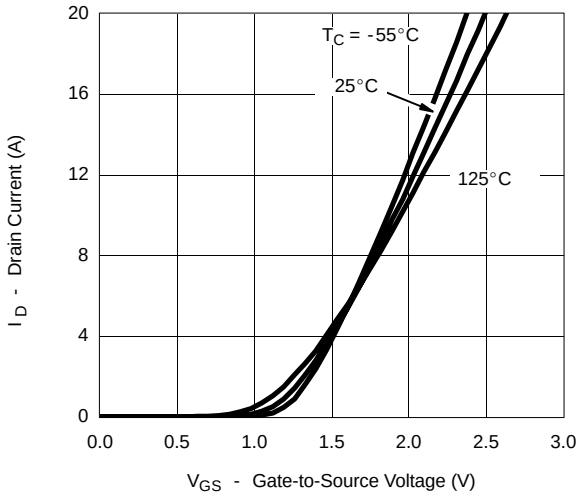
Notes
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

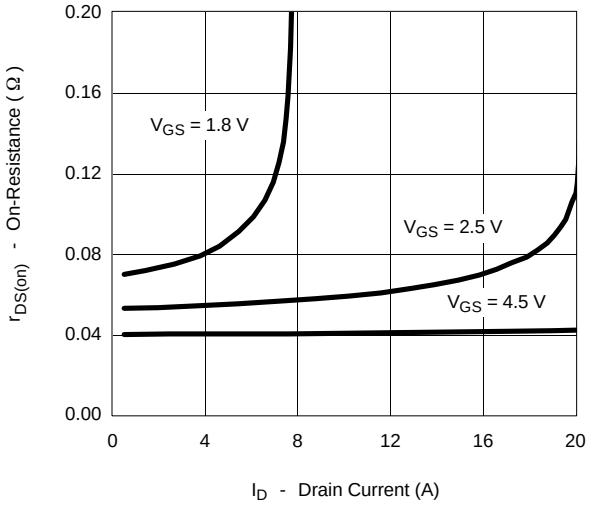


Transfer Characteristics

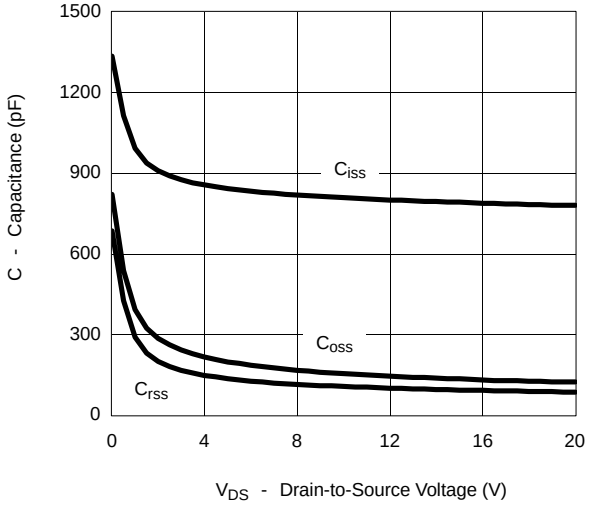


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

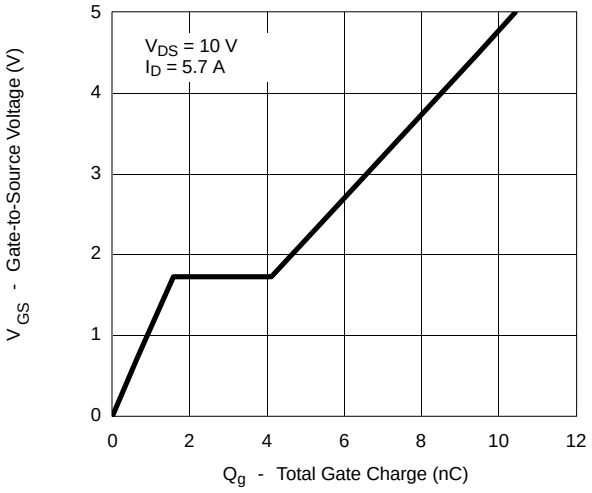
On-Resistance vs. Drain Current



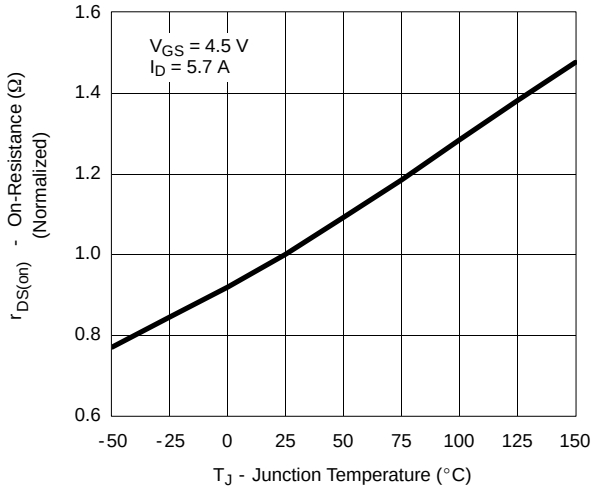
Capacitance



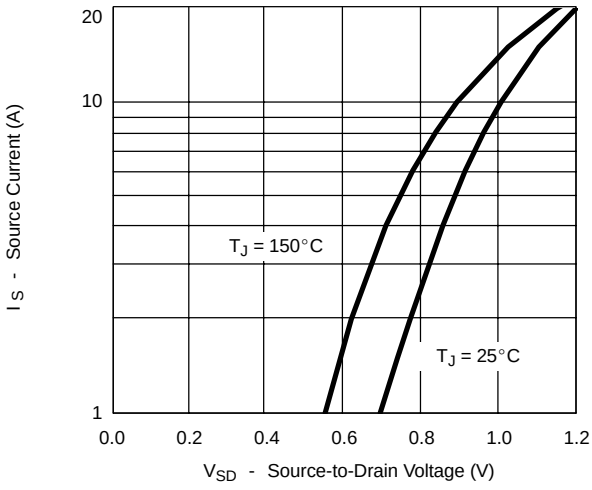
Gate Charge



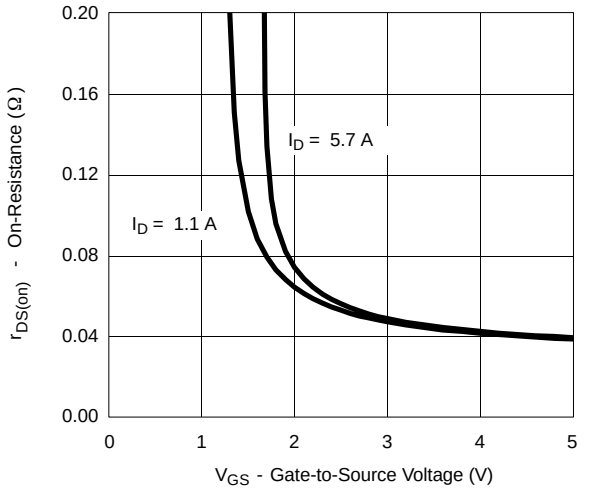
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

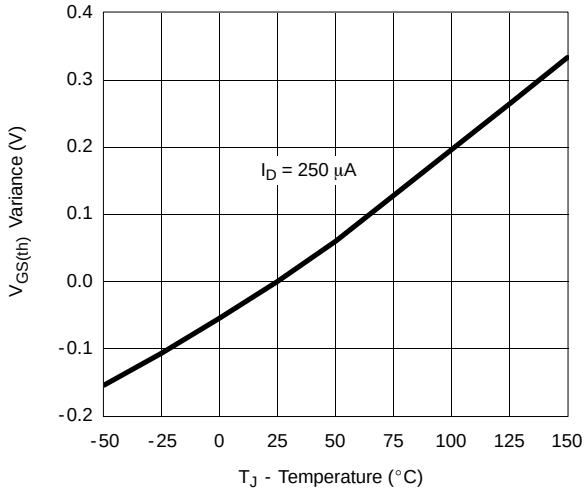


On-Resistance vs. Gate-to-Source Voltage

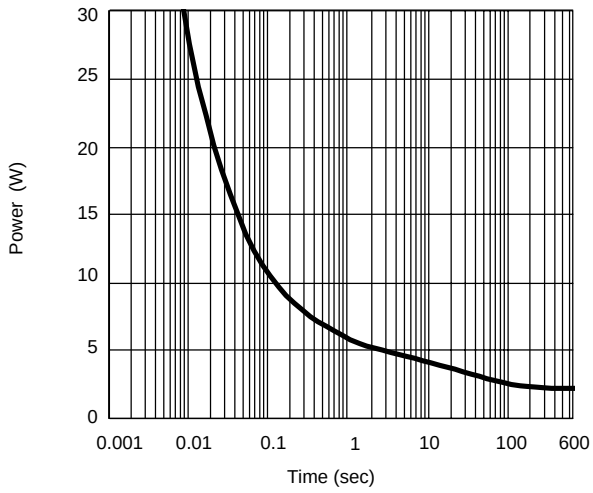


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

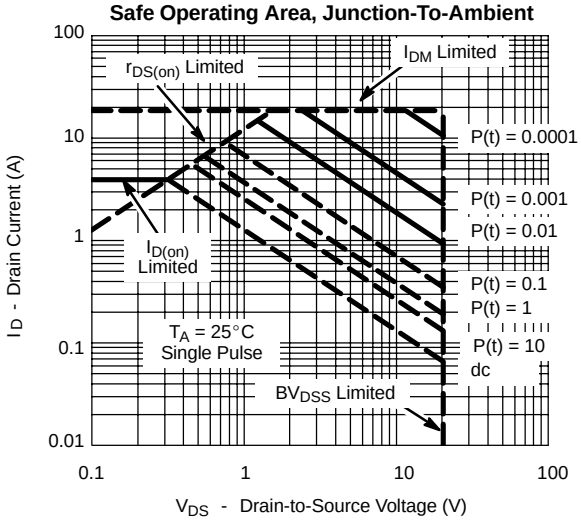
Threshold Voltage



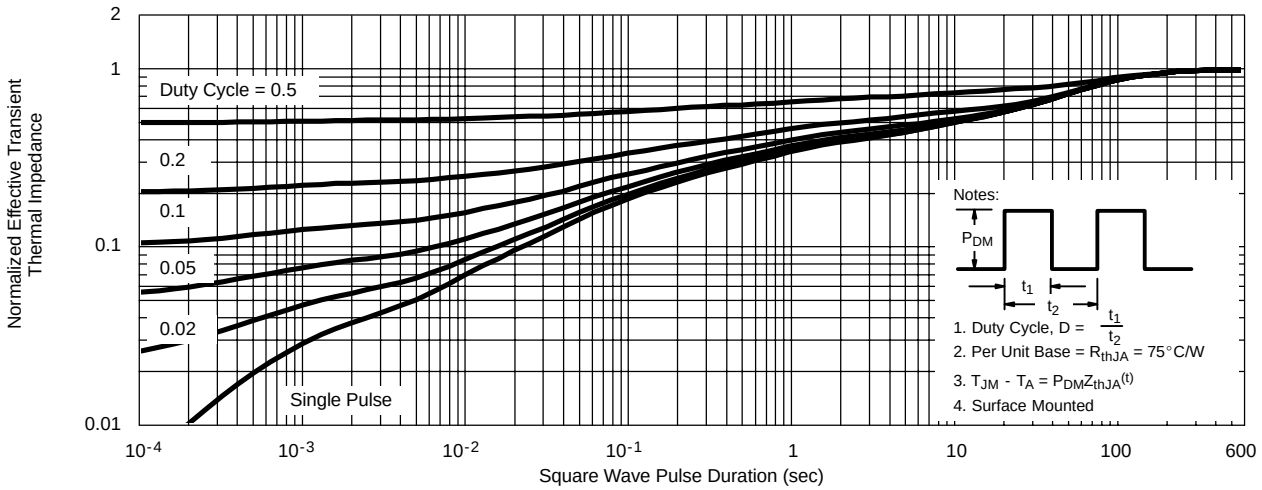
Single Pulse Power



Safe Operating Area, Junction-To-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)