



Dual N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
100	0.049 @ $V_{GS} = 10$ V	5.9
	0.060 @ $V_{GS} = 6$ V	5.5

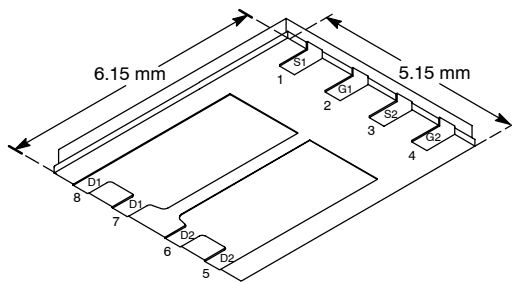
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package
- Dual MOSFET for Space Savings

APPLICATIONS

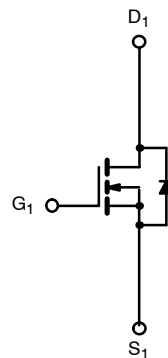
- Synchronous Buck Shoot-Through Resistant
- Optimized for Primary Side Switch

PowerPAK SO-8

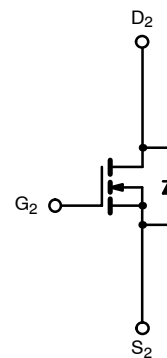


Bottom View

Ordering Information: Si7942DP-T1



N-Channel MOSFET



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	100		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	5.9	3.8	A
	T _A = 70°C		4.7	3.0	
Pulsed Drain Current		I _{DM}	20		
Continuous Source Current (Diode Conduction) ^a		I _S	2.9	1.2	
Single Avalanche Current	L = 0.1 mH	I _{AS}	20		mJ
Single Avalanche Energy		E _{AS}	20		
Maximum Power Dissipation ^a	T _A = 25°C	P _D	3.5	1.4	W
	T _A = 70°C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	26	35	$^\circ\text{C/W}$
	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	2.2	2.7	

Notes

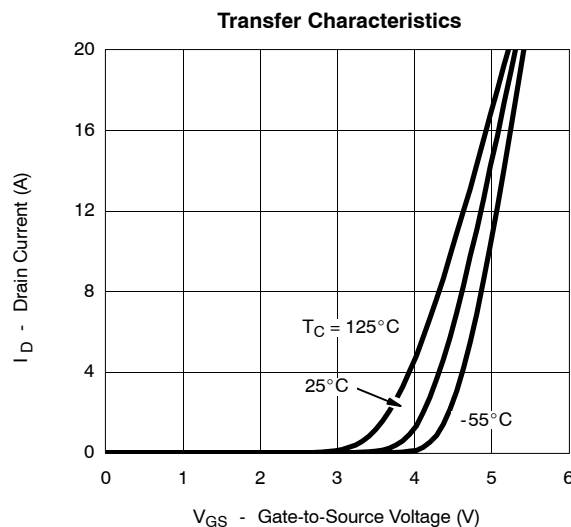
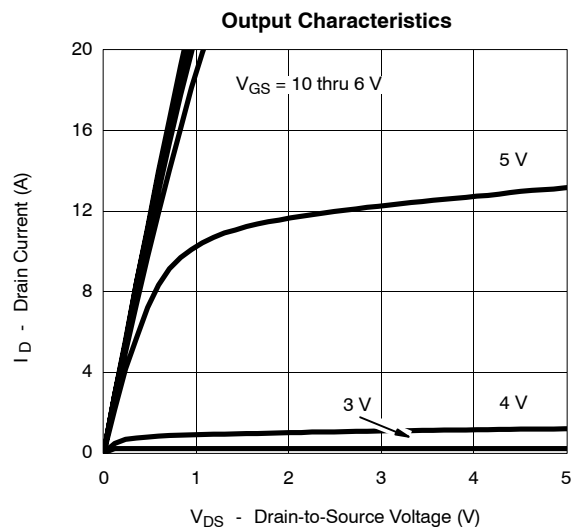
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2		4.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}, V_{GS} = 10\ \text{V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}, I_D = 5.9\ \text{A}$		0.041	0.049	Ω
		$V_{GS} = 6\ \text{V}, I_D = 5.5\ \text{A}$		0.048	0.060	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}, I_D = 5.9\ \text{A}$		14		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 2.9\ \text{A}, V_{GS} = 0\ \text{V}$		0.77	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 50\ \text{V}, V_{GS} = 10\ \text{V}, I_D = 5.9\ \text{A}$		16	24	nC
Gate-Source Charge	Q_{gs}			3.8		
Gate-Drain Charge	Q_{gd}			5.5		
Gate Resostance	R_g			2.2		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\ \text{V}, R_L = 50\ \Omega$ $I_D \cong 1\ \text{A}, V_{GEN} = 10\ \text{V}, R_G = 6\ \Omega$		15	25	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			35	55	
Fall Time	t_f			20	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.9\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		50	75	

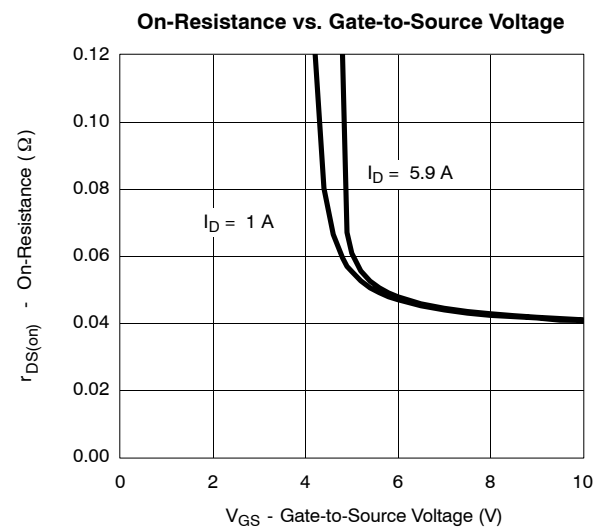
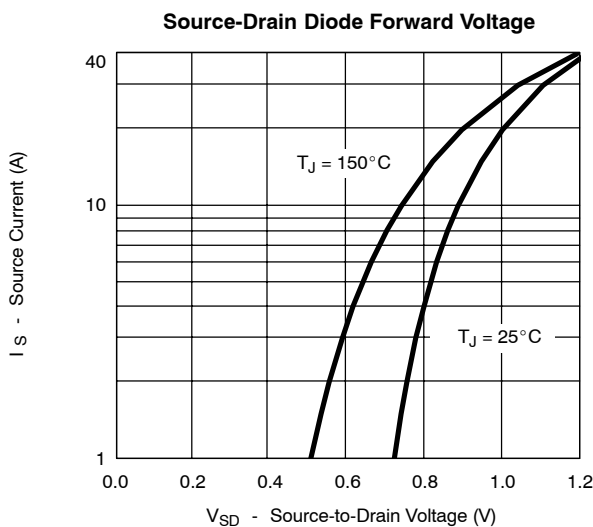
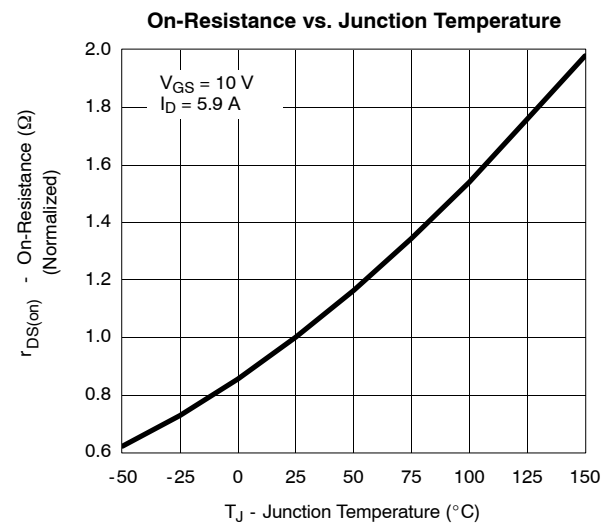
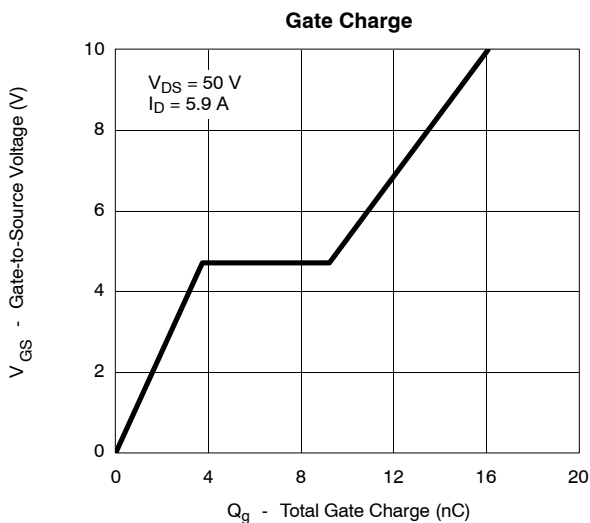
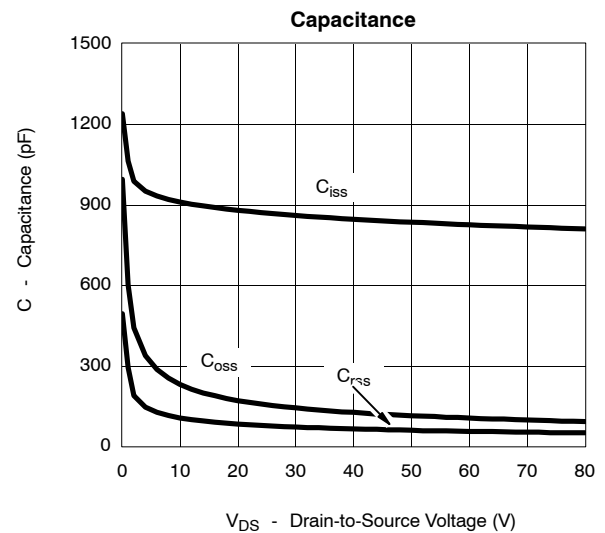
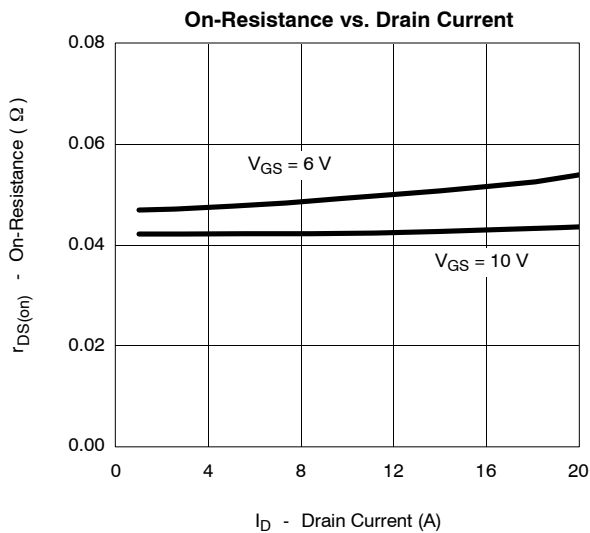
Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

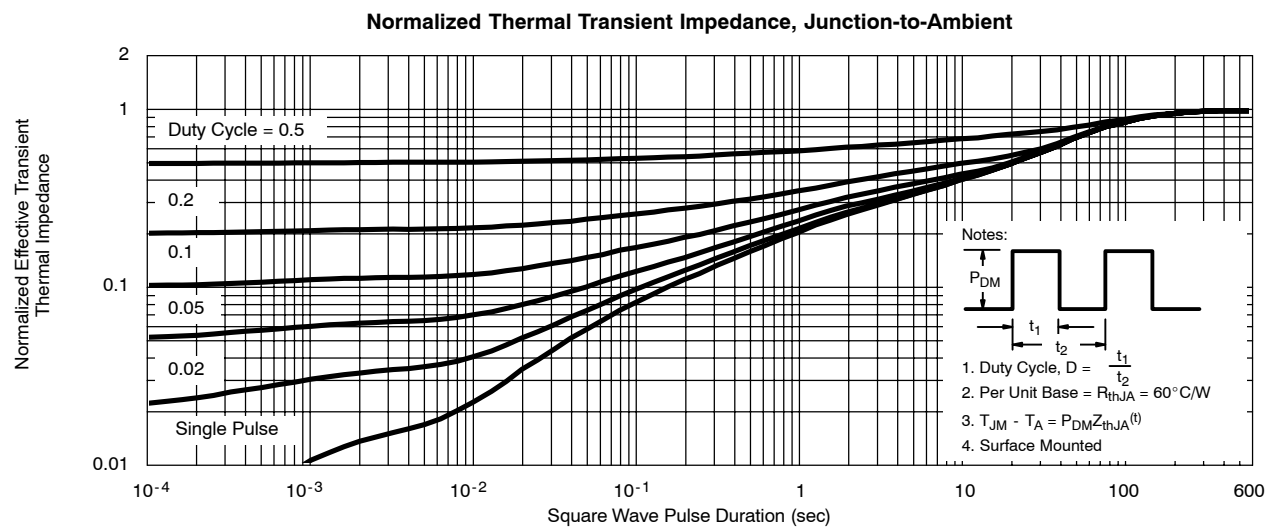
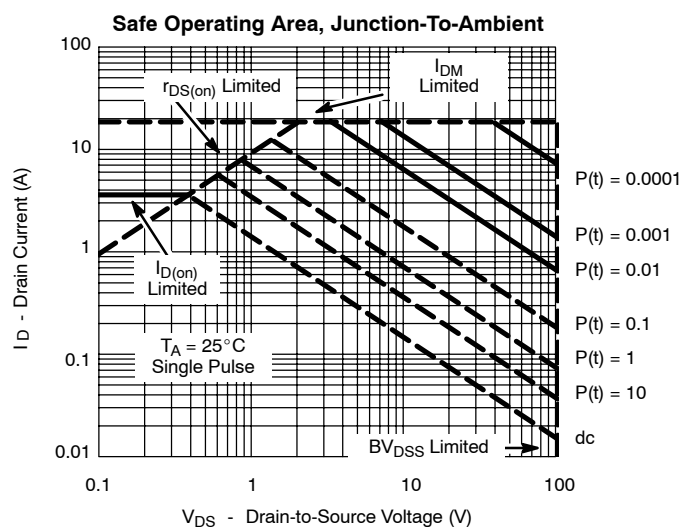
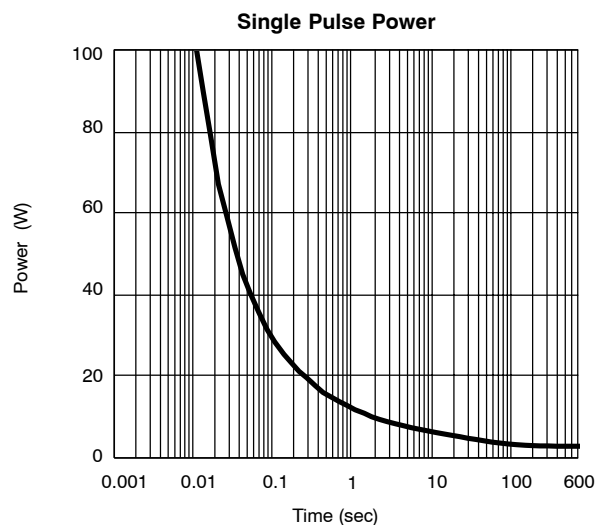
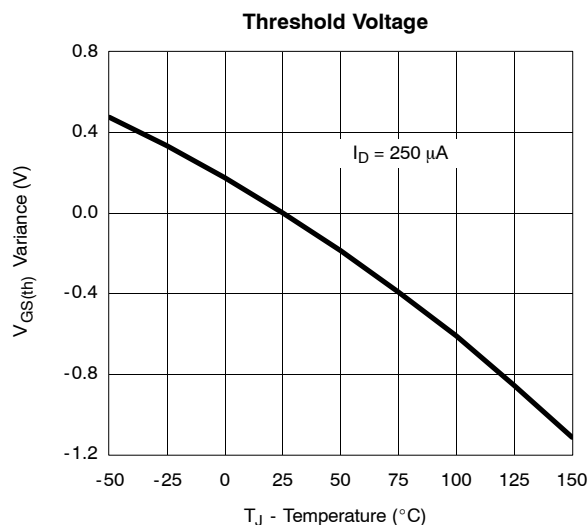
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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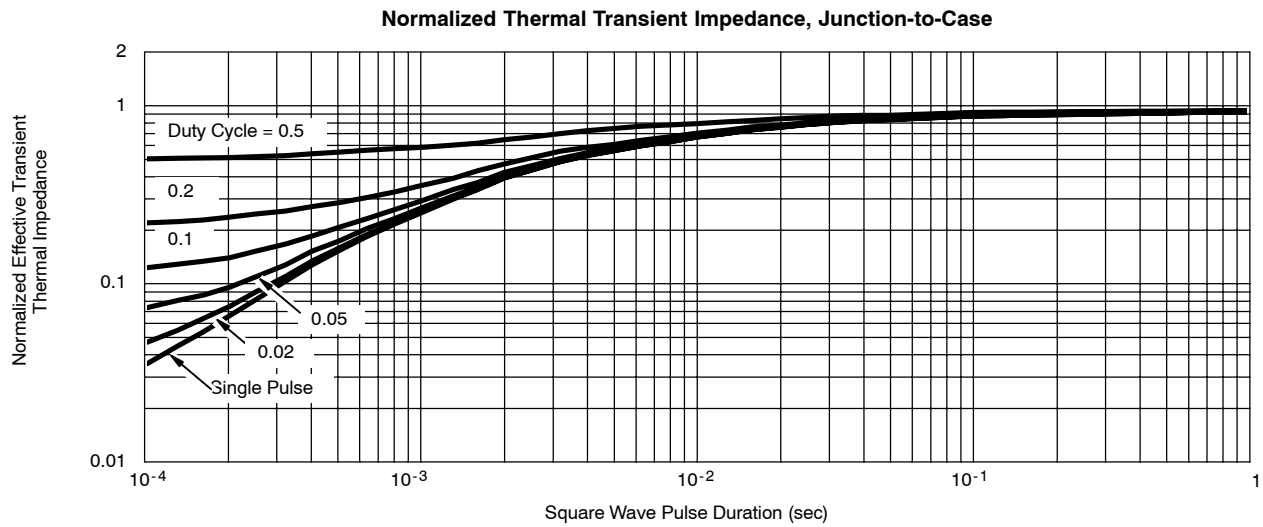


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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