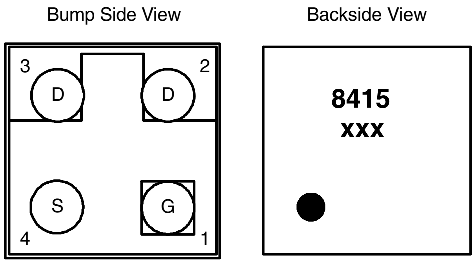
P-Channel 12 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 12	0.037 at V_{GS} = - 4.5 V	- 7.3	19
	0.046 at V_{GS} = - 2.5 V	- 6.6	
	0.060 at V_{GS} = - 1.8 V	- 5.8	

MICRO FOOT


Bump Side View
Backside View

Device Marking: 8415
xxx = Date/Lot Traceability Code

Ordering Information: Si8415DB-T1-E1 (Lead (Pb)-free and Halogen-free)

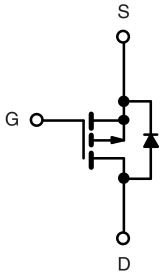
FEATURES

- TrenchFET® Power MOSFET
- MICRO FOOT® Chipscale Packaging Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area
- Ultra-Low On-Resistance
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Load Switch, Charger Switch, and PA Switch for Portable Devices



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	- 12		V
Gate-Source Voltage		V_{GS}	± 8		
Continuous Drain Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	- 7.3	- 5.3	A
	T_A = 70 °C		- 5.9	- 4.3	
Pulsed Drain Current		I_{DM}	- 25		
Continuous Source Current (Diode Conduction)[a]		I_S	- 2.5	- 1.3	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	2.77	1.47	W
	T_A = 70 °C		1.77	0.94	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C
Package Reflow Conditions[b]	IR/Convection		260		

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 5 s	R_{thJA}	35	45	°C/W
	Steady State		72	85	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	16	20	

Notes:
a. Surface mounted on 1" x 1" FR4 board.
b. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
c. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.

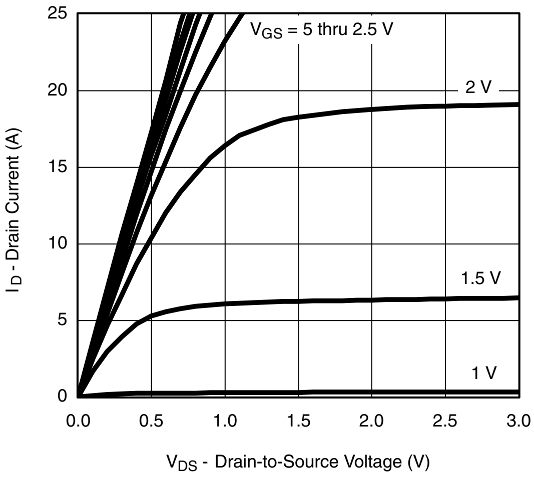
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = - 250 µA	- 0.4		- 1	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 8 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = - 12 V, V_{GS} = 0 V			- 1	µA
		V_{DS} = - 12 V, V_{GS} = 0 V, T_J = 70 °C			- 5	
On-State Drain Current[a]	$I_{D(on)}$	$V_{DS} \leq$ - 5 V, V_{GS} = - 4.5 V	- 5			A
Drain-Source On-State Resistance[a]	$R_{DS(on)}$	V_{GS} = - 4.5 V, I_D = - 1 A		0.031	0.037	Ω
		V_{GS} = - 2.5 V, I_D = - 1 A		0.038	0.046	
		V_{GS} = - 1.8 V, I_D = - 1 A		0.050	0.060	
Forward Transconductance[a]	g_{fs}	V_{DS} = - 10 V, I_D = - 1 A		11		S
Diode Forward Voltage[a]	V_{SD}	I_S = - 1 A, V_{GS} = 0 V		- 0.8	- 1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = - 6 V, V_{GS} = - 4.5 V, I_D = - 1 A		19	30	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			4.8		
Gate Resistance	R_g	f = 1 MHz		19		Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = - 6 V, R_L = 6 Ω $I_D \cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		15	25	ns
Rise Time	t_r			32	50	
Turn-Off Delay Time	$t_{d(off)}$			180	270	
Fall Time	t_f			115	175	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = - 1 A, dI/dt = 100 A/µs		80	120	

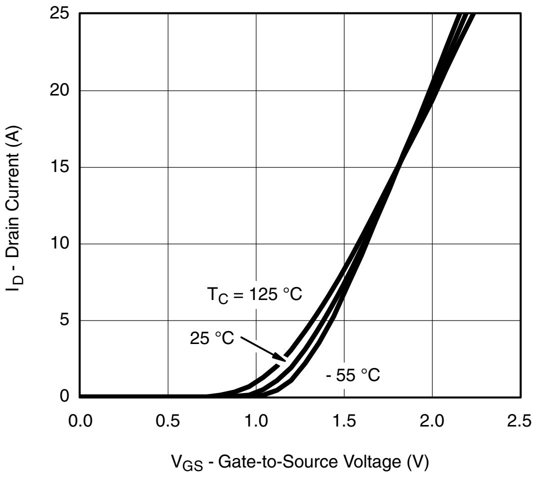
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

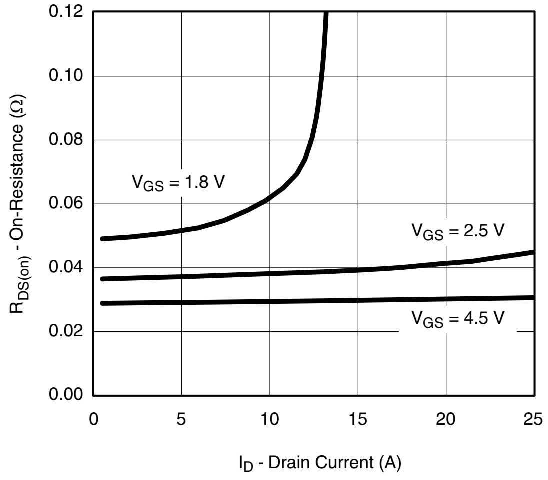


Output Characteristics

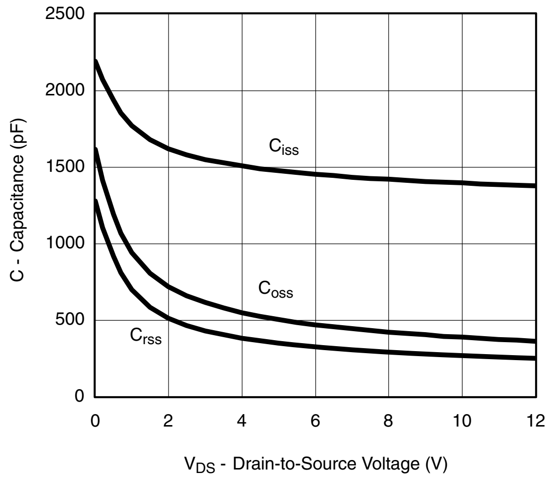


Transfer Characteristics

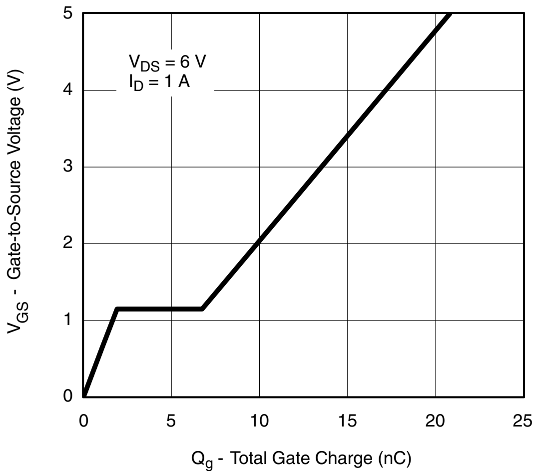
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



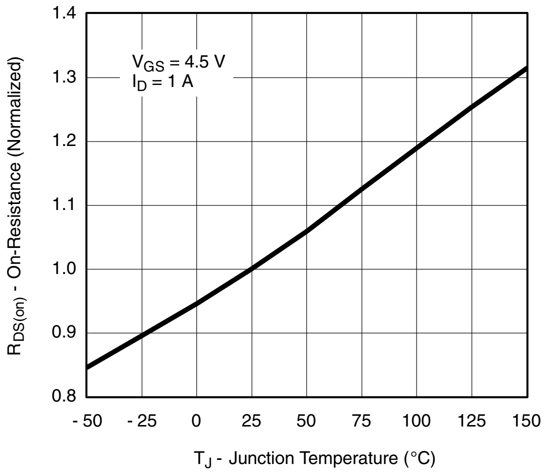
On-Resistance vs. Drain Current



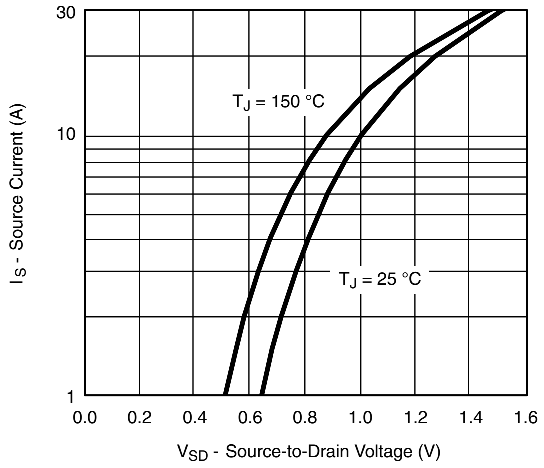
Capacitance



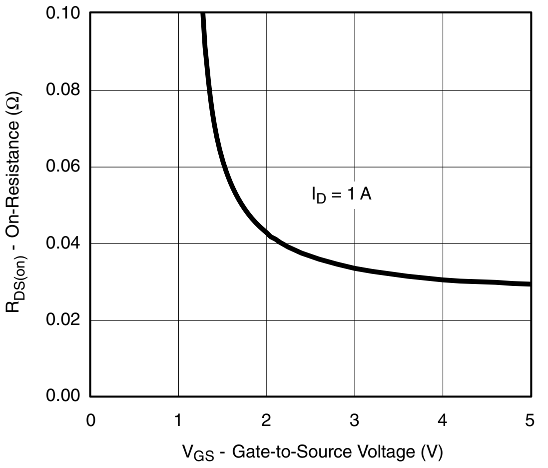
Gate Charge



On-Resistance vs. Junction Temperature

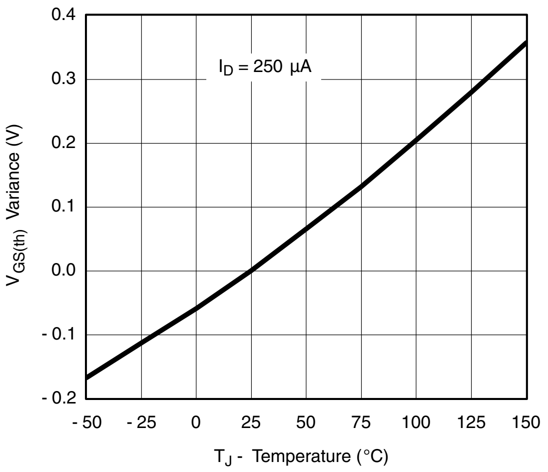


Source-Drain Diode Forward Voltage

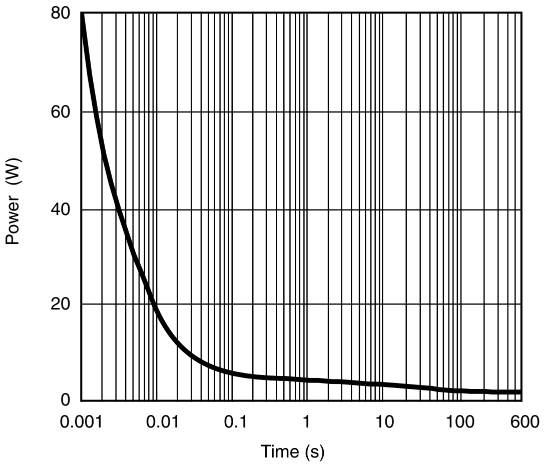


On-Resistance vs. Gate-to-Source Voltage

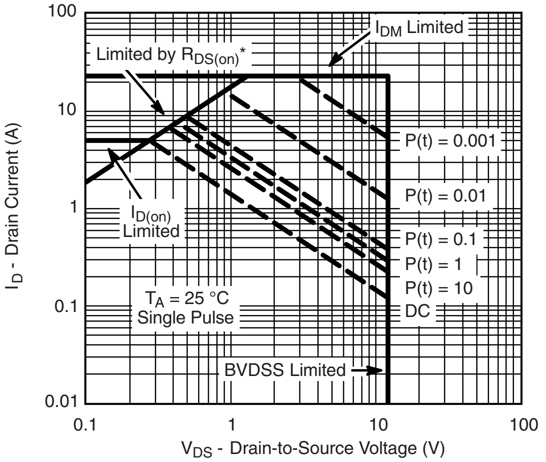
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Threshold Voltage

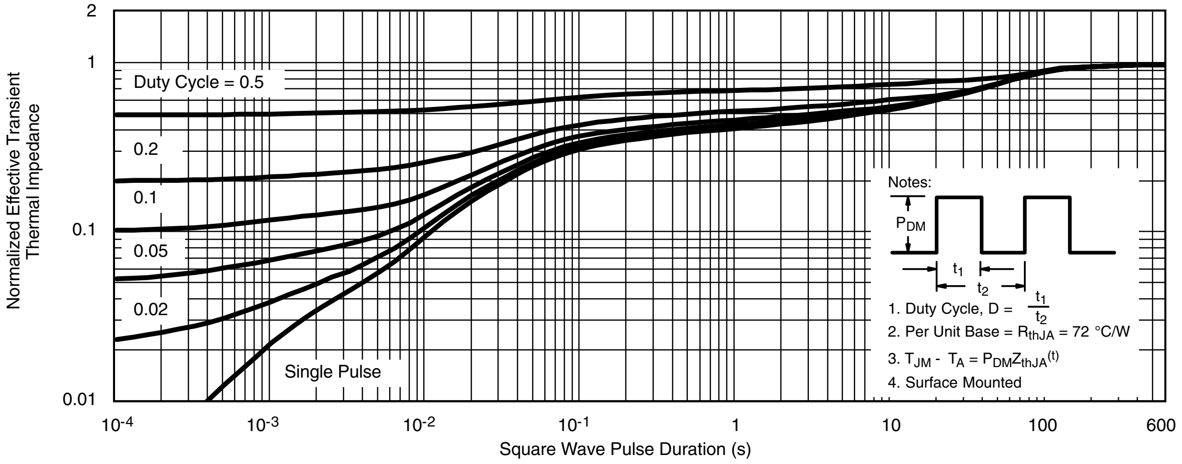


Single Pulse Power, Junction-to-Ambient



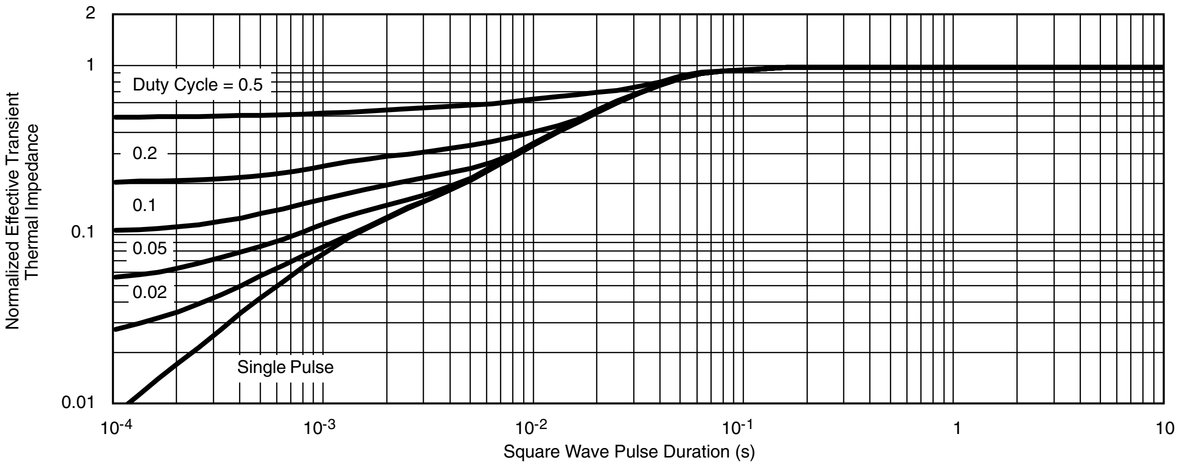
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

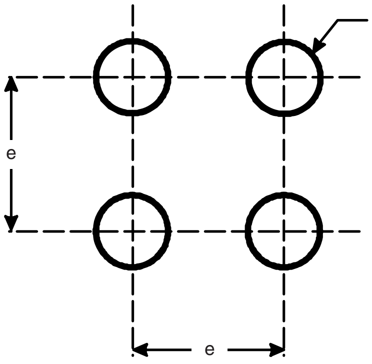
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



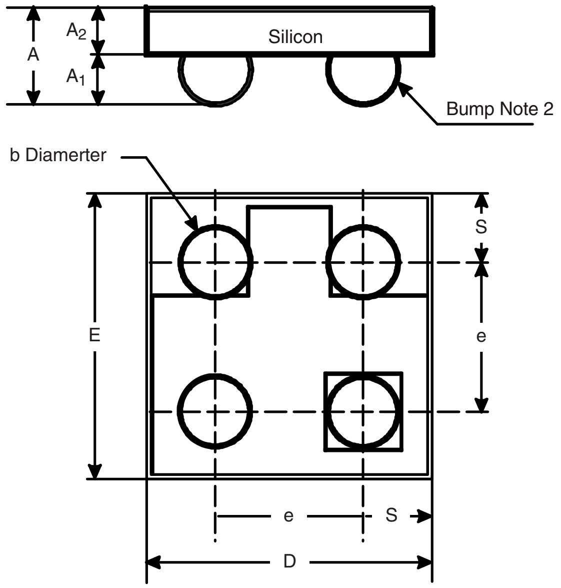
Normalized Thermal Transient Impedance, Junction-to-Foot

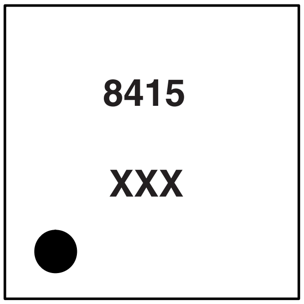
PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (0.8 mm PITCH)



Recommended Land





Mark on Backside of Die

Notes (unless otherwise specified):
1. Laser mark on the silicon die back, coated with a thin metal.
2. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
3. Non-solder mask defined copper landing pad.
4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters[a]		Inches	
	Min.	Max.	Min.	Max.
A	0.600	0.650	0.0236	0.0256
A_1	0.260	0.290	0.0102	0.0114
A_2	0.340	0.360	0.0134	0.0142
b	0.370	0.410	0.0146	0.0161
D	1.520	1.600	0.0598	0.0630
E	1.520	1.600	0.0598	0.0630
e	0.800		0.0315	
S	0.360	0.400	0.0142	0.0157

Notes:
a. Use millimeters as the primary measurement.

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