N-Channel 24 V (D-S) MOSFET

PRODUCT SUMMARY		
V_{S1S2} (V)	R_{S1S2} (Ω) Max.	I_{S1S2} (A) [a]
24	0.028 at V_{GS} = 4.5 V	5.9
	0.029 at V_{GS} = 3.7 V	5.8
	0.031 at V_{GS} = 2.5 V	5.6
	0.037 at V_{GS} = 1.8 V	5.1

FEATURES

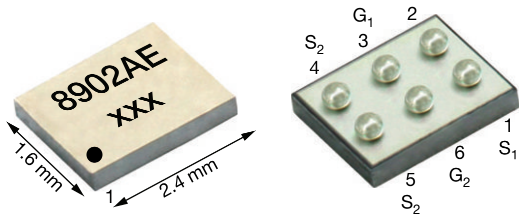
- TrenchFET® power MOSFET
- Small 2.4 mm x 1.6 mm outline
- Thin 0.6 mm max. height
- Typical ESD protection 5000 V (HBM)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS
COMPLIANT
HALOGEN
FREE

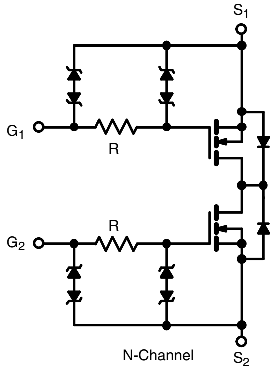
APPLICATIONS

- Battery protection switch
- Bi-directional switch

MICRO FOOT® 2.4 x 1.6



Backside View Bump Side View



Marking Code: 8902AE

Ordering Information:
Si8902AEDB-T2-E1 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Source 1-to-Source 2 Voltage		V_{S1S2}	24	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Source 1-to-Source 2 Current (T_J = 150 °C)	T_C = 25 °C	I_{S1S2}	11 [b]	A
	T_C = 85 °C		7.9 [b]	
	T_A = 25 °C		5.9 [a]	
	T_A = 85 °C		4.3 [a]	
Pulsed Source 1-to-Source 2 Current (t = 100 μs)		I_{SM}	40	
Maximum Power Dissipation	T_C = 25 °C	P_D	5.7 [b]	W
	T_C = 85 °C		3 [b]	
	T_A = 25 °C		1.7 [a]	
	T_A = 85 °C		0.9 [a]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Soldering Recommendations (Peak Temperature) [c]			260	

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient [a, d]	t ≤ 5 s	R_{thJA}	60	75	°C/W
Maximum Junction-to-Case [b]	Steady State	R_{thJC}	18	22	

Notes

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. The case is defined as the top surface of the package.
c. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
d. Maximum under steady state conditions is 120 °C/W.

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Source 1-to-Source 2 Breakdown Voltage	V_{S1S2}	V_{GS} = 0 V, I_S = 250 µA	24	-	-	V
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_S = 250 µA	-	3	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{SS} = V_{GS} , I_S = 250 µA	0.4	-	0.9	V
Gate-Source Leakage	I_{GSS}	V_{SS} = 0 V, V_{GS} = ± 4.5 V	-	-	± 0.2	µA
		V_{SS} = 0 V, V_{GS} = ± 12 V	-	-	± 10	mA
Zero Gate Voltage Source Current	I_{S1S2}	V_{SS} = 24 V, V_{GS} = 0 V	-	-	1	µA
		V_{SS} = 24 V, V_{GS} = 0 V, T_J = 85 °C	-	-	10	
On-State Source Current [a]	$I_{S(on)}$	$V_{SS} \geq$ 5 V, V_{GS} = 4.5 V	5	-	-	A
Source1-to-Source 2 On-State Resistance [a]	R_{S1S2}	V_{GS} = 4.5 V, I_{SS} = 1 A	-	0.0215	0.0280	Ω
		V_{GS} = 3.7 V, I_{SS} = 1 A	-	0.0222	0.0290	
		V_{GS} = 2.5 V, I_{SS} = 1 A	-	0.0240	0.0310	
		V_{GS} = 1.8 V, I_{SS} = 1 A	-	0.0260	0.0370	
Forward Transconductance [a]	g_{fs}	V_{SS} = 10 V, I_{SS} = 1 A	-	15	-	S
Dynamic [b]						
Gate Resistance	R_g	f = 1 MHz	-	5.3	-	kΩ
Turn-On Delay Time	$t_{d(on)}$	V_{SS} = 12.5 V, R_L = 12.5 Ω $I_{SS} \cong$ 1 A, V_{GEN} = 4.5 V, R_g = 1 Ω	-	1.5	3	µs
Rise Time	t_r		-	3.5	7	
Turn-Off Delay Time	$t_{d(off)}$		-	25	50	
Fall Time	t_f		-	12	25	
Turn-On Delay Time	$t_{d(on)}$	V_{SS} = 12.5 V, R_L = 12.5 Ω $I_{SS} \cong$ 1 A, V_{GEN} = 10 V, R_g = 1 Ω	-	0.7	1.4	
Rise Time	t_r		-	1.3	2.6	
Turn-Off Delay Time	$t_{d(off)}$		-	35	70	
Fall Time	t_f		-	12	25	

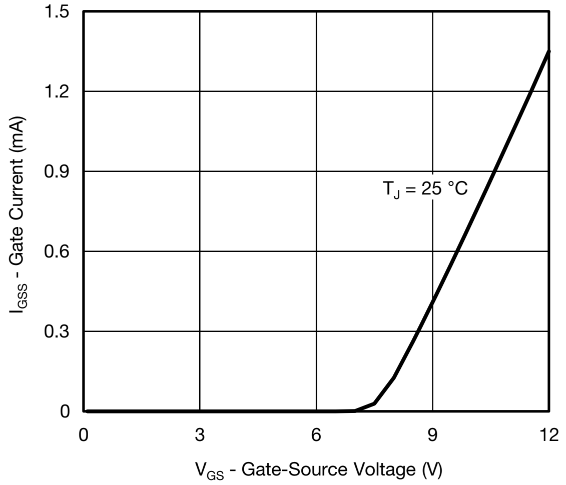
Notes

a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

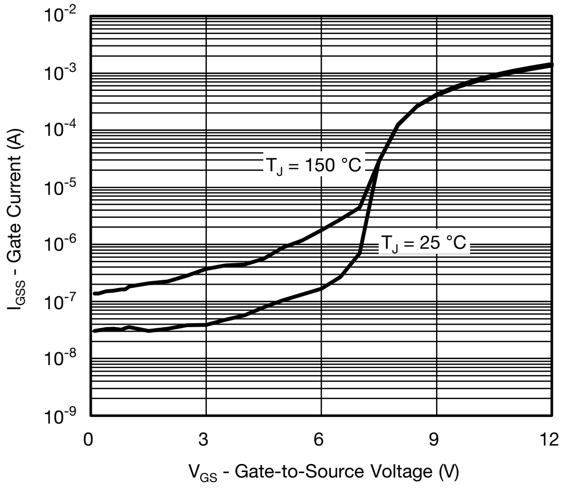
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

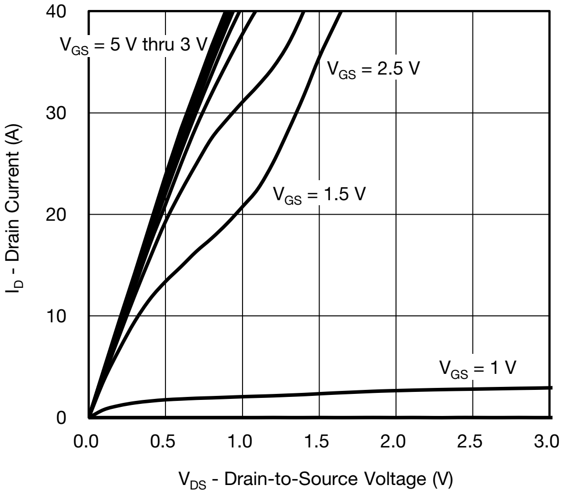
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



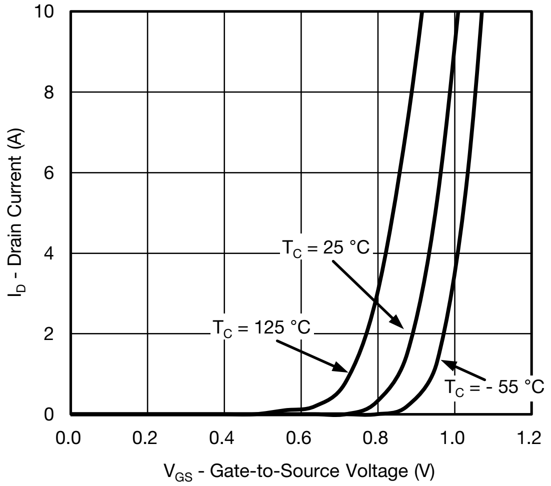
Gate Current vs. Gate-Source Voltage



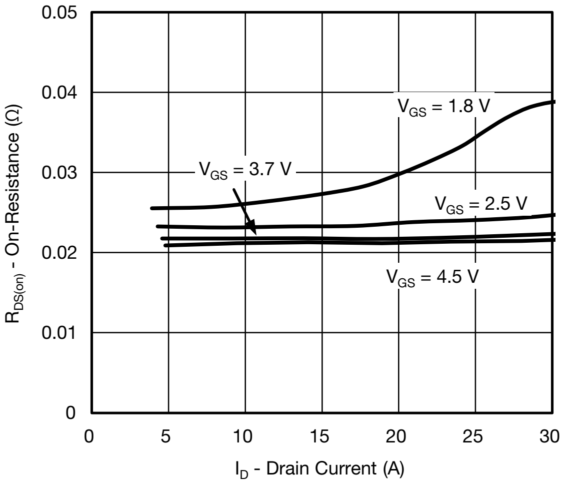
Gate Current vs. Gate-Source Voltage



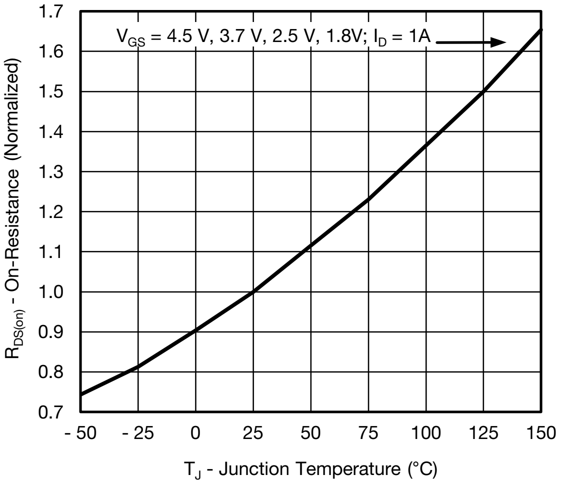
Output Characteristics



Transfer Characteristics

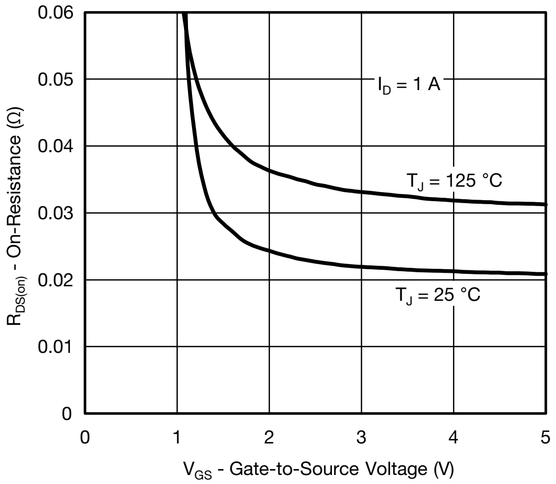


On-Resistance vs. Drain Current

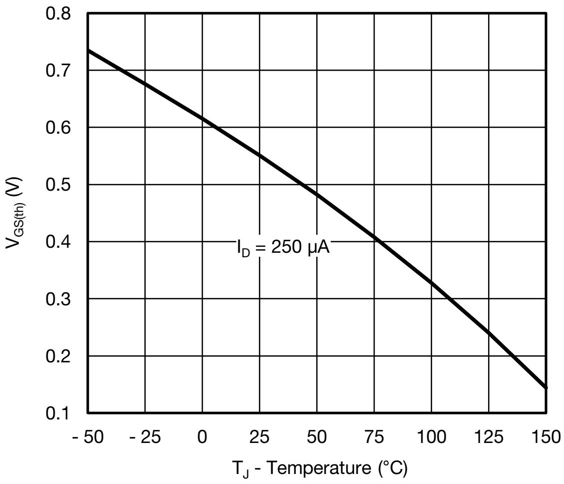


On-Resistance vs. Junction Temperature

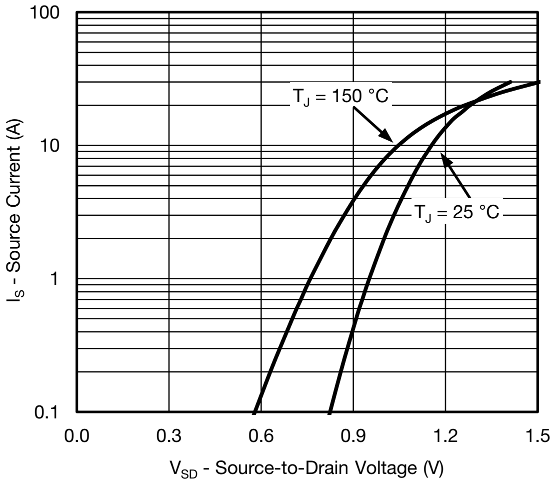
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



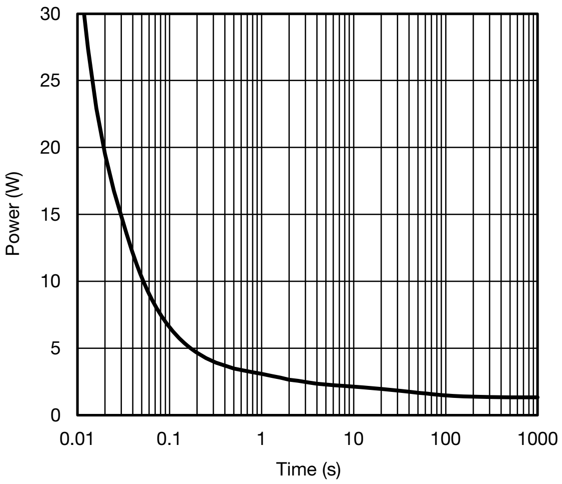
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

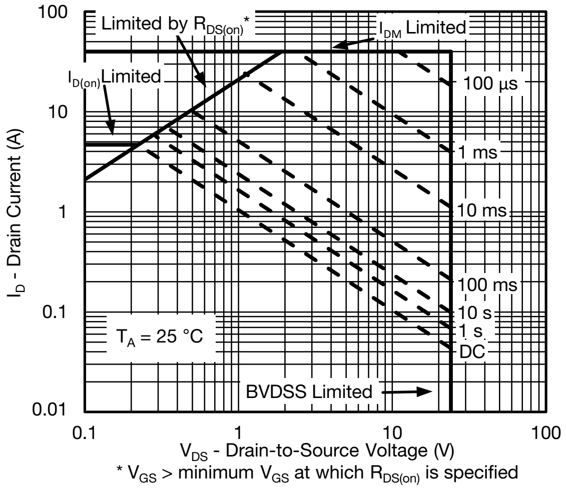


Source-Drain Diode Forward Voltage

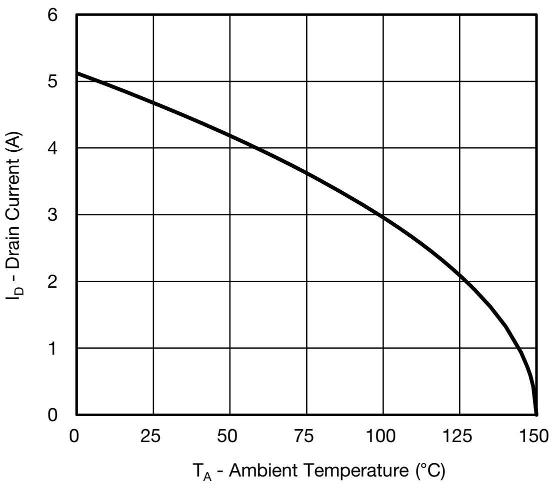


Single Pulse Power (Junction-to-Ambient)

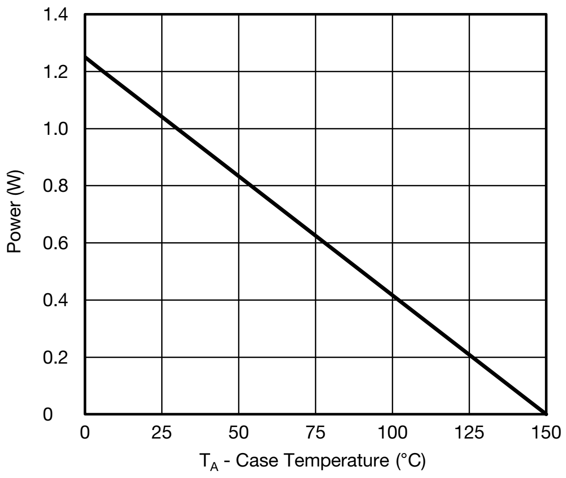
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating*



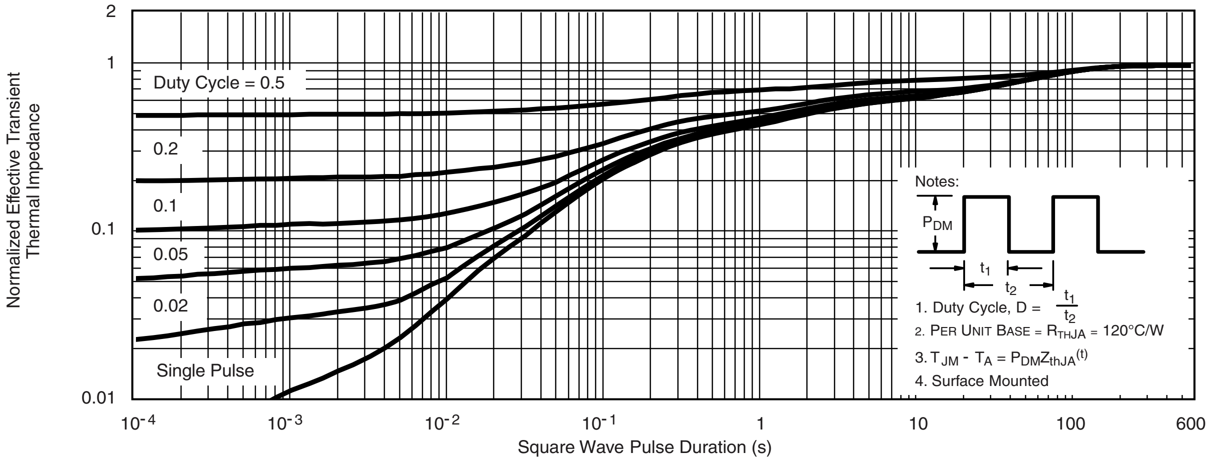
Power Derating

Note

- When mounted on 1" x 1" FR4 with full copper.

* The power dissipation P_D is based on $T_{J\ (max.)}$ = 150 °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

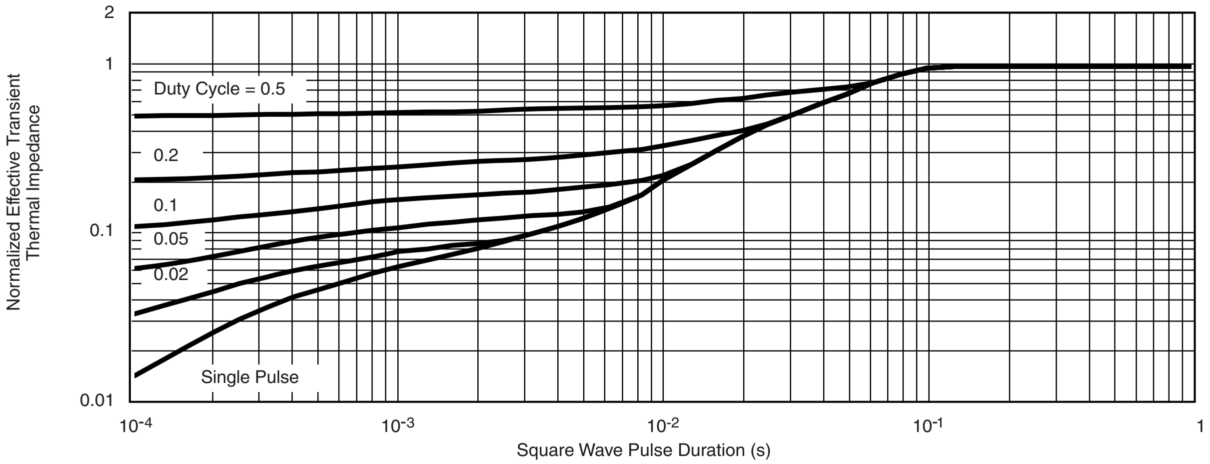


Notes:

1. Duty Cycle, D = $\frac{t_1}{t_2}$
2. PER UNIT BASE = R_{THJA} = 120°C/W
3. $T_{JM} - T_A = P_{DM}Z_{thJA}^{(t)}$
4. Surface Mounted

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 board with maximum copper)

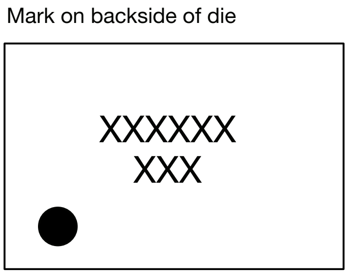


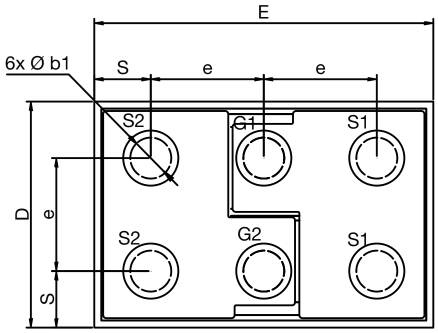
Normalized Thermal Transient Impedance, Junction-to-Case

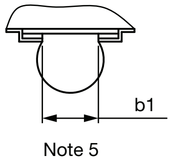
Normalized Thermal Transient Impedance, Junction-to-Case (on 1" x 1" FR4 board with minimum copper)

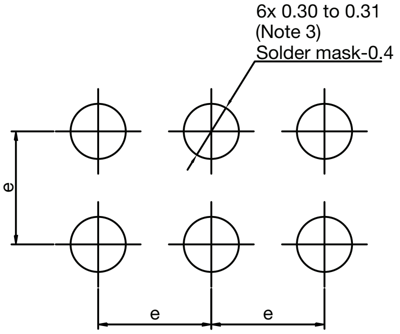
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62948.

MICRO FOOT®: 6-Bumps (1.6 mm x 2.4 mm, 0.8 mm Pitch, 0.290 mm Bump Height)

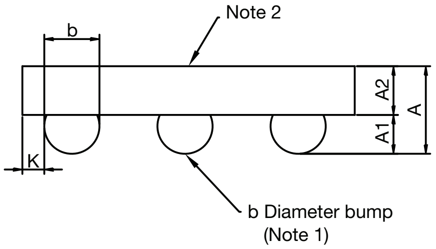








Recommended land pattern



Notes

1. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
2. Backside surface is coated with a Ti/Ni/Ag layer.
3. Non-solder mask defined copper landing pad.
4. Laser marks on the silicon die back.
5. “b1” is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
6. • is the location of pin 1

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.550	0.575	0.600	0.0217	0.0226	0.0236
A1	0.260	0.275	0.290	0.0102	0.0108	0.0114
A2	0.290	0.300	0.310	0.0114	0.0118	0.0122
b	0.370	0.390	0.410	0.0146	0.0153	0.0161
b1		0.300			0.0118	
e		0.800			0.0314	
s	0.360	0.380	0.400	0.0141	0.0150	0.0157
D	1.520	1.560	1.600	0.0598	0.0614	0.0630
E	2.320	2.360	2.400	0.0913	0.0929	0.0945
K	0.155	0.185	0.215	0.0061	0.0072	0.0084

Note

- Use millimeters as the primary measurement.

ECN: T15-0143-Rev. A, 27-Apr-15
DWG: 6036

PCB Design and Assembly Guidelines For MICRO FOOT® Products

Johnson Zhao

INTRODUCTION

Vishay Siliconix's MICRO FOOT product family is based on a wafer-level chip-scale packaging (WL-CSP) technology that implements a solder bump process to eliminate the need for an outer package to encase the silicon die. MICRO FOOT products include power MOSFETs, analog switches, and power ICs.

For battery powered compact devices, this new packaging technology reduces board space requirements, improves thermal performance, and mitigates the parasitic effect typical of leaded packaged products. For example, the 6-bump MICRO FOOT Si8902EDB common drain power MOSFET, which measures just 1.6 mm x 2.4 mm, achieves the same performance as TSSOP-8 devices in a footprint that is 80% smaller and with a 50% lower height profile (Figure 1). A MICRO FOOT analog switch, the 6-bump DG3000DB, offers low charge injection and 1.4 W on-resistance in a footprint measuring just 1.08 mm x 1.58 mm (Figure 2).

Vishay Siliconix MICRO FOOT products can be handled with the same process techniques used for high-volume assembly of packaged surface-mount devices. With proper attention to PCB and stencil design, the device will achieve reliable performance without underfill. The advantage of the device's small footprint and short thermal path make it an ideal option for space-constrained applications in portable devices such as battery packs, PDAs, cellular phones, and notebook computers.

This application note discusses the mechanical design and reliability of MICRO FOOT, and then provides guidelines for board layout, the assembly process, and the PCB rework process.

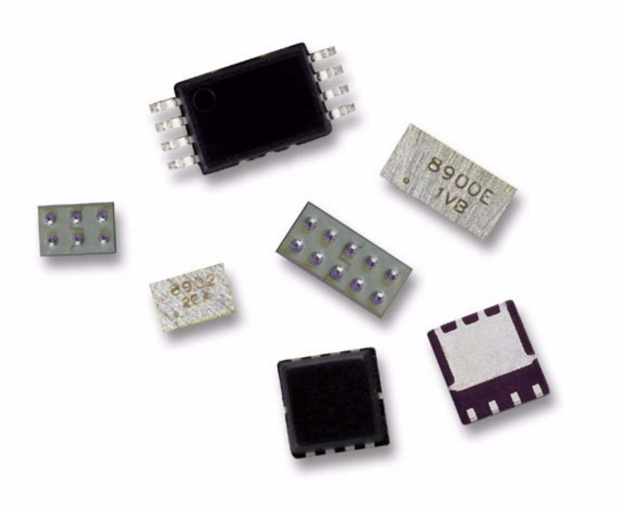


FIGURE 1. 3D View of MICRO FOOT Products Si8902DB and Si8900EDB

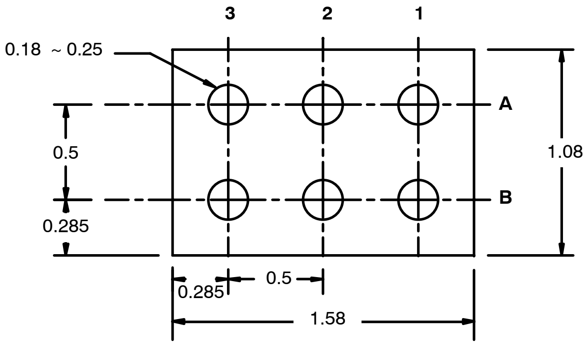


FIGURE 2. Outline of MICRO FOOT CSP & Analog Switch DG3000DB

TABLE 1
Main Parameters of Solder Bumps in MICRO FOOT Designs

MICRO FOOT CSP	Bump Material	Bump Pitch*	Bump Diameter*	Bump Height*
MICRO FOOT CSP MOSFET	Eutectic Solder: 63Sm/37Pb	0.8	0.37-0.41	0.26-0.29
MICRO FOOT CSP Analog Switch		0.5	0.18-0.25	0.14-0.19
MICRO FOOT UCSP Analog Switch		0.5	0.32-0.34	0.21-0.24

* All measurements in millimeters

MICRO FOOT'S DESIGN AND RELIABILITY

As a mechanical, electrical, and thermal connection between the device and PCB, the solder bumps of MICRO FOOT products are mounted on the top active surface of the die. Table 1 shows the main parameters for solder bumps used in MICRO FOOT products. A silicon nitride passivation layer is applied to the active area as the last masking process in fabrication,ensuring that the device passes the pressure pot test. A green laser is used to mark the backside of the die without damaging it. Reliability results for MICRO FOOT products mounted on a FR-4 board without underfill are shown in Table 2.

TABLE 2
MICRO FOOT Reliability Results

Test Condition C: –65° to 150°C	>500 Cycles
Test condition B: –40° to 125°C	>1000 Cycles
121°C @ 15PSI 100% Humidity Test	96 Hours

The main failure mechanism associated with wafer-level chip-scale packaging is fatigue of the solder joint. The results shown in Table 2 demonstrate that a high level of reliability can be achieved with proper board design and assembly techniques.

BOARD LAYOUT GUIDELINES

Board materials. Vishay Siliconix MICRO FOOT products are designed to be reliable on most board types, including organic boards such as FR-4 or polyamide boards. The package qualification information is based on the test on 0.5-oz. FR-4 and polyamide boards with NSMD pad design.

Land patterns. Two types of land patterns are used for surface-mount packages. Solder mask defined (SMD) pads have a solder mask opening smaller than the metal pad (Figure 3), whereas on-solder mask defined (NSMD) pads have a metal pad smaller than the solder-mask opening (Figure 4).

NSMD is recommended for copper etch processes, since it provides a higher level of control compared to SMD etch processes. A small-size NSMD pad definition provides more area (both lateral and vertical) for soldering and more room for escape routing on the PCB. By contrast, SMD pad definition introduces a stress -concentration point near the solder mask on the PCB side that may result in solder joint cracking under extreme fatigue conditions.

Copper pads should be finished with an organic solderability preservative (OSP) coating. For electroplated nickel-immersion gold finish pads, the gold thickness must be less than 0.5 μm to avoid solder joint embrittlement.

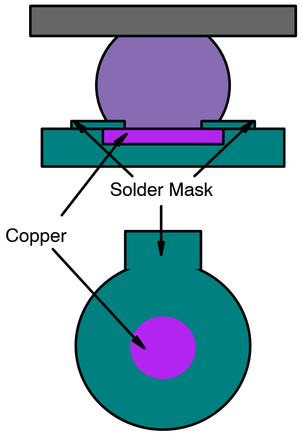


FIGURE 3. SMD

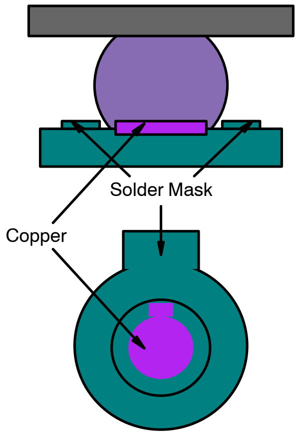


FIGURE 4. NSMD

Board pad design. The landing-pad size for MICRO FOOT products is determined by the bump pitch as shown in Table 3. The pad pattern is circular to ensure a symmetric, barrel-shaped solder bump.

TABLE 3
Dimensions of Copper Pad and Solder Mask Opening in PCB and Stencil Aperture

Pitch	Copper Pad	Solder Mask Opening	Stencil Aperture
0.80 mm	0.30 ± 0.01 mm	0.41 ± 0.01 mm	0.33 ± 0.01 mm in ciircle aperture
0.50 mm	0.17 ± 0.01 mm	0.27 ± 0.01 mm	0.30 ± 0.01 mm in square aperture

ASSEMBLY PROCESS

MICRO FOOT products' surface-mount-assembly operations include solder paste printing, component placement, and solder reflow as shown in the process flow chart (Figure 5).

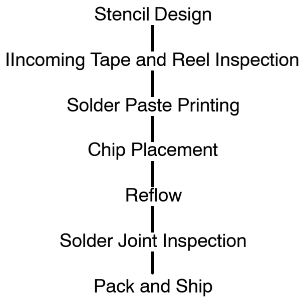


FIGURE 5. SMT Assembly Process Flow

Stencil design. Stencil design is the key to ensuring maximum solder paste deposition without compromising the assembly yield from solder joint defects (such as bridging and extraneous solder spheres). The stencil aperture is dependent on the copper pad size, the solder mask opening, and the quantity of solder paste.

In MICRO FOOT products, the stencil is 0.125-mm (5-mils) thick. The recommended apertures are shown in Table 3 and are fabricated by laser cut.

Solder-paste printing. The solder-paste printing process involves transferring solder paste through pre-defined apertures via application of pressure.

In MICRO FOOT products, the solder paste used is UP78 No-clean eutectic 63 Sn/37Pb type3 or finer solder paste.

Chip pick-and-placement. MICRO FOOT products can be picked and placed with standard pick-and-place equipment. The recommended pick-and-place force is 150 g. Though the part will self-center during solder reflow, the maximum placement offset is 0.02 mm.

Reflow Process. MICRO FOOT products can be assembled using standard SMT reflow processes. Similar to any other package, the thermal profile at specific board locations must be determined. Nitrogen purge is recommended during reflow operation. Figure 6 shows a typical reflow profile.

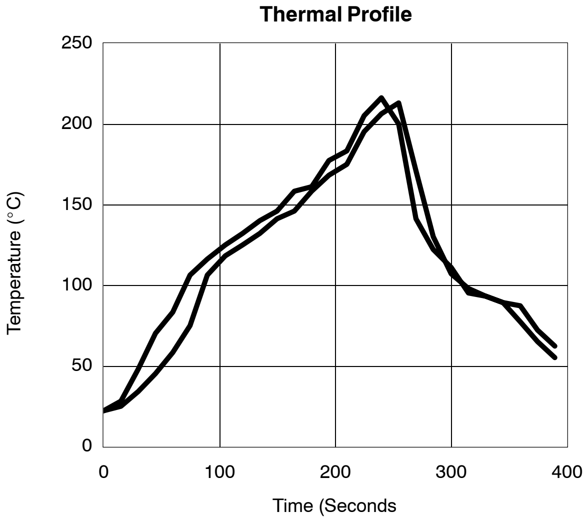


FIGURE 6. Reflow Profile

PCB REWORK

To replace MICRO FOOT products on PCB, the rework procedure is much like the rework process for a standard BGA or CSP, as long as the rework process duplicates the original reflow profile. The key steps are as follows:

1. Remove the MICRO FOOT device using a convection nozzle to create localized heating similar to the original reflow profile. Preheat from the bottom.
2. Once the nozzle temperature is +190°C, use tweezers to remove the part to be replaced.
3. Resurface the pads using a temperature-controlled soldering iron.
4. Apply gel flux to the pad.
5. Use a vacuum needle pick-up tip to pick up the replacement part, and use a placement jig to placed it accurately.
6. Reflow the part using the same convection nozzle, and preheat from the bottom, matching the original reflow profile.

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Material Category Policy

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as RoHS-Compliant fulfill the definitions and restrictions defined under Directive 2011/65/EU of The European Parliament and of the Council of June 8, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (EEE) - recast, unless otherwise specified as non-compliant.

Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.