Si9113 Demonstration Board

FEATURES

- ISDN-NT Input Voltage Range 28 V to 99 V
- Non-Polar Input
- 3.3-V/120-mA, 40-V/12-mA Outputs With Up To 80% Efficiency
- Up to 68% Efficiency at 80-mW Load
- 40 V Isolated By 3 kV From Input And 3.3-V Output – Si9113D1
- 3.3 V, 40 V Isolated By 1.5 kV From Input/Each Other – Si9113D2
- Current Mode Control, 0.6-V Fast Over-Current Protection
- Max 50% Duty Cycle Operation
- 1.3-MHz Error Amp
- Soft-Start
- <10-μA Supply Current for $+V_{IN}$ <18 V
- Programmed Start/Stop
- Internal Start-Up Circuit
- Power_Good Output

DESCRIPTION

As discussed in application note, AN728, the Si9113 power supply controller is an ideal choice for ISDN terminal equipment, where high efficiency at a low power level is one of most important criteria. Therefore, Vishay Siliconix has developed versions of a dual output flyback application demonstration boards, the Si9113D1 and the Si9113D2, which use different regulation schemes. These readily available demo boards are configured to deliver approximately 800 mW at 3.3-V, and40-V. These outputs and can be easily modified for other output voltages at approximately same power level. The flyback converters are designed to operate from a wide input voltage range of 28 V to 99 V and are polarity protected by a diode bridge. The Si9113D1 and Si9113D2, both operate at 20-kHz switching frequency to achieve the best possible efficiency. The transformer is selected to be slightly larger in this application so that the same area product would be good enough for an even lower window utilization factor (w.u.f.) transformer in order to meet the stringent requirements of clearance and creepage distances.

The Si9113D1 senses and tightly regulates the main output V_{OUT1} (3.3 V), which has the common ground as input and the secondary output V_{OUT2} (40 V) is regulated to within ± 10% at 10% to100% load range, including the set point accuracy. Correspondingly. the transformer must be specified with tight tolerance to achieve the given set point accuracy. The 40-V output is isolated from both the input and 3.3-V output by minimum 3 kV_{rms} isolation.

The Si9113D2 uses the auxiliary output (V_{CC} bootstrap winding) for sensing. Both V_{OUT1} (3.3 V) and V_{OUT2} (40 V) follow the auxiliary output, residing on one core and sharing the same flux. Both the outputs are isolated from the input as well as from each other by 1.5 kV and moderately regulated to ± 5%.

Each demonstration board uses all surface mount components except the high voltage electrolyte capacitor and are fully assembled and tested for quick evaluation. Test points are provided for the power_good signal and the closed loop response measurement.

Included in this document are the Bill-Of-Materials, Schematics, PCB Layout of the Demo Boards and actual waveforms/graphs.

The demonstration board layout is available in Gerber file format. Please contact your Vishay Siliconix sales representative or distributor for a copy.

ORDERING INFORMATION:

Si9113D1— V_{OUT1} (3.3 V) Tightly regulated, non-isolated
V_{OUT2} (40 V) Loosely regulated, 3 kV isolated

Si9113D2— V_{OUT1} (3.3 V) Moderately regulated, 1.5 kV isolated
V_{OUT2} (40 V) Moderately regulated, 1.5 kV isolated

POWER UP CHECK LIST AND OPERATION

The Si9113D1 and Si9113D2 are designed to operate in discontinuous mode at nominal line and load conditions. Both demo boards use the same operational procedure, as follows:

1 Visually inspect the PCB to be sure that all the components are intact and no foreign substance is lying on the board.

2 Solder the leads at C1 negative and MOSFET Q1 drain to monitor the drain waveform on the oscilloscope.

3 Reduce the source voltage to zero and connect it through the dc ammeter at V_{IN} + and V_{IN} –. Connect the dc voltmeter precisely across V_{IN} + and V_{IN} –. For the application where input is of fixed polarity, the diode bridge BR1 can be eliminated by shorting pin 1 to 4 and pin 2 to 3 to achieve even higher efficiency.

4 Connect the voltmeter precisely across V_{OUT1} – Com1 and V_{OUT2} – Com2 for the output voltage measurement. Connect the oscilloscope ground to C1 negative while the probe to Q1 drain to observe the switching waveforms.

5 Slowly increase the input voltage while monitoring the input current meter. Note the input current is less than 10 μA at 18 V_{IN} and continue to increase the voltage further till the circuit turns on at approximately 24 V.

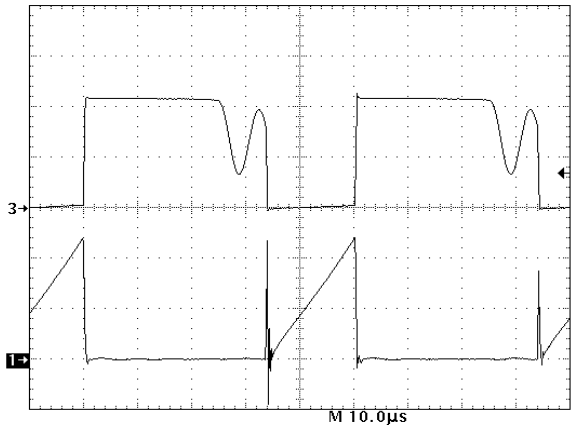
6 Set the input voltage to 48 V nominal and monitor the drain waveform, switching frequency, input and output ripple and noise.

7 The efficiency, line, load and cross regulation can be measured by varing the line between 28 to 99 V, and the load between 10% and 100%.

ACTUAL WAVEFORMS AND PERFORMANCE

Drain Voltage and Current

The circuit is designed to operate in discontinuous mode at nominal line and full load. The transformer is cleverly designed to reduce the leakage inductance. Refer to Figure 1 for the drain voltage and current waveforms. The current starting from zero indicates the discontinuous mode operation and absence of any leakage spike at drain shows the tight coupling between the windings.



V_{IN} = 28 V
Outputs – Full lLoad
Ch1 – Primary Current (0.1A/div)
Ch3 – Drain Voltage (20 V/div)

FIGURE 1. Drain Voltage and Current Waveform – Si9113D2

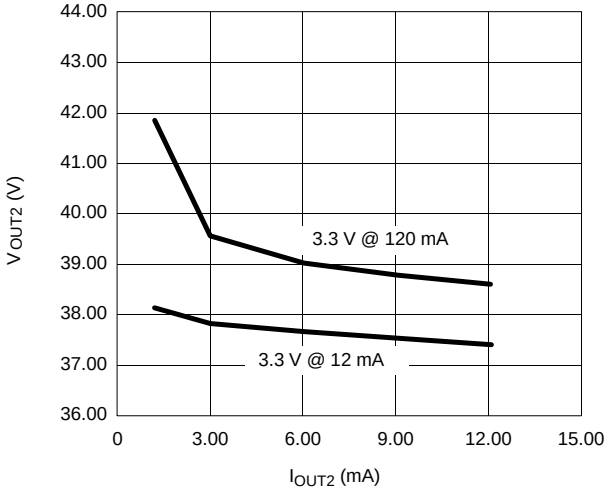


FIGURE 2. V_{OUT2} (40 V) Load/cross Regulation – Si9113D1

Output Regulation

The output regulation of slave outputs depend upon the loading condition of main output.

In Si9113D1, the V_{OUT1} (3.3 V) is tightly regulated to within 1%, while V_{OUT2} (40 V) follows the main output. Figure 2 depicts the typical load regulation of 40 V output, when the main output is at 10% and at full load condition.

In Si9113D2, the V_{OUT1} and V_{OUT2} are both moderately regulated. Figures 3 and 4 show the 3.3-V and 40-V regulation with the outputs loaded at 10% to100% of the rated load. The output voltages are essentially constant with respect to any variation of input voltage in case of both demo boards.

Output Ripple and Noise

The tantalum chip capacitors are used for lower ESR and higher ripple current capability. Low cost aluminium capacitors can also be used where form fator and/or output ripple are of secondary importance. Also, a small additional LC filter can be added at 3.3-V output for further attenuation of ac component by even five to ten times. The Si9113D1 – Figure 5 and Si9113D2 – Figure 6 show the ripple at a full load and 48-V input.

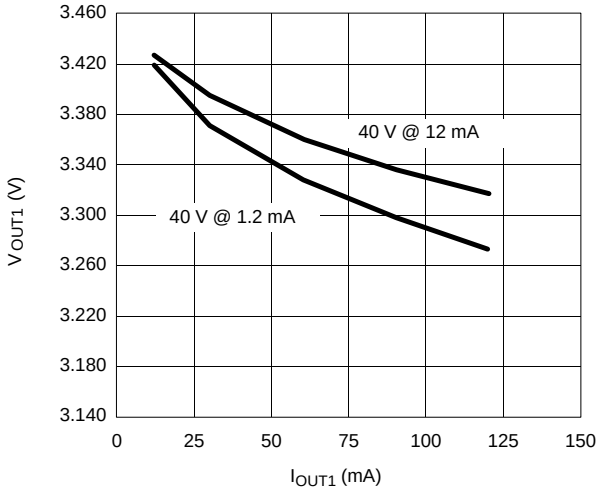


FIGURE 3. V_{OUT1} (3.3 V) Load/cross Regulation – Si9113D2

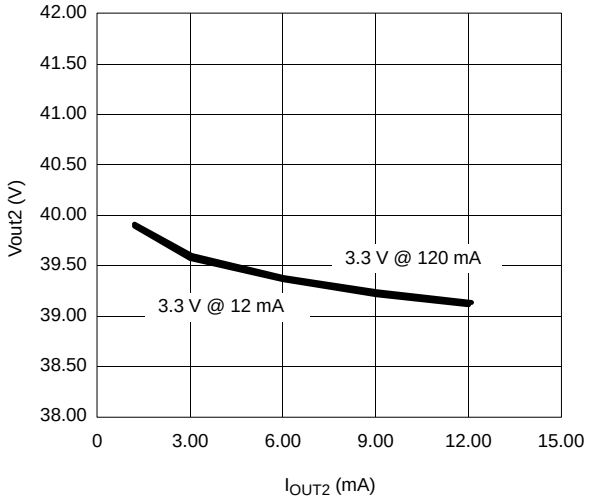
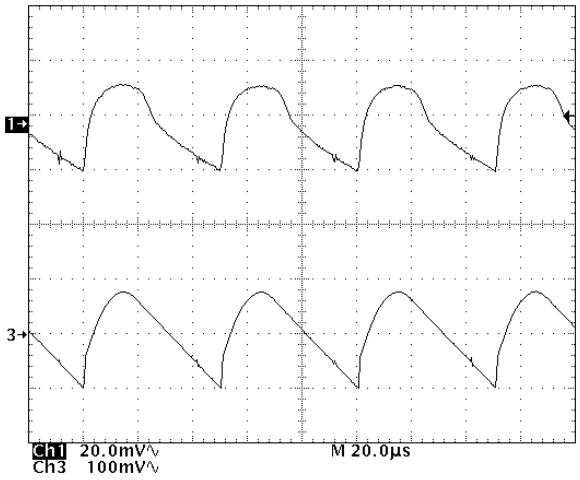
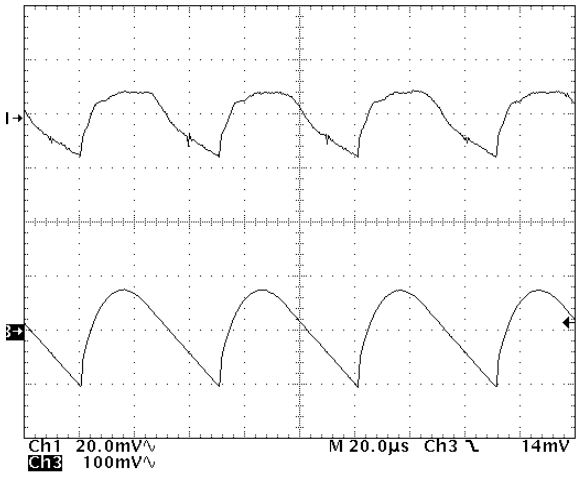


FIGURE 4. V_{OUT2} (40 V) Load/Cross Regulation – Si9113D2



V_{IN} = 48 V
Outputs = At Full Load
Ch1 = 3.3 V (20 mV/div))
Ch3 = 40 V (100 mV/div)

FIGURE 5. Output Ripple and Noise – Si9113D1



V_{IN} = 48 V
Outputs = At Full Load
Ch1 = 3.3 V (20 mV/div))
Ch3 = 40 V (100 mV/div)

FIGURE 6. Output Ripple and Noise – Si9113D2

EFFICIENCY

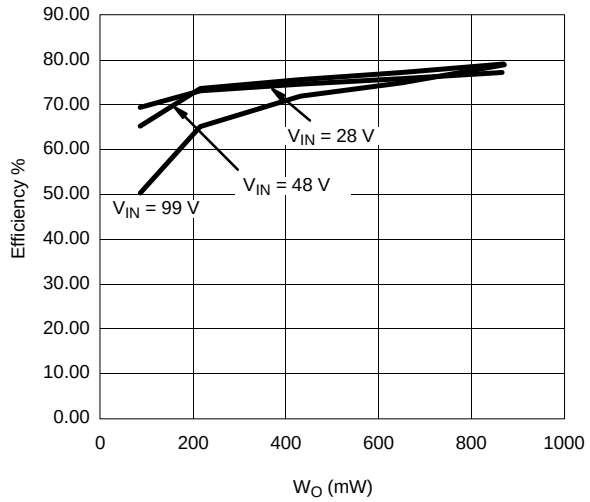


FIGURE 7. Converter Output Load vs Efficiency – Si9113D1

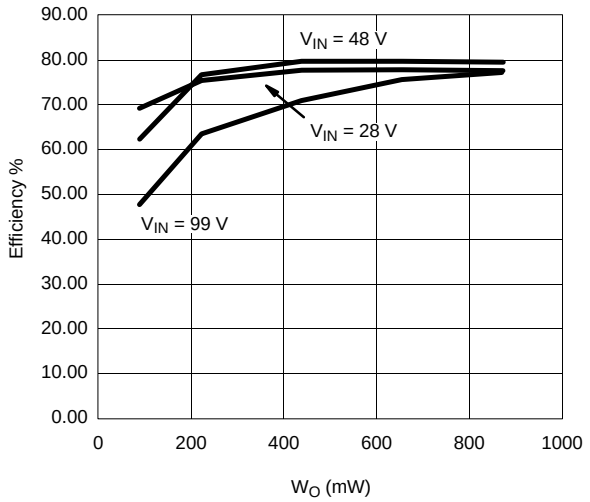


FIGURE 8. Converter Output Load vs Efficiency – Si9113D2

COMPENSATION

The closed loop response is observed at 48 V_{IN} and full load at both outputs on the venable by applying the error across R8 and measuring the gain, phase change encountered by the signal at both ends of R8. Refer to Figures 9 and 10 for the actual response.

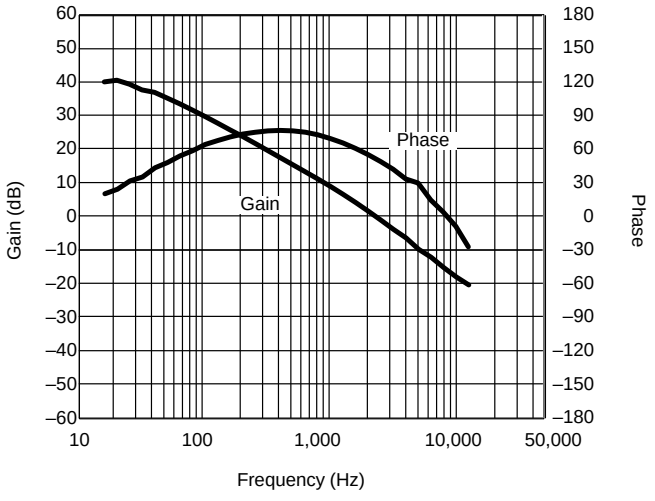


FIGURE 9. Measured Close Loop Response – Si9113D1

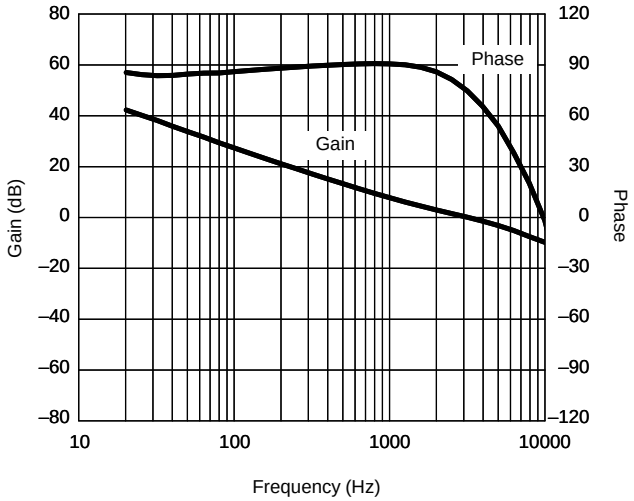
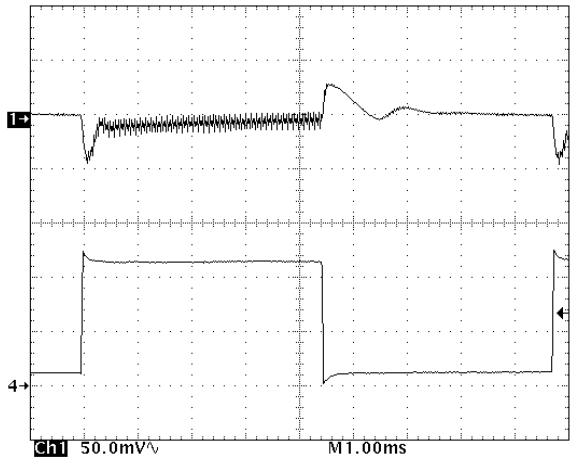


FIGURE 10. Measured Closed Loop Response–Si9113D2

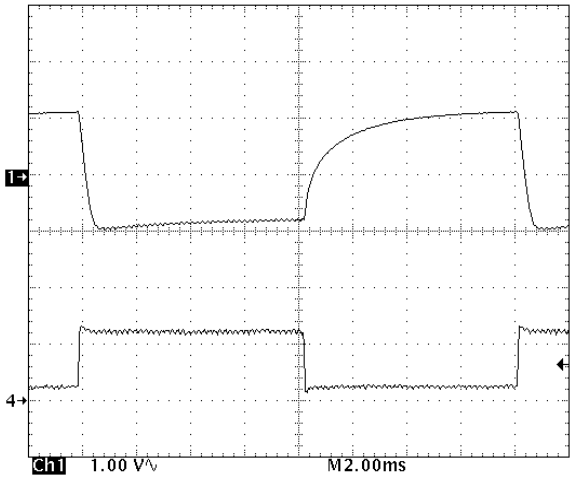
Dynamic Load Response

The step load is applied at 1A/µS slew rate at one output, while keeping the other output at rated load. Refer to Figures 11 through 14.



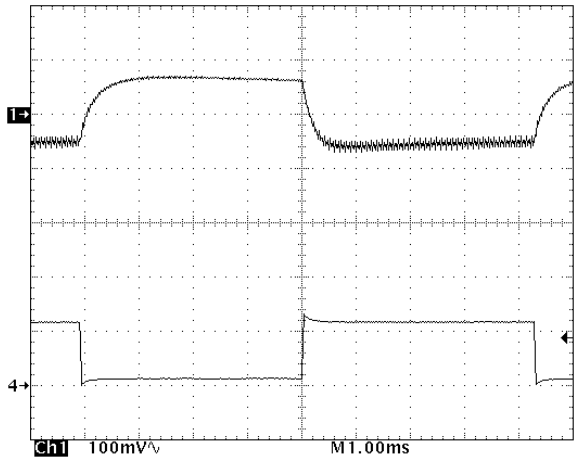
V_{IN} = 48 V
V_{OUT1} = Step –12 to 120 mA
Ch1 = V_{OUT1} (3.3 V)
Ch4 = Load (50 mA/div)
Slew Rate = 1A/µsec

FIGURE 11. V_{OUT1} (3.3 V) Transient Load Response – Si9113D1



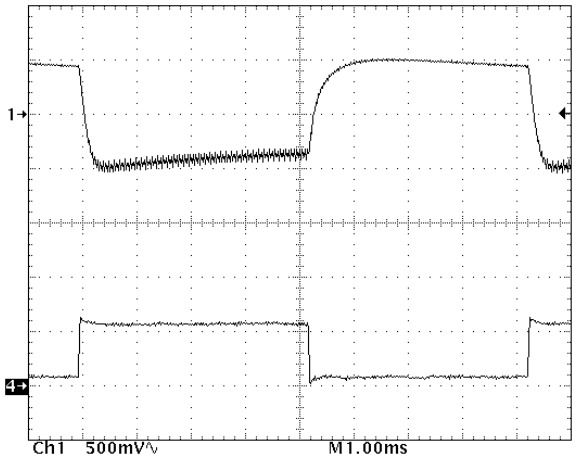
V_{IN} = 48 V
V_{OUT2} = Step Load 1.2 to 12 mA
V_{OUT1} = At Full Load
Ch1 = V_{OUT2} (40 V)
Ch4 = Load (10 mA/div)
Slew Rate = 1A/µsec

FIGURE 12. V_{OUT2} (40 V) Transient Load Response – Si9113D1



V_{IN} = 48 V
V_{OUT1} = Step Load 12 mA – 120 mA
V_{OUT2} = At Full Load
Ch1 = V_{OUT1} (3.3 V)
Ch4 = 100 mA/div
Slew Rate = 1A/µsec

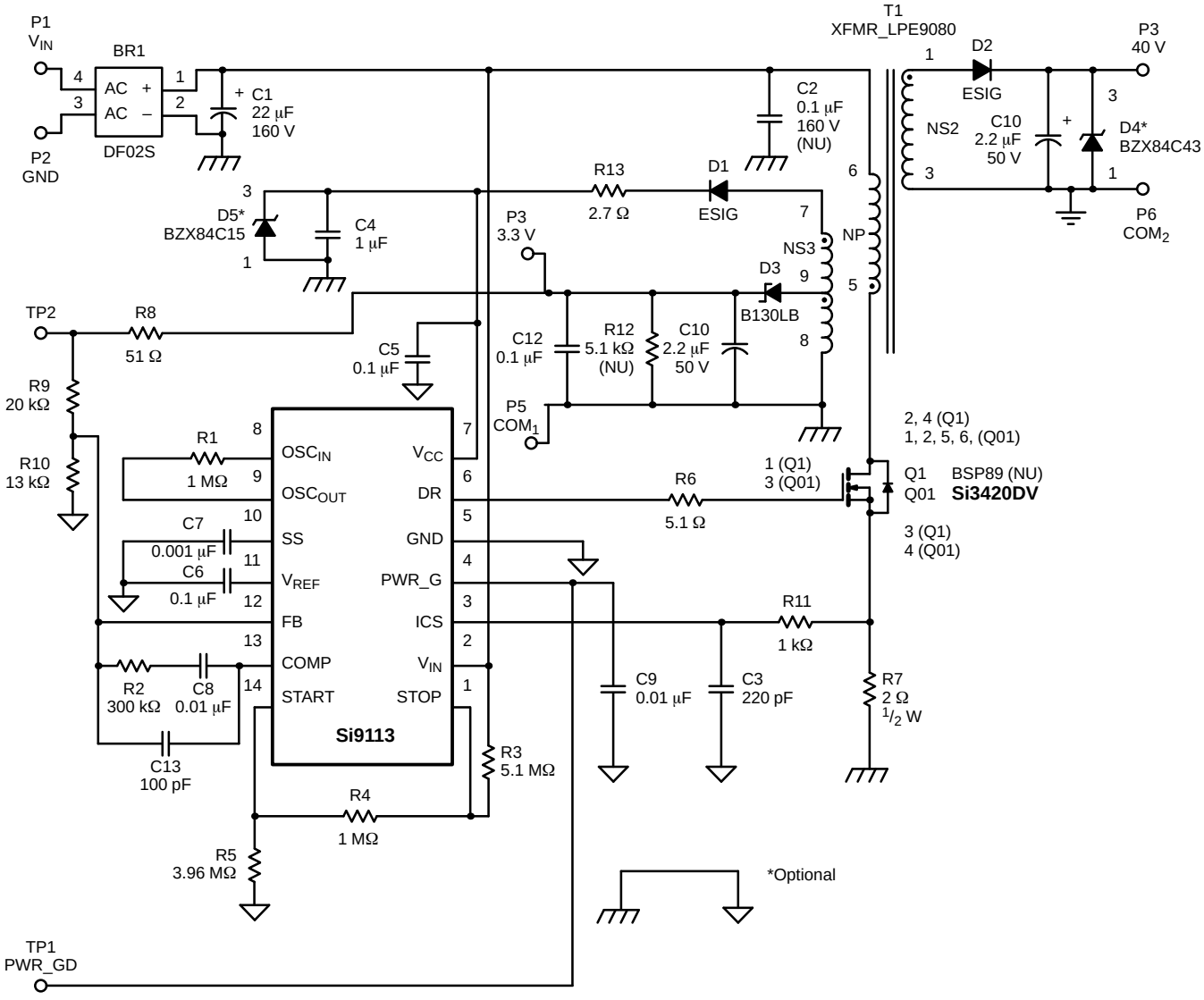
FIGURE 13. V_{OUT1} (3.3 V) Transient Load Response—Si9113D2



V_{IN} = 48 V
V_{OUT2} = Step Load 1.2 mA – 12 mA
V_{OUT1} = At Full Load
Ch1 = V_{OUT2} (40 V)
Ch4 = 10 mA/div
Slew Rate = 1A/µsec

FIGURE 14. V_{OUT2} (40 V) Transient Load Response—Si9113D2

SCHEMATIC, PCB LAYOUT AND BILL OF MATERIAL (SI9113D1)



Dual Output Flyback Converter with Tightly Regulated Main Output

FIGURE 15. Demo Board—Si9113D1

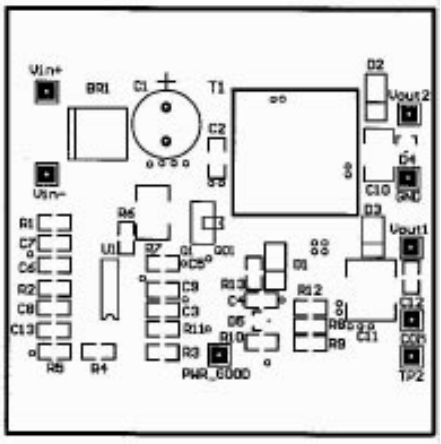


FIGURE 16. Silk Screen—Si9113D1

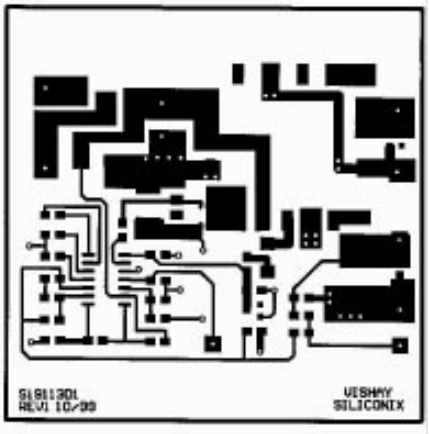


FIGURE 17. Top Layer—Si9113D1

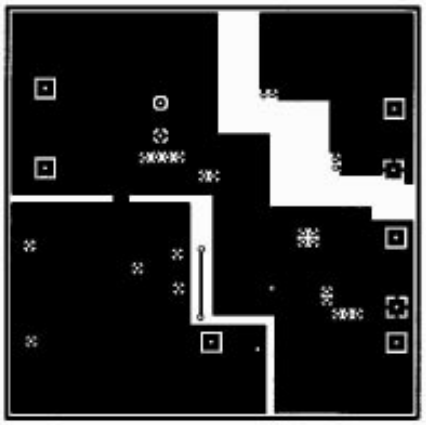


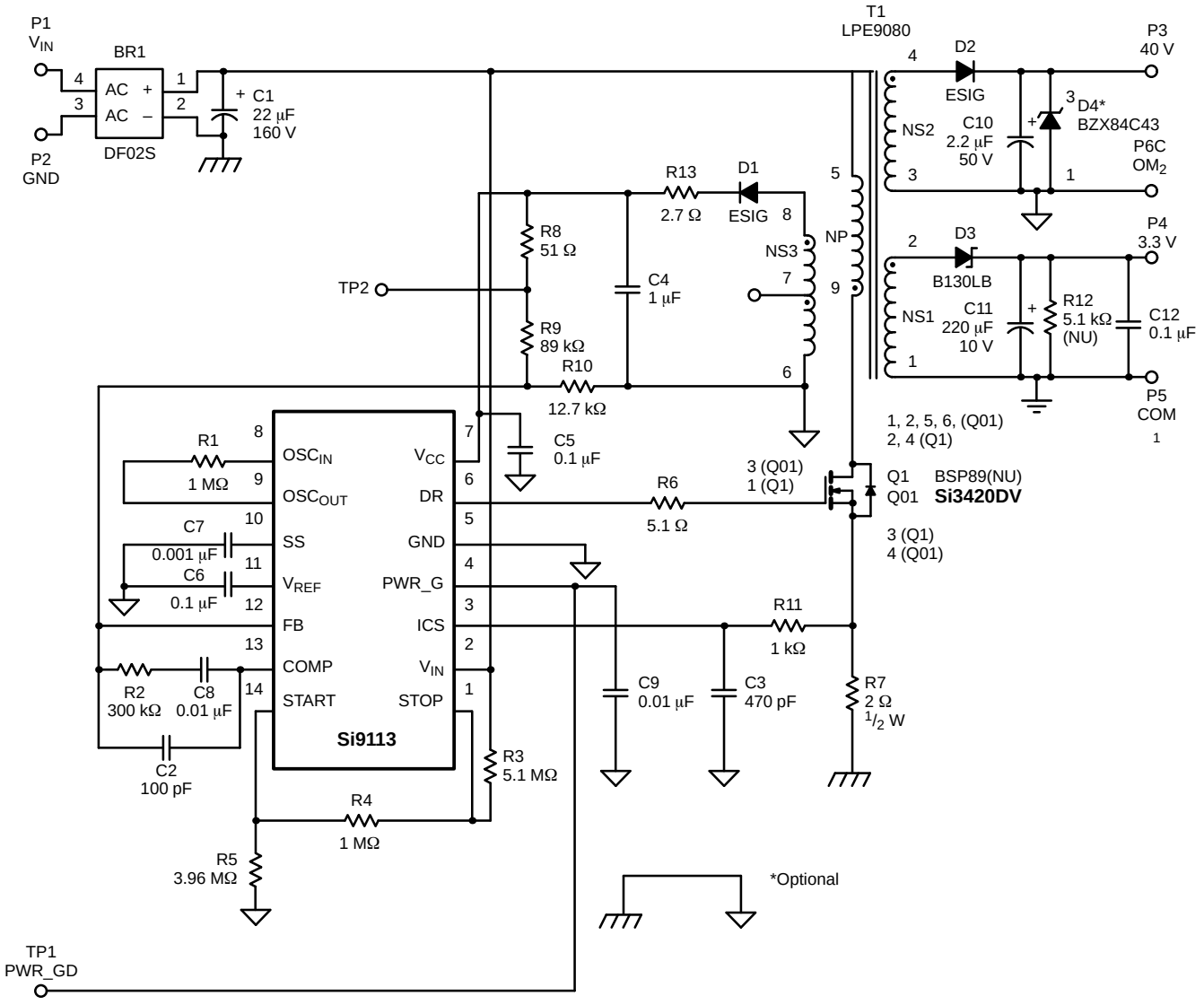
FIGURE 18. Bottom Layer—Si9113D1

TABLE 1. BILL-OF-MATERIALS—Si9113D1

Item	Qty	Designator	Part Type	Description	Footprint	Vendor Part #	Manufacturer
1	2	"R1, R4"	1 MΩ	"RES, 1%, 1/8 W"	0805	CRCW08051004FRT1	Vishay Dale
2	1	R2	300 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08053003FRT1	Vishay Dale
3	1	R3	5.1 MΩ	"RES, 1%, 1/8 W"	0805	CRCW08055104FRT1	Vishay Dale
4	1	R5	3.96 MΩ	RES, 1%, 1/8 W"	0805	CRCW08053964FRT1	Vishay Dale
5	1	R6	5.1 Ω	RES, 5%, 1/8 W"	0805	CRCW080551JRT1	Vishay Dale
6	1	R7	2 Ω	"RES, 1%, 1/2 W, PWR Metal"	2010	WSC-1/2	Vishay Dale
7	1	R8	51 Ω	"RES, 5%, 1/8 W"	0805	CRCW0805510JRT1	Vishay Dale
8	1	R9	20 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08052002FRT1	Vishay Dale
9	1	R10	13 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08051302FRT1	Vishay Dale
10	1	R11	1 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08051001FRT1	Vishay Dale
11	1	R12 (NU)	5.1 kΩ	"RES, 1%, 1/8 W (NU)"	0805	CRCW08055101FRT1	Vishay Dale
12	1	R13	2.7 Ω	"RES, 5%, 1/8 W"	0805	CRCW080527JRT1	Vishay Dale
13	1	C1	22 µF	"CAP, ELEC, 160 V, VR "	RB.2/.4	UVR2C220MEA	Nichicon
14	1	C2 (NU)	0.1 µF	"CAP, CER, 200 V"	1206	VJ1210Y104KXC	Vishay Vitramon
15	1	C3	220 pF	"CAP, CER"	0805	VJ0805Y221KXXAT	Vishay Vitramon
16	1	C4	1 µF	"CAP, CER, 25 V"	1210	VJ1210U105ZXAA	Vishay Vitramon
17	3	"C5, C6, C12"	0.1 µF	"CAP, CER"	0805	VJ0805Y104KXXAT	Vishay Vitramon
18	1	C7	0.001 µF	"CAP, CER"	0805	VJ0805Y102KXXAT	Vishay Vitramon
19	2	"C8, C9"	0.01 µF	"CAP, CER"	0805	VJ0805Y103KXXAT	Vishay Vitramon
20	1	C10	2.2 µF	"CAP, TAN, 50 V"	595D_C	595D225X0050C2T	Vishay Sprague
21	1	C11	220 µF	"CAP, TAN, 6.3 V"	594D_C	594D227X06R3C2T	Vishay Sprague
22	1	C13	100 pF	"CAP, CER"	0805	VJ0805Y101KXXAT	Vishay Vitramon
23	2	"D1, D2"	ES1G	"Diode, 1 A"	SMA	ES1G	Vishay Liteon
24	1	D3	B130LB	"Schottky Diode, 1 A"	SMB	B130LB	Vishay Liteon
25	1	D4*	BZX84C43	"Zener Diode, 41 V"	SOT-23	BZX84C43	Vishay Liteon
26	1	D5	BZX84C15	Zener Diode	SOT-23	BZX84C15	Vishay Dale
27	1	T1	LPE-9080-A413	Transformer	XFMR_LPE9080	LPE-9080-A413	Vishay Liteon
28	1	BR1	DF04S	Bridge		BR1	Vishay Liteon
29	1	Q1 (NU)	BSP89	N–Channel DMOSFET (NU)	SOT-223	BSP89	Philips Semiconductors
30	1	Q01	Si3420DV	N–Channel MOSFET	TSOP-6	Si3420DV	Vishay Siliconix
31	1	U1	Si9113	Power IC	SO–14	Si9113	Vishay Siliconix
32	2	"TP1, TP2"	Test Point	1-Pin Header	TP1		Multi-Source
33	6	P1 TO P6	"PWR, GND"	1-Pin Header	TP1		Multi-Source

*Optional

SCHEMATIC, PCB LAYOUT AND BILL OF MATERIAL (SI9113D2)



Dual Output Flyback Converter with Moderately Regulated Outputs

FIGURE 19. Demo Board—Si9113D2

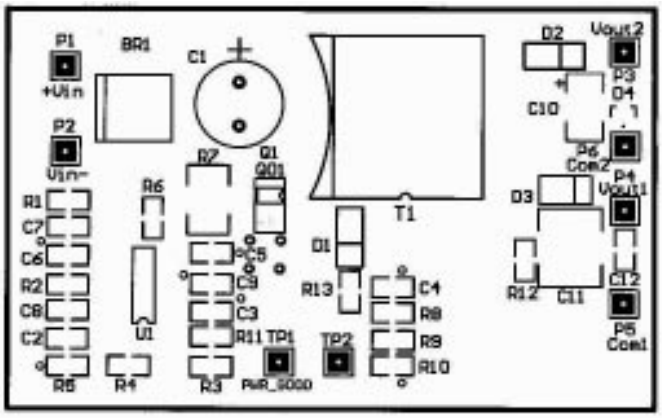


FIGURE 20. Silk Screen—Si9113D2

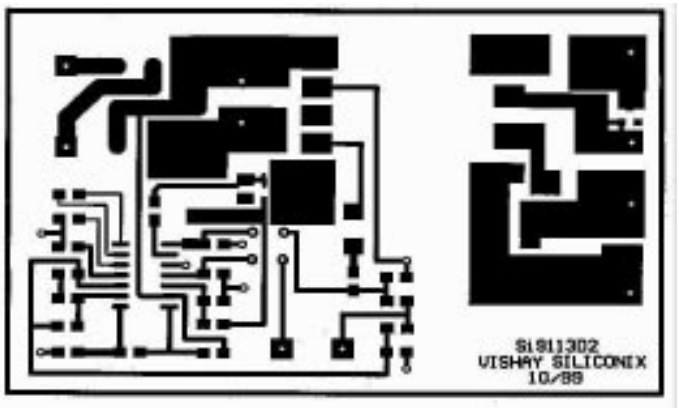


FIGURE 21. Top Layer—Si9113D2

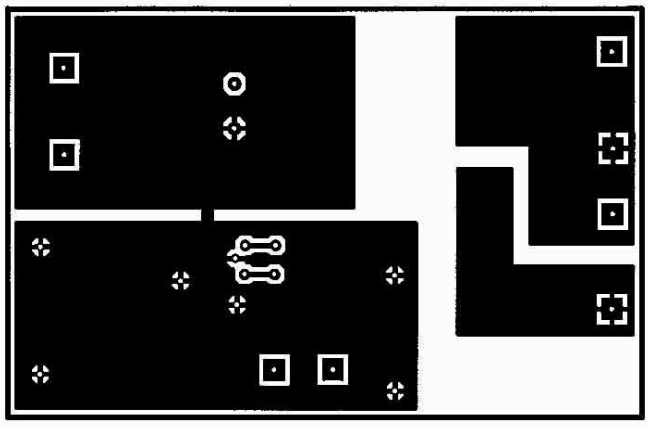


FIGURE 22. Bottom Layer—Si9113D2

TABLE 2. BILL-OF-MATERIALS—Si9113D2

Item	Qty	Designator	Part Type	Description	Footprint	Vendor Part #	Manufacturer
1	2	"R1, R4"	1 MΩ	"RES, 1%, 1/8 W"	0805	CRCW08051004FRT1	Vishay Dale
2	1	R2	300 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08053003FRT1	Vishay Dale
3	1	R3	5.1 MΩ	"RES, 1%, 1/8 W"	0805	CRCW08055104FRT1	Vishay Dale
4	1	R5	3.96 MΩ	"RES, 1%, 1/8 W"	0805	CRCW08053964FRT1	Vishay Dale
5	1	R6	5.1 Ω	"RES, 5%, 1/8 W"	0805	CRCW080551JRT1	Vishay Dale
6	1	R7	2 Ω	"RES, 1%, 1/2 W, PWR Metal"	2010	WSC-1/2	Vishay Dale
7	1	R8	51 Ω	"RES, 5%, 1/8 W"	0805	CRCW0805510JRT1	Vishay Dale
8	1	R9	89 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08058902FRT1	Vishay Dale
9	1	R10	12.7 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08051272FRT1	Vishay Dale
10	1	R11	1 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08051001FRT1	Vishay Dale
11	1	R12	5.1 kΩ	"RES, 1%, 1/8 W"	0805	CRCW08055101FRT1	Vishay Dale
12	1	R13	2.7 Ω	"RES, 5%, 1/8 W"	0805	CRCW080527JRT1	Vishay Dale
13	1	C1	22 μF	"CAP, ELEC, 160 V, VR"	RB.2/.4	UVR2C220MEA	Nichicon
14	1	C2	100 pF	"CAP, CER"	0805	VJ0805Y101KXXAT	Vishay Vitramon
15	1	C3	470 pF	"CAP, CER"	0805	VJ0805Y471KXXAT	Vishay Vitramon
16	1	C4	1 μF	"CAP, CER, 25 V"	1210	VJ1210U105ZXAA	Vishay Vitramon
17	3	"C5, C6, C12"	0.1 μF	"CAP, CER"	0805	VJ0805Y104KXXAT	Vishay Vitramon
18	1	C7	0.001 μF	"CAP, CER"	0805	VJ0805Y102KXXAT	Vishay Vitramon
19	2	"C8, C9"	0.01 μF	"CAP, CER"	0805	VJ0805Y103KXXAT	Vishay Vitramon
20	1	C10	2.2 μF	"CAP, TAN, 50 V"	595D_C	595D225X0050C2T	Vishay Sprague
21	1	C11	220 μF	"CAP, TAN, 6.3 V"	594D_C	594D227X06R3C2T	Vishay Sprague
22	2	"D1, D2"	ES1G	"Diode, 1 A"	SMA	ES1G	Vishay Liteon
23	1	D3	B130LB	"Schottky Diode, 1 A"	SMB	B130LB	Vishay Liteon
24	1	D4*	BZX84C43	"Zener Diode, 41 V"	SOT–23	BZX84C43	Vishay Liteon
25	1	T1	LPE-9080-A414	Transformer	XFMR_LPE9080	LPE-9080-A414	Vishay Dale
26	1	BR1	DF04S	Bridge		BR1	Vishay Liteon
27	1	Q1 (NU)	BSP89	N–Channel DMOSFET (NU)	SOT-223	BSP89	Philips Semicoductors
28	1	Q01	Si3420DV	N–Channel MOSFET	TSOP-6	Si2320DS	Vishay Siliconix
29	1	U1	Si9113	Power IC	SO-14	Si9113	Vishay Siliconix
30	2	"TP1, TP2"	Test Point	1-Pin Header	TP1		Multi-Source
31	6	P1 TO P6	"PWR, GND"	1-Pin Header	TP1		Multi-Source

*Optional