

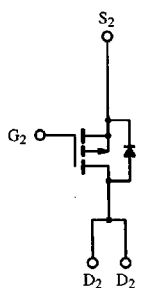
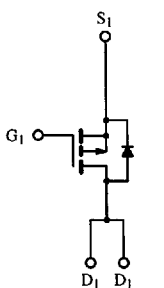
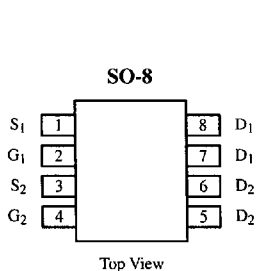
Dual P-Channel Enhancement-Mode MOSFET

Product Summary

V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A)
-20	0.11 @ V _{GS} = -4.5 V	± 3.4
	0.15 @ V _{GS} = -3.0 V	± 2.9
	0.19 @ V _{GS} = -2.7 V	± 2.6

Recommended upgrade: Si9934DY

Lower profile/smaller size—see LITE FOOT® equivalent: Si6943DQ



Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	-20	V	
Gate-Source Voltage	V _{GS}	± 12		
Continuous Drain Current (T _J = 150°C) ^a	I _D	T _A = 25°C	± 3.4	A
		T _A = 70°C	± 2.7	
Pulsed Drain Current	I _{DM}	± 8		
Continuous Source Current (Diode Conduction) ^a	I _S	-2.0		
Maximum Power Dissipation ^a	P _D	T _A = 25°C	2.0	W
		T _A = 70°C	1.3	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C	

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1209. A SPICE Model data sheet is available for this product (FaxBack document #5121).

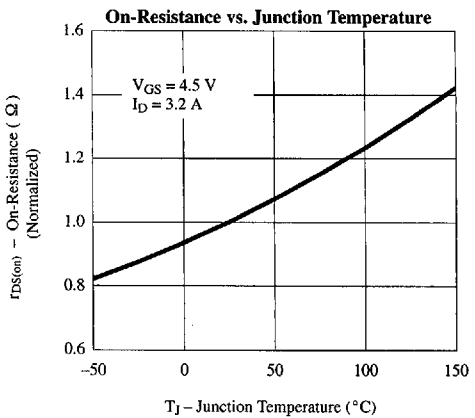
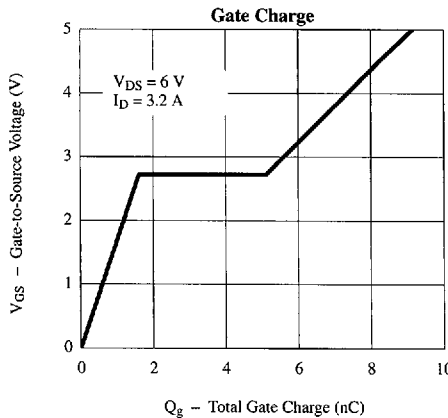
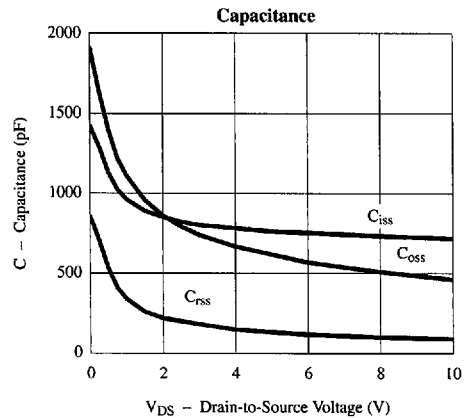
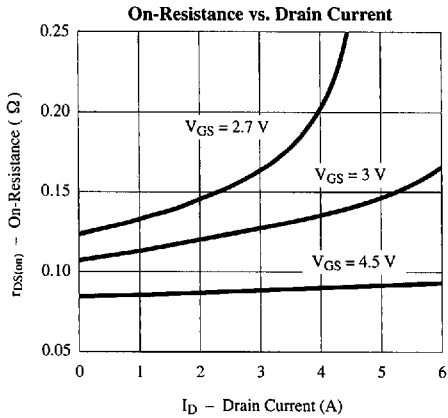
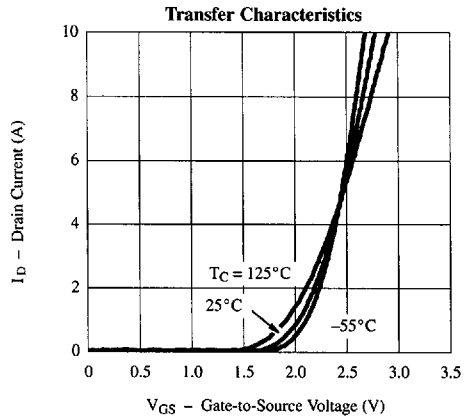
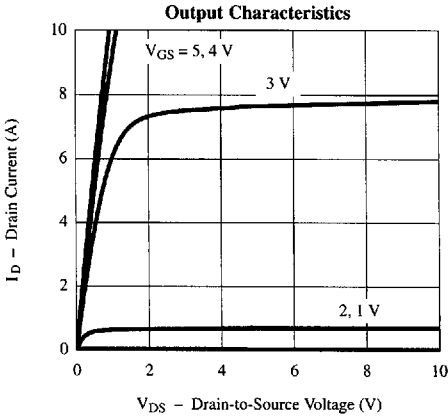
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-0.8			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$			-3	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} \leq -5 \text{ V}, V_{GS} = -4.5 \text{ V}$	-8			A
		$V_{DS} \leq -5 \text{ V}, V_{GS} = -2.7 \text{ V}$	-2			
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = -4.5 \text{ V}, I_D = -3.2 \text{ A}$		0.09	0.11	Ω
		$V_{GS} = -3.0 \text{ V}, I_D = -2.0 \text{ A}$		0.120	0.15	
		$V_{GS} = -2.7 \text{ V}, I_D = -1 \text{ A}$		0.135	0.19	
Forward Transconductance ^b	g_{fs}	$V_{DS} = -9 \text{ V}, I_D = -3.4 \text{ A}$		8		S
Diode Forward Voltage ^b	V_{SD}	$I_S = -2.0 \text{ A}, V_{GS} = 0 \text{ V}$		-0.9	-1.2	V
Dynamic^a						
Total Gate Charge	Q_g	$V_{DS} = -6 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -3.2 \text{ A}$		8	20	nC
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			3.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6 \text{ V}, R_L = 6 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_G = 6 \Omega$		22	40	ns
Rise Time	t_r			43	80	
Turn-Off Delay Time	$t_{d(off)}$			35	70	
Fall Time	t_f			20	40	
Source-Drain Reverse Recovery Time	t_{rr}		$I_F = -2.0 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		75	

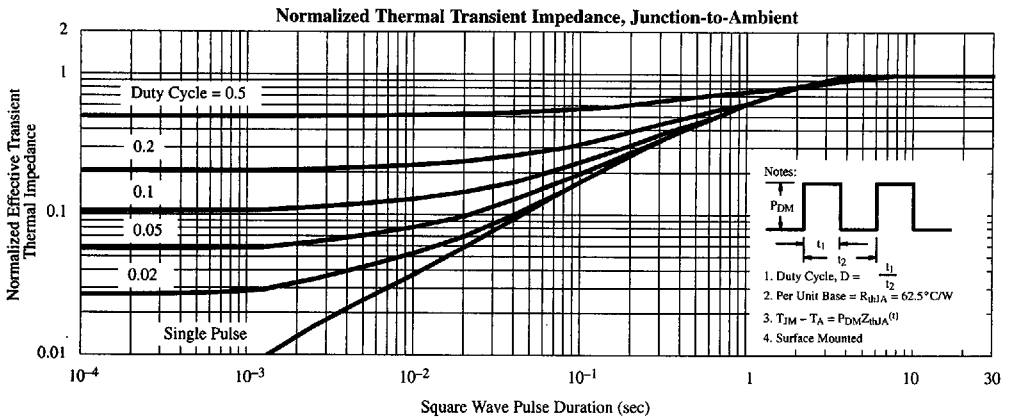
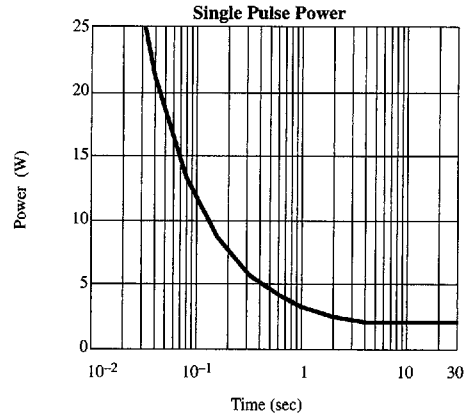
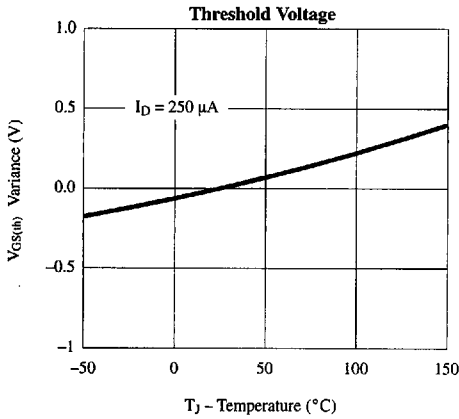
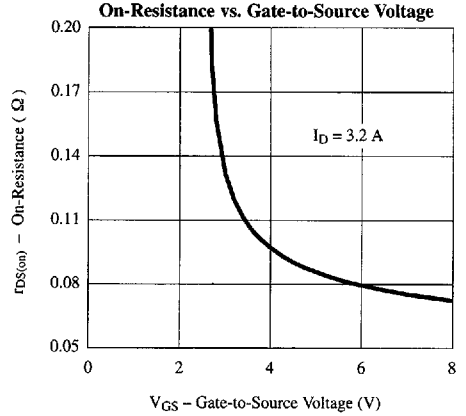
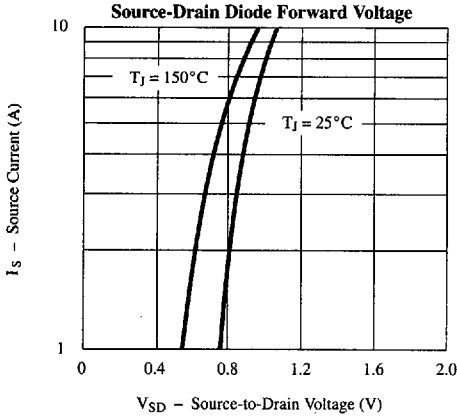
Notes

- a. For design aid only; not subject to production testing.
 b. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

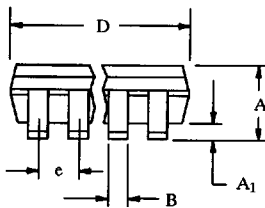
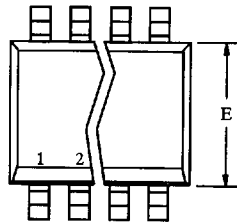
Typical Characteristics (25°C Unless Otherwise Noted)



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SO Package (Y Suffix), 8-16 Leads



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A ₁	0.10	0.20	0.004	0.008
B	0.35	0.45	0.014	0.018
C	0.18	0.23	0.007	0.009
D-8	4.60	5.20	0.181	0.205
D-14	8.35	8.95	0.329	0.352
D-16	9.60	10.20	0.378	0.402
E	3.55	4.05	0.140	0.160
e	1.27 BSC		0.050 BSC	
H	5.70	6.30	0.224	0.248
L	0.60	0.80	0.024	0.031
Θ	0°	8°	0°	8°

