SIGC156T120R2CL

IGBT Chip in NPT-technology

FEATURES:

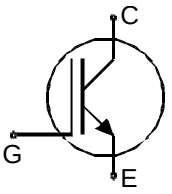
- 1200V NPT technology
- 180µm chip
- low turn-off losses
- positive temperature coefficient
- easy paralleling
- integrated gate resistor

This chip is used for:

- power module BSM100GD120DLC

Applications:

- drives



Chip Type	V_{CE}	I_{Cn}	Die Size	Package	Ordering Code
SIGC156T120R2CL	1200V	100A	12.59 X 12.59 mm^2	sawn on foil	Q67041-A4663-A003

MECHANICAL PARAMETER:

Raster size	12.59 X 12.59	mm^2
Emitter pad size	8 x (3.98 x 2.38)	
Gate pad size	1.46 x 0.8	
Area total / active	158.5 / 132.6	
Thickness	180	µm
Wafer size	150	mm
Flat position	90	grd
Max.possible chips per wafer	82 pcs	
Passivation frontside	Photoimide	
Emitter metallization	3200 nm Al Si 1%	
Collector metallization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	electrically conductive glue or solder	
Wire bond	Al, <500µm	
Reject Ink Dot Size	∅ 0.65mm ; max 1.2mm	
Recommended Storage Environment	store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	

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MAXIMUM RATINGS:

Parameter	Symbol	Value	Unit
Collector-emitter voltage, T_j=25 °C	V_{CE}	1200	V
DC collector current, limited by T_{jmax}	I_C	1)	A
Pulsed collector current, t_p limited by T_{jmax}	I_{cpuls}	300	A
Gate emitter voltage	V_{GE}	±20	V
Operating junction and storage temperature	T_j, T_{stg}	-55 ... +150	°C

1) depending on thermal properties of assembly

STATIC CHARACTERISTICS (tested on chip), T_j=25 °C, unless otherwise specified:

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	V_{GE}=0V , I_C=5mA	1200			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	V_{GE}=15V, I_C=100A	1.8	2.2	2.6	
Gate-emitter threshold voltage	$V_{GE(th)}$	I_C=4mA , V_{GE}=V_{CE}	4.5	5.5	6.5	
Zero gate voltage collector current	I_{CES}	V_{CE}=1200V , V_{GE}=0V			12.2	µA
Gate-emitter leakage current	I_{GES}	V_{CE}=0V , V_{GE}=20V			600	nA
Integrated gate resistor	R_{Gint}			5		Ω

ELECTRICAL CHARACTERISTICS (tested at component):

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	V_{CE}=25V,	-	6.5	-	nF
Output capacitance	C_{oss}	V_{GE}=0V,	-	-	-	
Reverse transfer capacitance	C_{rss}	f=1MHz	-	0.42	-	

SWITCHING CHARACTERISTICS (tested at component), Inductive Load

Parameter	Symbol	Conditions 1)	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	T_j=125°C	-	60	-	ns
Rise time	t_r	V_{CC}=600V,	-	50	-	
Turn-off delay time	$t_{d(off)}$	I_C=100A, V_{GE}=±15V,	-	400	-	
Fall time	t_f	R_G=5.6Ω	-	80	-	

1) values also influenced by parasitic L- and C- in measurement and package.

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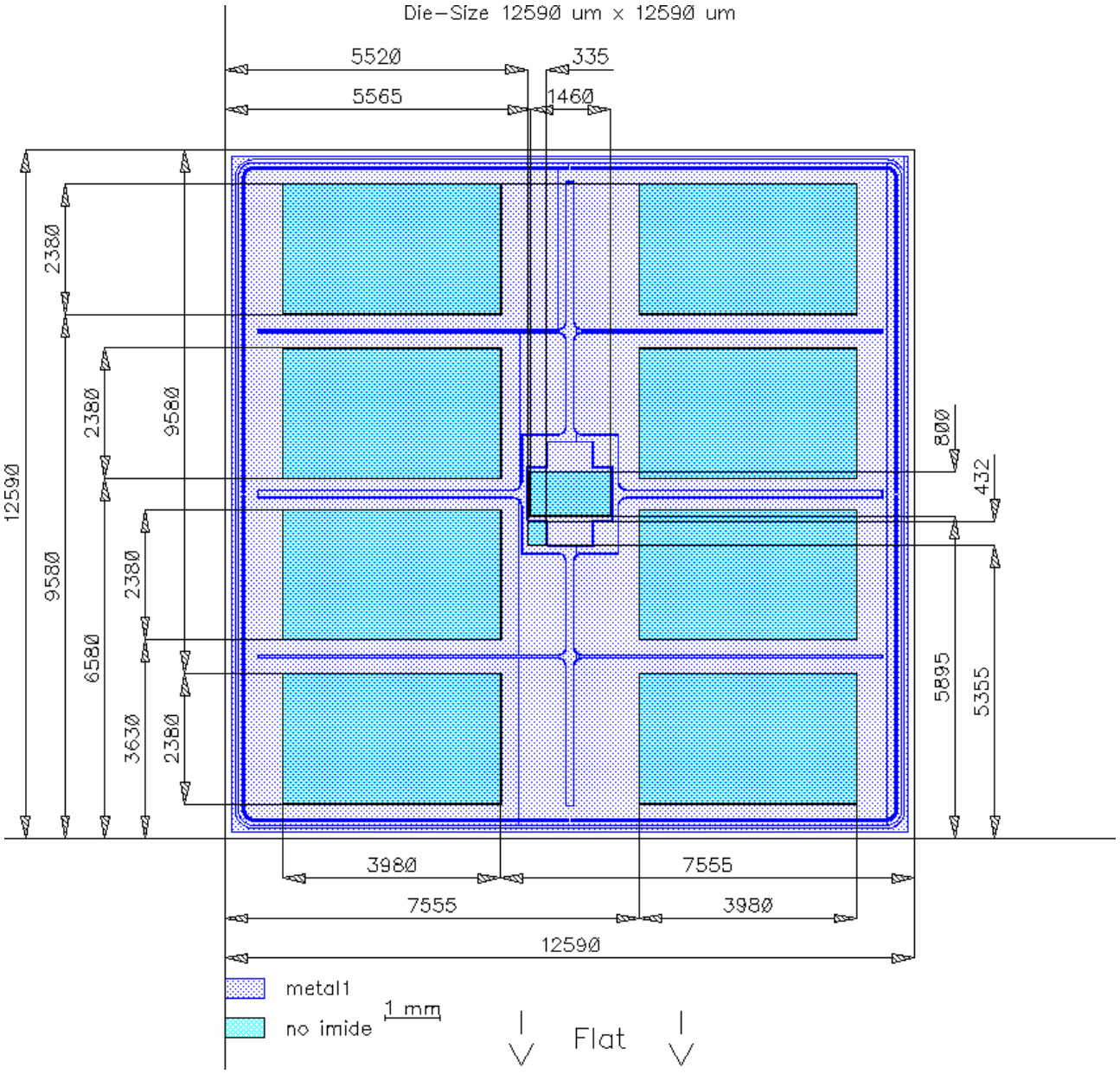
CHIP DRAWING:



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FURTHER ELECTRICAL CHARACTERISTICS:

This chip data sheet refers to the device data sheet	BSM100GD120DLC	Package Econopack 3

DESCRIPTION:

AQL 0,65 for visual inspection according to failure catalog

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Test-Normen Villach/Prüffeld

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