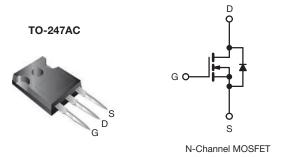
Vishay Siliconix

E Series Power MOSFET with Fast Body Diode and Low Gate Charge

PRODUCT SUMMARY				
V _{DS} (V) at T _J max.	650			
R _{DS(on)} typ. (Ω) at 25 °C	V _{GS} = 10 V	0.127		
Q _g (Max.) (nC)	75			
Q _{gs} (nC)	17			
Q _{gd} (nC)	19			
Configuration	Single			



FEATURES

- Reduced figure-of-merit (FOM): Ron x Qa
- Fast body diode MOSFET using E series technology



- Reduced t_{rr}, Q_{rr}, and I_{RRM}
- Increased robustness due to low Q_{rr}
- Low input capacitance (C_{iss})
- · Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

APPLICATIONS

- Telecommunications
 - Server and telecom power supplies
- Computing
 - ATX power supplies
- Industrial
 - Welding
 - Induction heating
 - Battery chargers
 - Uninterruptible power supplies (UPS)
- · Renewable energy
 - String PV inverters

ORDERING INFORMATION	
Package	TO-247AC
Lead (Pb)-free and Halogen-free	SiHG25N60EFL-GE3

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	600	V	
Gate-Source Voltage			V_{GS}	± 30	v	
Continuous Drain Current (T _J = 150 °C)	\/ at 10.\/	T _C = 25 °C T _C = 100 °C		25		
	V _{GS} at 10 V	T _C = 100 °C	ID	16	Α	
Pulsed Drain Current ^a			I _{DM}	61		
Linear Derating Factor				2	W/°C	
Single Pulse Avalanche Energy b			E _{AS}	353	mJ	
Maximum Power Dissipation			P _D	250	W	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	$V_{DS} = 0 \text{ V to } 80 \% V_{DS}$		dV/dt	70	1//20	
Reverse Diode dV/dt d		uv/ui	15	- V/ns		
Soldering Recommendations (Peak temperature) c	for 10 s			300	°C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
- b. V_{DD} = 140 V, starting T_J = 25 °C, L = 28.2 mH, R_g = 25 Ω , I_{AS} = 5 A.
- c. 1.6 mm from case.
- d. $I_{SD} \le I_D$, dI/dt = 100 A/ μ s, starting $T_J = 25$ °C.



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THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	62	°C/W	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.5	C/VV	

PARAMETER	SYMBOL	TES	T CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static					Į.		
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	600	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	e to 25 °C, I _D = 10 mA	1	0.69	-	V/°C
Gate-Source Threshold Voltage (N)	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	3.0	-	5.0	V
Coto Courso Logicoro		$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 30 V		-	± 1	μΑ
Zava Cata Valtaga Dvain Cuwant		V _{DS} =	= 480 V, V _{GS} = 0 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 480 \	V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	500	μΑ
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 12.5 A	-	0.127	0.146	Ω
Forward Transconductance	9 _{fs}	V _{DS} = 30 V, I _D = 12.5 A		-	11.3	-	S
Dynamic							
Input Capacitance	C _{iss}	$V_{GS} = 0 \text{ V},$ $V_{DS} = 100 \text{ V},$ $f = 1 \text{ MHz}$		1	2274	-	pF
Output Capacitance	C _{oss}			-	137	-	
Reverse Transfer Capacitance	C _{rss}			=	4	-	
Effective Output Capacitance, Energy Related ^a	C _{o(er)}	$V_{DS} = 0 \text{ V to } 480 \text{ V}, V_{GS} = 0 \text{ V}$		-	79	-	
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	330	-	
Total Gate Charge	Qg			-	50	75	
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 12.5 \text{ A}, V_{DS} = 480 \text{ V}$		17	-	nC
Gate-Drain Charge	Q _{gd}			-	19	-	1
Turn-On Delay Time	t _{d(on)}			1	25	50	
Rise Time	t _r	V _{DD} = 480 V, I _D = 12.5 A,		-	39	68	ns
Turn-Off Delay Time	t _{d(off)}	$R_g = 1$	$R_g = 9.1 \Omega, V_{GS} = 10 V$		47	94	
Fall Time	t _f	1		-	21	42	
Gate Input Resistance	R _g	f = 1 MHz, open drain		0.4	0.7	1.4	Ω
Drain-Source Body Diode Characteristic	S						•
Continuous Source-Drain Diode Current	I _S	MOSFET symi	MOSFET symbol showing the		-	25	
Pulsed Diode Forward Current	I _{SM}	integral reverse p - n junction diode		-	-	61	A
Diode Forward Voltage	V _{SD}	$T_J = 25 ^{\circ}\text{C}, I_S = 12.5 \text{A}, V_{GS} = 0 \text{V}$		-	0.9	1.2	V
Reverse Recovery Time	t _{rr}				138	276	ns
Reverse Recovery Charge	Q _{rr}	$T_J = 25$ °C, $I_F = I_S = 12.5$ A, $dI/dt = 100$ A/ μ s, $V_R = 25$ V		-	0.8	1.6	μC
Reverse Recovery Current	I _{RRM}			_	11	_	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

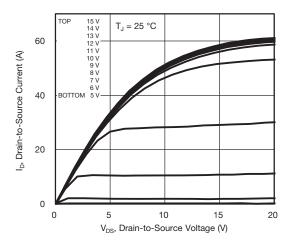


Fig. 1 - Typical Output Characteristics

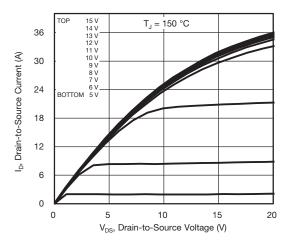


Fig. 2 - Typical Output Characteristics

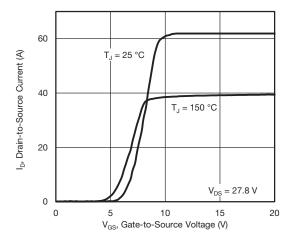


Fig. 3 - Typical Transfer Characteristics

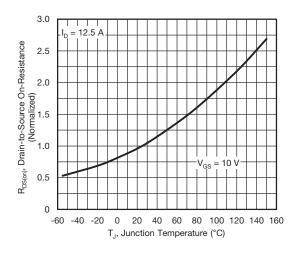


Fig. 4 - Normalized On-Resistance vs. Temperature

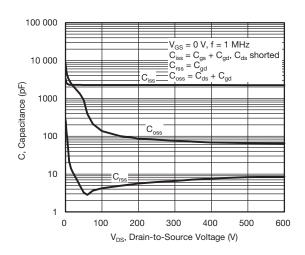


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

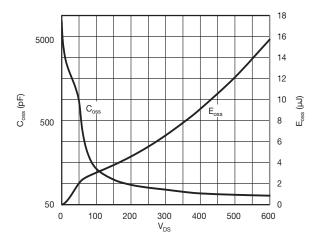


Fig. 6 - C_{OSS} and E_{OSS} vs. V_{DS}



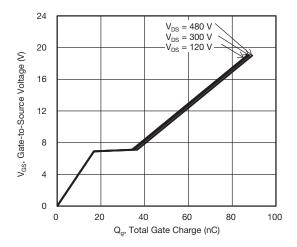


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

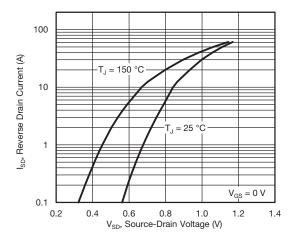


Fig. 8 - Typical Source-Drain Diode Forward Voltage

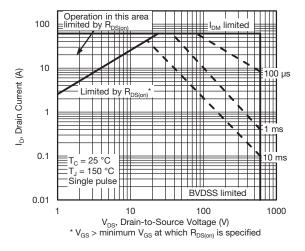


Fig. 9 - Maximum Safe Operating Area

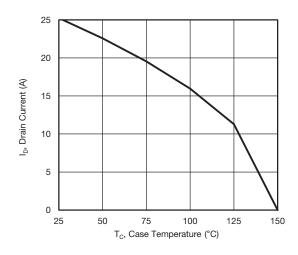


Fig. 10 - Maximum Drain Current vs. Case Temperature

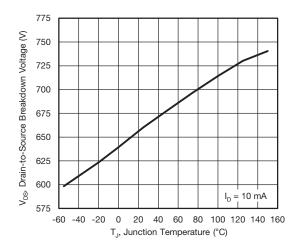


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature



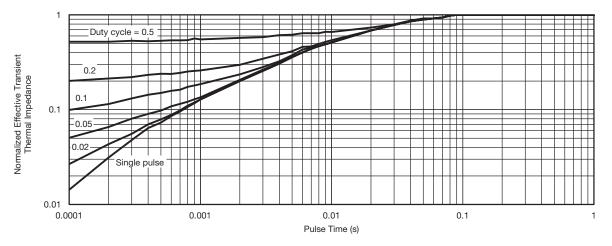


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

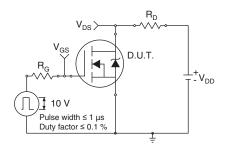


Fig. 13 - Switching Time Test Circuit

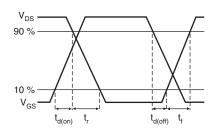


Fig. 14 - Switching Time Waveforms

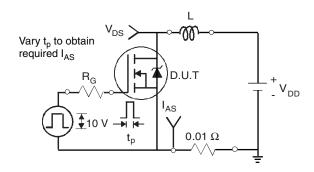


Fig. 15 - Unclamped Inductive Test Circuit

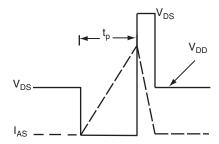


Fig. 16 - Unclamped Inductive Waveforms

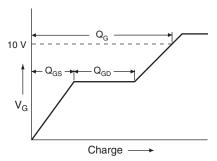


Fig. 17 - Basic Gate Charge Waveform

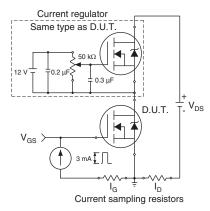
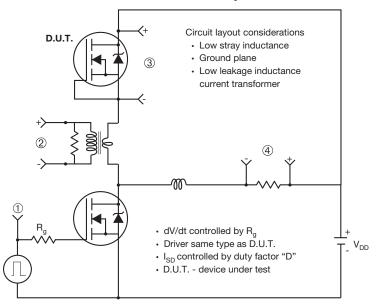


Fig. 18 - Gate Charge Test Circuit



Peak Diode Recovery dV/dt Test Circuit



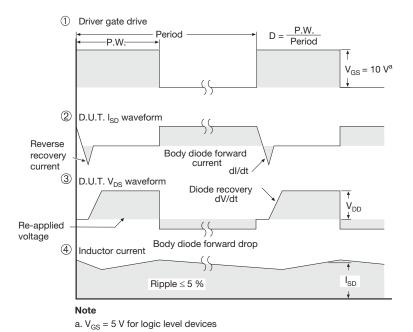


Fig. 19 - For N-Channel

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