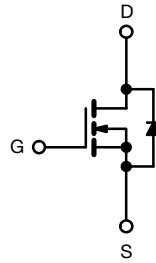
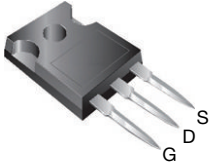


## E Series Power MOSFET

TO-247AC



N-Channel MOSFET

### FEATURES

- Low figure-of-merit (FOM)  $R_{on} \times Q_g$
- Low input capacitance ( $C_{iss}$ )
- Reduced switching and conduction losses
- Ultra low gate charge ( $Q_g$ )
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
Available

### APPLICATIONS

- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
  - High-intensity discharge (HID)
  - Fluorescent ballast lighting
- Industrial
  - Welding
  - Induction heating
  - Motor drives
  - Battery chargers
  - Renewable energy
  - Solar (PV inverters)

### PRODUCT SUMMARY

$V_{DS}$ (V) at $T_J$ max.	650	
$R_{DS(on)}$ max. ( $\Omega$ ) at 25 °C	$V_{GS} = 10$ V	0.064
$Q_g$ max. (nC)	220	
$Q_{gs}$ (nC)	29	
$Q_{gd}$ (nC)	57	
Configuration	Single	

### ORDERING INFORMATION

Package	TO-247AC
Lead (Pb)-free	SiHG47N60E-E3
Lead (Pb)-free and halogen-free	SiHG47N60E-GE3


### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	$V_{DS}$	600	V
Gate-source voltage	$V_{GS}$	$\pm 30$	
Continuous drain current ( $T_J = 150$ °C)	$V_{GS}$ at 10 V	$T_C = 25$ °C	A
		$T_C = 100$ °C	
Pulsed drain current <sup>a</sup>	$I_{DM}$	145	
Linear derating factor		3	W/°C
Single pulse avalanche energy <sup>b</sup>	$E_{AS}$	1800	mJ
Maximum power dissipation	$P_D$	357	W
Operating junction and storage temperature range	$T_J, T_{stg}$	-55 to +150	°C
Drain-source voltage slope	$dV/dt$	$V_{DS} = 0$ V to 80 % $V_{DS}$	V/ns
Reverse diode $dV/dt$ <sup>d</sup>		11	
Soldering recommendations (peak temperature) <sup>c</sup>	for 10 s	300	°C

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 50$  V, starting  $T_J = 25$  °C,  $L = 73.5$  mH,  $R_g = 25$   $\Omega$ ,  $I_{AS} = 7$  A
- 1.6 mm from case
- $I_{SD} \leq I_D$ ,  $dI/dt = 100$  A/ $\mu$ s, starting  $T_J = 25$  °C

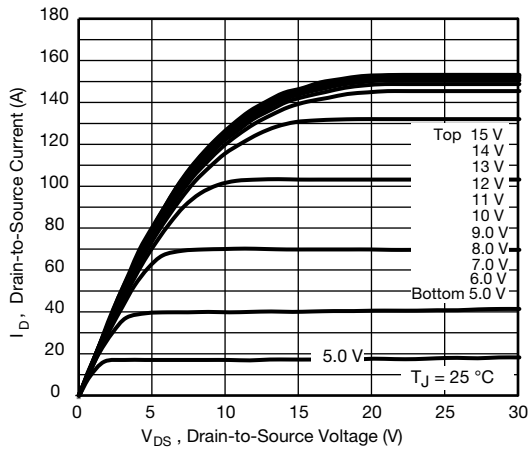
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	$R_{thJA}$	-	40	°C/W
Maximum junction-to-case (drain)	$R_{thJC}$	-	0.33	

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 250\text{ }\mu\text{A}$		-	0.66	-	V/°C
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2	-	4	V
Gate-source leakage	$I_{GSS}$	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
		$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 1$	$\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	10	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 24\text{ A}$	-	0.053	0.064	$\Omega$
Forward transconductance	$g_{fs}$	$V_{DS} = 8\text{ V}, I_D = 3\text{ A}$		-	6.8	-	S
<b>Dynamic</b>							
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$		2405	4810	9620	pF
Output capacitance	$C_{oss}$			115	230	460	
Reverse transfer capacitance	$C_{rss}$			1.7	5	10	
Effective output capacitance, energy related <sup>a</sup>	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 480\text{ V}, V_{GS} = 0\text{ V}$		-	170	-	pF
Effective output capacitance, time related <sup>b</sup>	$C_{o(tr)}$			-	604	-	
Total gate charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 24\text{ A}, V_{DS} = 480\text{ V}$	74	148	220	nC
Gate-source charge	$Q_{gs}$			14.5	29	58	
Gate-drain charge	$Q_{gd}$			28.5	57	86	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480\text{ V}, I_D = 24\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 4.4\text{ }\Omega$		14	28	56	ns
Rise time	$t_r$			36	72	108	
Turn-off delay time	$t_{d(off)}$			47	93	140	
Fall time	$t_f$			41	82	123	
Gate input resistance	$R_g$	$f = 1\text{ MHz}, \text{open drain}$		0.13	0.65	1.3	$\Omega$
<b>Drain-Source Body Diode Characteristics</b>							
Continuous source-drain diode current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	47	A
Pulsed diode forward current	$I_{SM}$			-	-	140	
Diode forward voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 24\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.2	V
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 24\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 25\text{ V}$		-	582	1164	ns
Body diode reverse recovery charge	$Q_{rr}$			-	11	22	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$			-	31	62	A
Body diode reverse recovery time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = I_S = 24\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$		-	550	1164	ns
Body diode reverse recovery charge	$Q_{rr}$			-	10.7	22	$\mu\text{C}$
Reverse recovery current	$I_{RRM}$			-	38	62	A

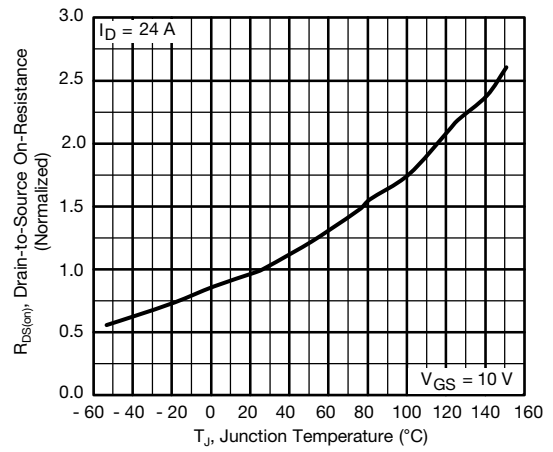
**Notes**

- a.  $C_{oss(er)}$  is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$   
 b.  $C_{oss(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 % to 80 %  $V_{DSS}$

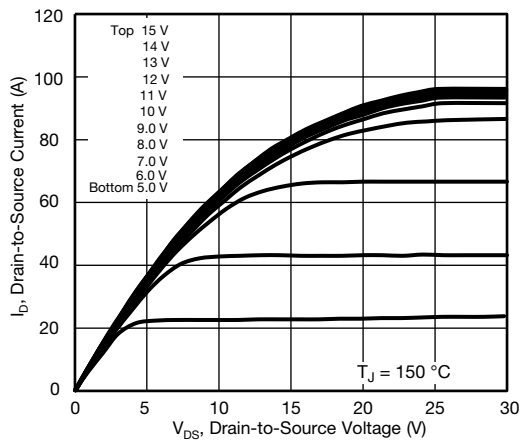
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



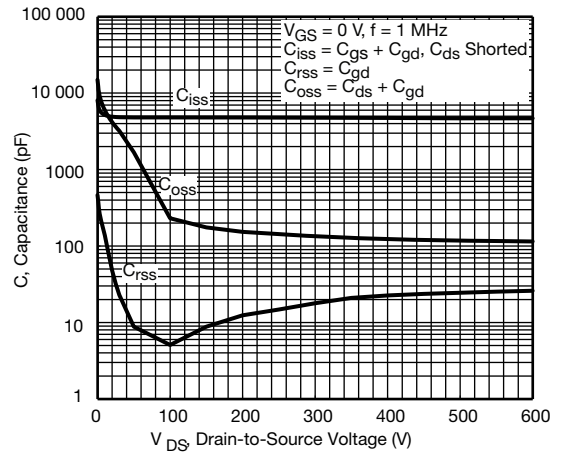
**Fig. 1 - Typical Output Characteristics,  $T_C = 25\text{ }^\circ\text{C}$**



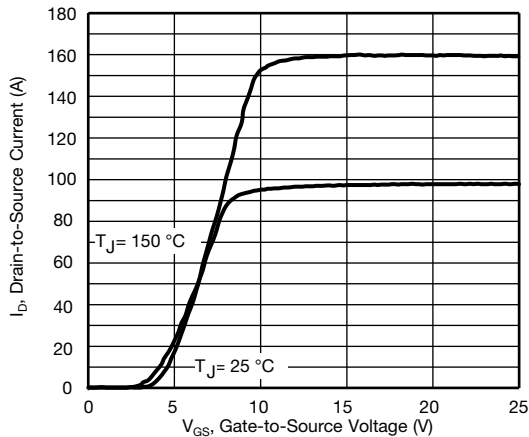
**Fig. 4 - Normalized On-Resistance vs. Temperature**



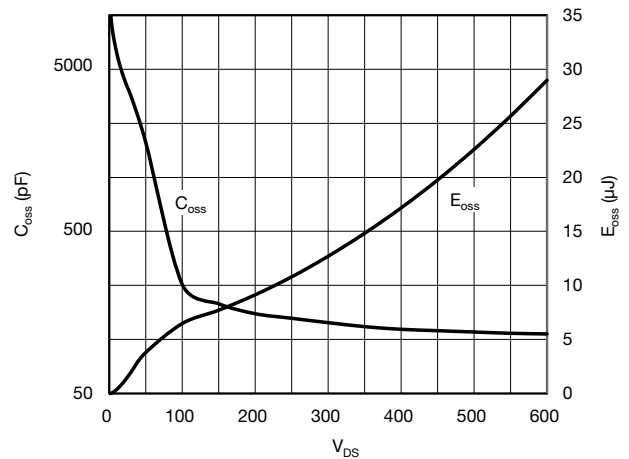
**Fig. 2 - Typical Output Characteristics,  $T_C = 150\text{ }^\circ\text{C}$**



**Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 6 -  $C_{oss}$  and  $E_{oss}$  vs.  $V_{DS}$**

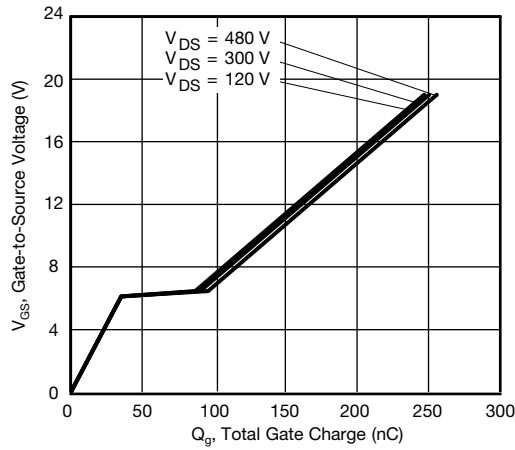


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

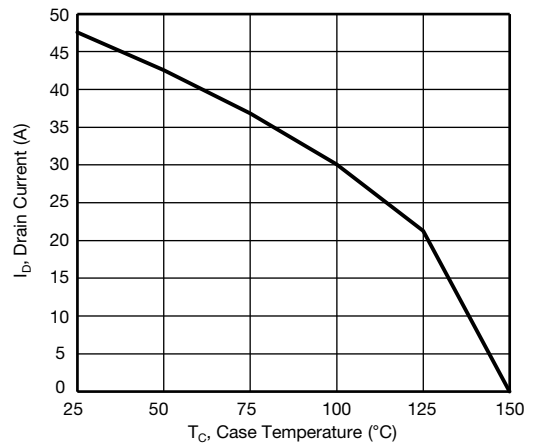


Fig. 10 - Maximum Drain Current vs. Case Temperature

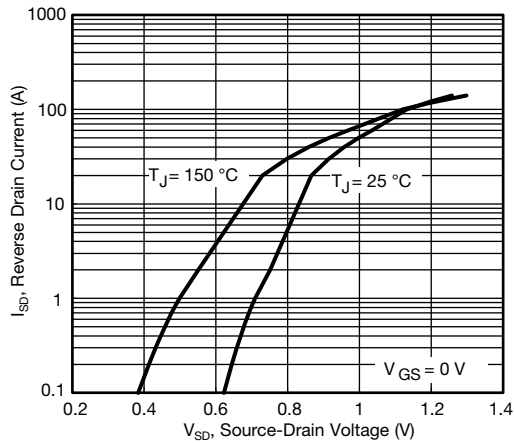


Fig. 8 - Typical Source-Drain Diode Forward Voltage

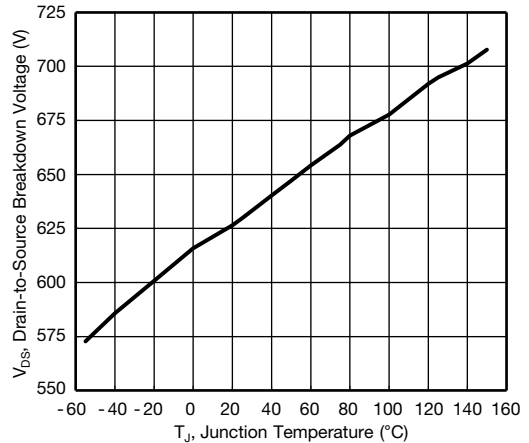


Fig. 11 - Temperature vs. Drain-to-Source Voltage

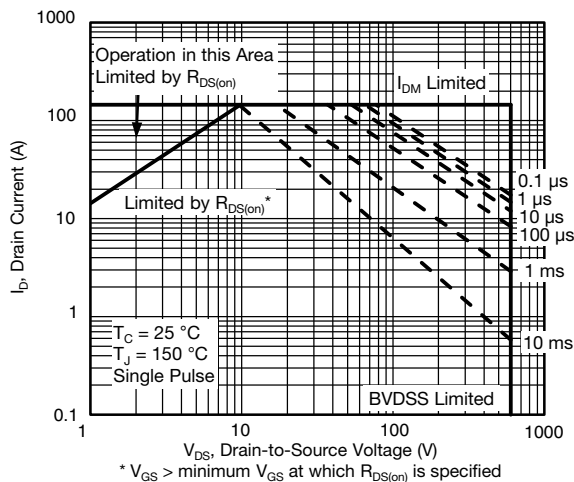


Fig. 9 - Maximum Safe Operating Area

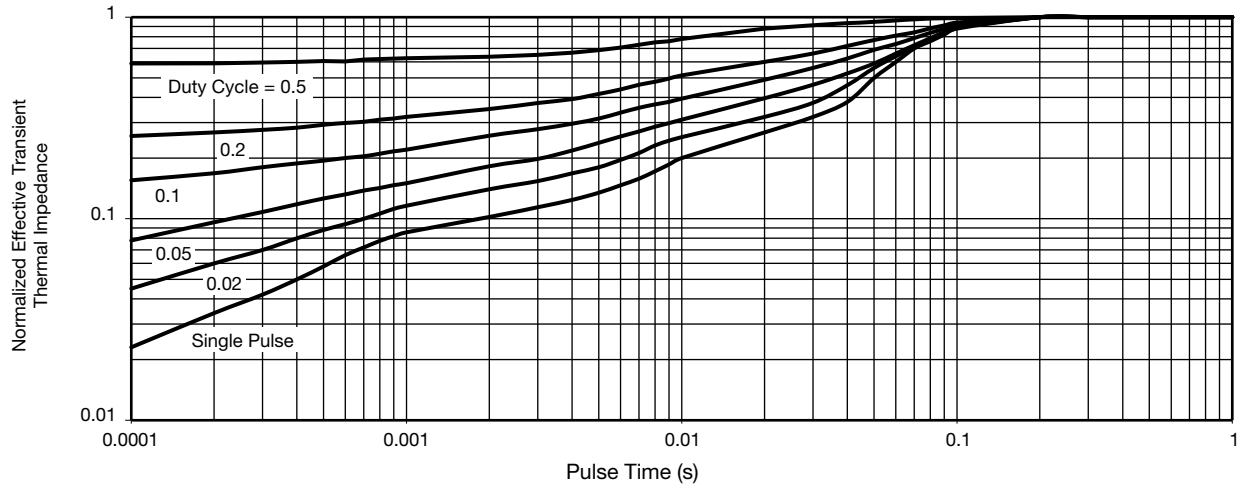


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

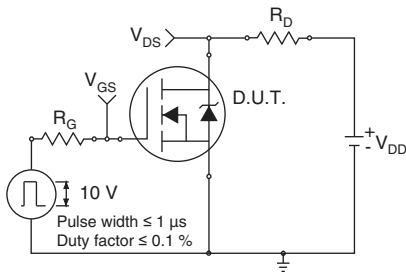


Fig. 13 - Switching Time Test Circuit

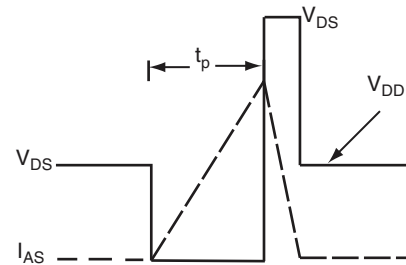


Fig. 16 - Unclamped Inductive Waveforms

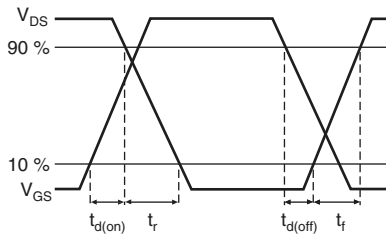


Fig. 14 - Switching Time Waveforms

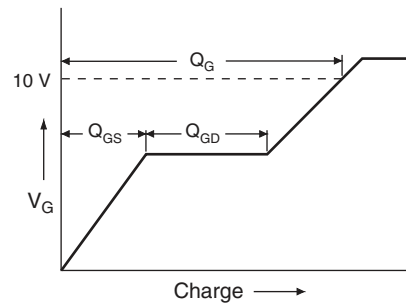


Fig. 17 - Basic Gate Charge Waveform

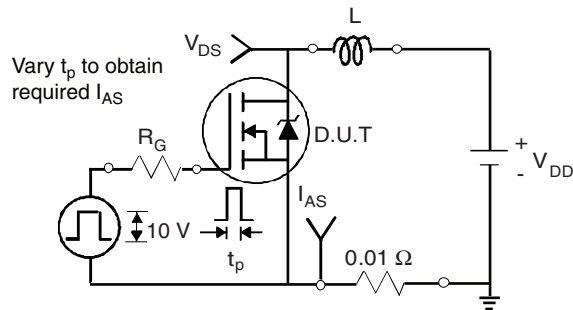


Fig. 15 - Unclamped Inductive Test Circuit

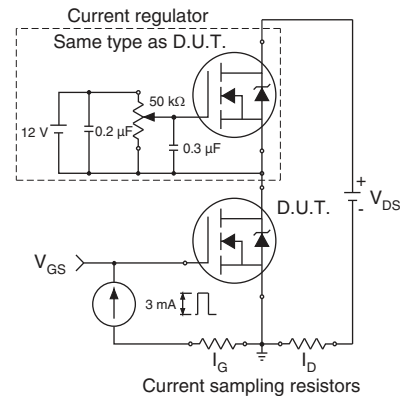
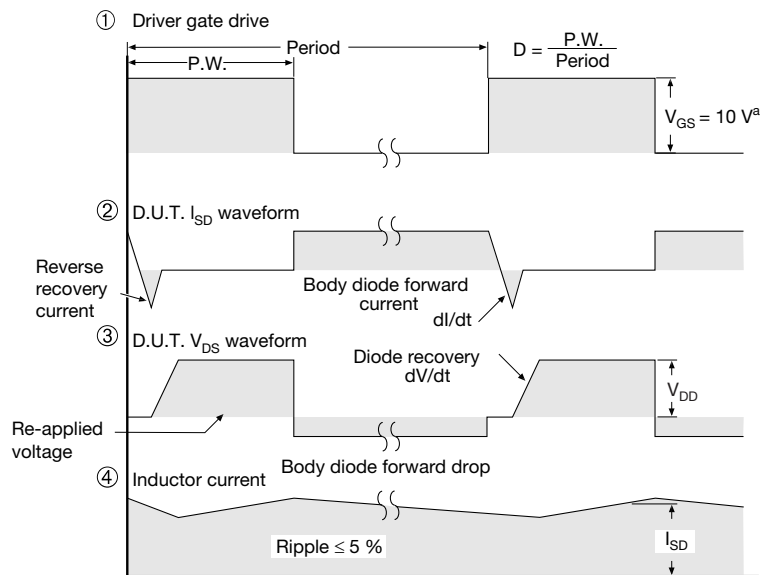
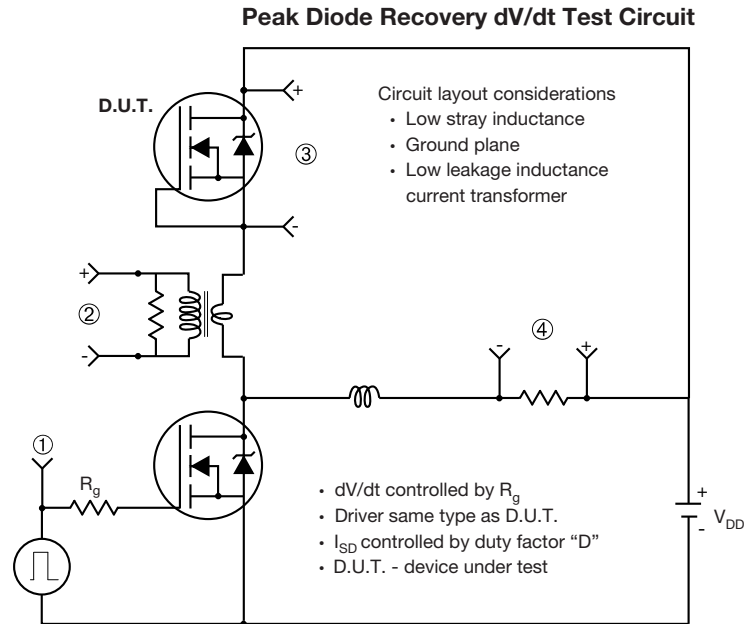


Fig. 18 - Gate Charge Test Circuit



**Note**

a.  $V_{GS} = 5\text{ V}$  for logic level devices

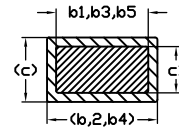
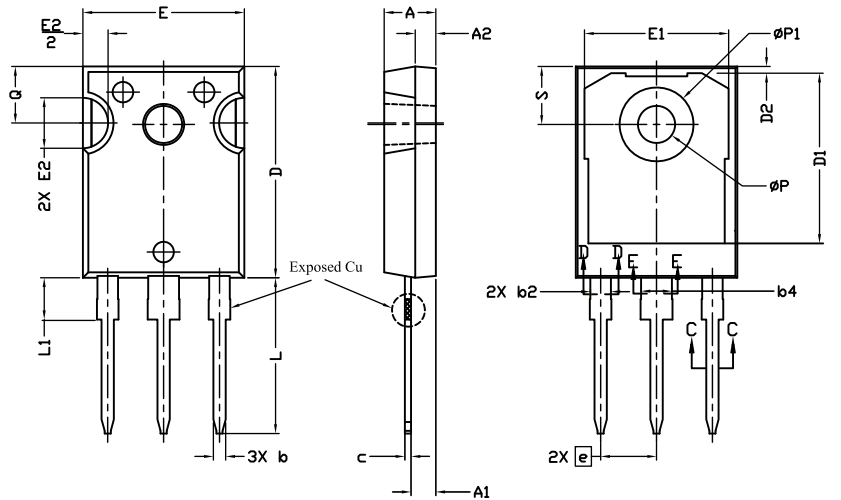
**Fig. 19 - For N-Channel**

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# TO-247AC (High Voltage)

VERSION 1: FACILITY CODE = 9



Section C--C, D---D, E--E

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.83	5.21	
A1	2.29	2.55	
A2	1.50	2.49	
b	1.12	1.33	
b1	1.12	1.28	
b2	1.91	2.39	6
b3	1.91	2.34	
b4	2.87	3.22	6, 8
b5	2.87	3.18	
c	0.55	0.69	6
c1	0.55	0.65	
D	20.40	20.70	4

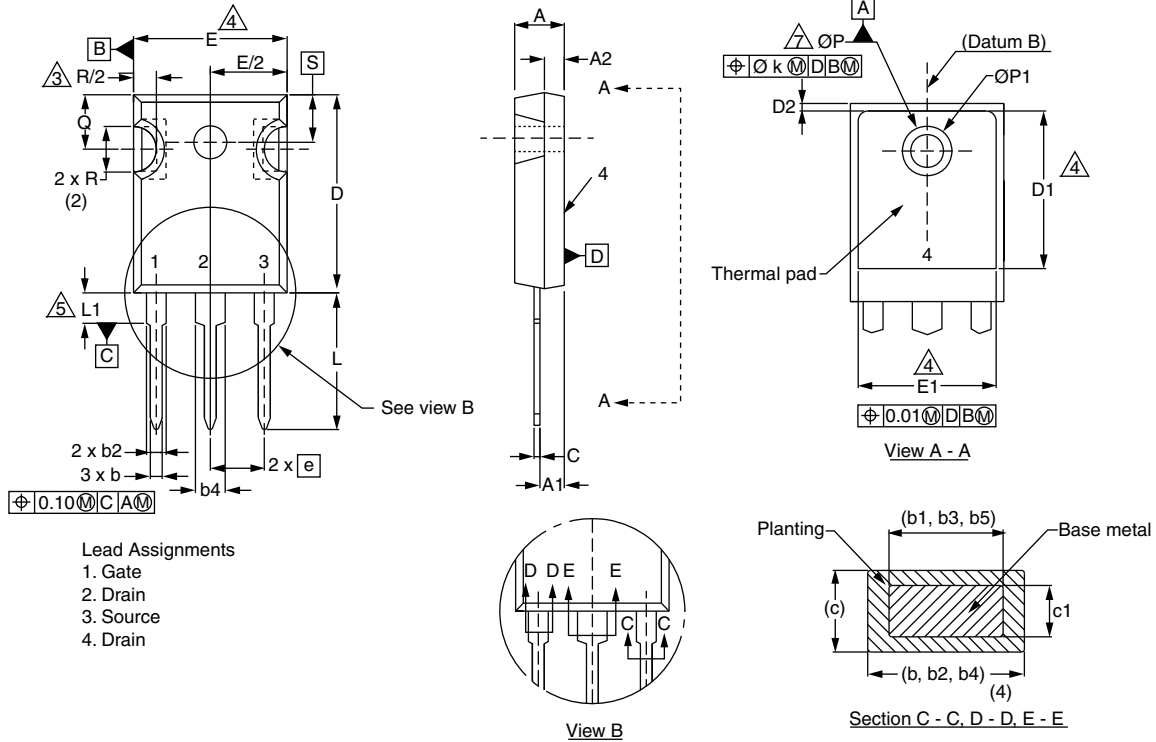
DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D1	16.25	16.85	5
D2	0.56	0.76	
E	15.50	15.87	4
E1	13.46	14.16	5
E2	4.52	5.49	3
e	5.44 BSC		
L	14.90	15.40	
L1	3.96	4.16	6
Ø P	3.56	3.65	7
Ø P1	7.19 ref.		
Q	5.31	5.69	
S	5.54	5.74	

### Notes

- (1) Package reference: JEDEC TO247, variation AC
- (2) All dimensions are in mm
- (3) Slot required, notch may be rounded
- (4) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outermost extremes of the plastic body
- (5) Thermal pad contour optional with dimensions D1 and E1
- (6) Lead finish uncontrolled in L1
- (7) Ø P to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91 mm
- (8) Dimension b2 and b4 does not include dambar protrusion. Allowable dambar protrusion shall be 0.1 mm total in excess of b2 and b4 dimension at maximum material condition



**VERSION 2: FACILITY CODE = Y**



DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
A	4.58	5.31	
A1	2.21	2.59	
A2	1.17	2.49	
b	0.99	1.40	
b1	0.99	1.35	
b2	1.53	2.39	
b3	1.65	2.37	
b4	2.42	3.43	
b5	2.59	3.38	
c	0.38	0.86	
c1	0.38	0.76	
D	19.71	20.82	
D1	13.08	-	

DIM.	MILLIMETERS		NOTES
	MIN.	MAX.	
D2	0.51	1.30	
E	15.29	15.87	
E1	13.72	-	
e	5.46 BSC		
Ø k	0.254		
L	14.20	16.25	
L1	3.71	4.29	
Ø P	3.51	3.66	
Ø P1	-	7.39	
Q	5.31	5.69	
R	4.52	5.49	
S	5.51 BSC		

ECN: E19-0614-Rev. E, 25-Nov-2019  
 DWG: 5971

**Notes**

- (1) Dimensioning and tolerancing per ASME Y14.5M-1994
- (2) Contour of slot optional
- (3) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Thermal pad contour optional with dimensions D1 and E1
- (5) Lead finish uncontrolled in L1
- (6) Ø P to have a maximum draft angle of 1.5 to the top of the part with a maximum hole diameter of 3.91 mm (0.154")
- (7) Outline conforms to JEDEC outline TO-247 with exception of dimension c
- (8) Xian and Mingxin actually photo





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