SiI 9135
HDMI Receiver with Enhanced Audio and Deep Color Outputs

Data Sheet

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Revision History

Revision	Date	Comment
A	01/07	Initial Production Data Sheet
B	02/07	Updates to template and timing measurements
C	06/07	Updated to DSD Audio specifications

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Introduction

The SiI9135 is a second generation HDMI v1.3 Receiver. It is software compatible with the SiI9133, but adds audio support for DTS-HD and Dolby TrueHD. Digital televisions that can display 10/12-bit color depth can now provide the highest quality protected digital audio/video over a single cable. The SiI9135 can receive deep color video up to 12-bit, 1080p@60Hz. Backward compatibility with DVI 1.0 allows HDMI systems to connect to existing DVI 1.0 hosts, such as HD set-top boxes and PCs. The specialized audio and video processing contained in the receiver can add HDMI capability to earlier-generation consumer electronics. Efficient color space conversion receives RGB video data and outputs either standard-definition or high-definition YCbCr formats.

The SiI9135 can send and receive up to eight channels of uncompressed digital audio at 192 kHz and 2-channel digital audio up to 192 kHz. Compressed streams are also supported through either the S/PDIF port or over I^2S for DTS-HD and Dolby TrueHD. An industry-standard I^2S port allows direct connection to low-cost audio DACs at up to 192 kHz. An S/PDIF port supports up to 192 kHz audio. The SiI9135 supports SACD (Super Audio Compact Disc) and provides DSD (Direct Stream Digital) ports that support 44.1 and 88.2 kHz one-bit audio. Audio down-sampling allows the SiI9135 to share the audio bus with a high-sample-rate audio DAC while down-sampling audio for an attached display that supports only lower rates.

The SiI9135 also comes pre-programmed with HDCP keys. This set of keys simplifies the manufacturing process and lowers costs, while providing the highest level of HDCP key security.

Silicon Image's HDMI Receivers use the latest generation of TMDS core technology. These TMDS cores pass all HDMI compliancy tests.

Features

- Dual-Input HDMI 1.3, HDCP 1.1, and DVI 1.0 compliant Receiver
- Integrated TMDS® core running at 25 – 225 MHz
- Digital video interface supports video processors:
  - 36-bit RGB / YCbCr 4:4:4
  - 16/20/24-bit YCbCr 4:2:2
  - 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
  - 12/15/18-bit DMO (Digital Multimedia Output) RGB/YCbCr 4:4:4 (clocked with rising & falling edges)
  - Color Space Conversion for both RGB-to-YCbCr and YCbCr-to-RGB (both 601 and 709)
    - True 12-bit accurate data using 14-bit processing
  - Auto video mode configuration simplifies system firmware design
- Digital audio interface supports high-end audio systems:
  - DTS-HD and Dolby TrueHD high bit rate audio support
  - 4 x I^2S inputs accept Dolby Digital, DVD-Audio input (2-channel 192 kHz, 8-channel 192 kHz)
  - S/PDIF input supports PCM, Dolby Digital, DTS digital audio transmission (32-192 kHz Fs sample rate)
  - IEC60958 or IEC61937 compatible
  - Flexible, programmable I^2S channel mapping
  - 2:1 and 4:1 down-sampling to handle 96 kHz and 192 kHz audio streams.
- Integrated HDCP decryption engine for receiving protected audio and video content:
  - Pre-programmed HDCP keys provide highest level of key security and simplify manufacturing
  - Full support for HDCP Repeaters (up to 16 attached downstream devices)
  - Built in HDCP BIST
- Software compatible with SiI 9033 and SiI 9133
  - Additional register programming required for deep color, DTS-HD and Dolby TrueHD support
- Flexible power management
- 20 mm x 20 mm 144-pin TQFP package with ePad

Pin Diagram

Figure 1 shows the pin connections for the SiI9135 in the 144-pin TQFP package.

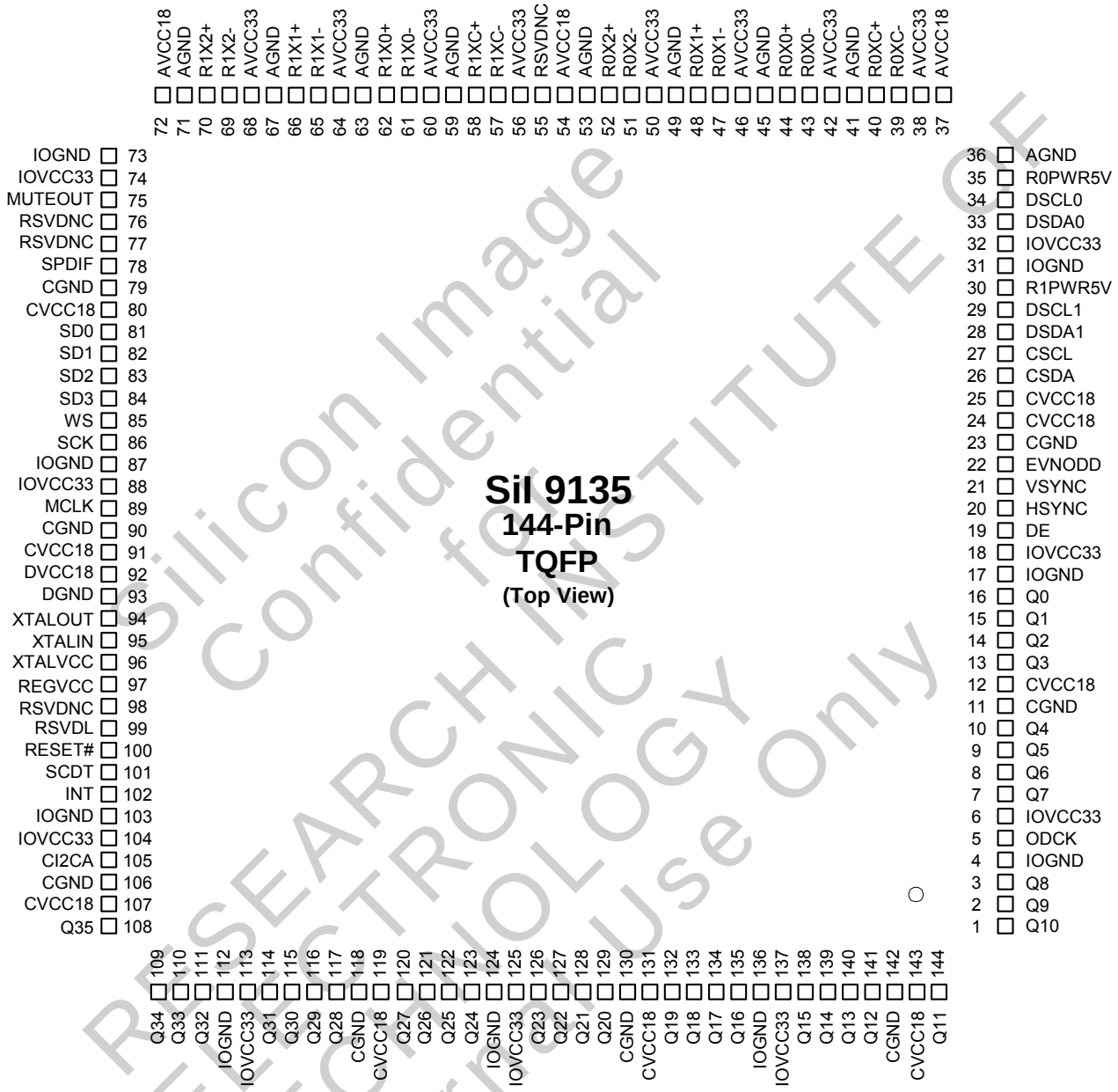


Figure 1. Pin Diagram

Individual pin functions are described beginning on page 34.

System Applications

The SiI9135 is designed for AV Receivers that require support for HDMI v1.3 Deeper Color and the latest audio technologies; DTS-HD and Dolby TrueHD. The SiI9135 supports the HDMI v1.3 specification and allows receipt of 10/12-bit color depth up to 1080p resolutions. A single SiI9135 provides two HDMI input ports. The video output goes to a video processor or HDMI transmitter. Besides DTS-HD and Dolby TrueHD, the SiI9135 supports full surround sound audio including DVD-Audio and SACD. The audio output can go directly to an audio DAC or an Audio DSP for further processing as shown in Figure 2.

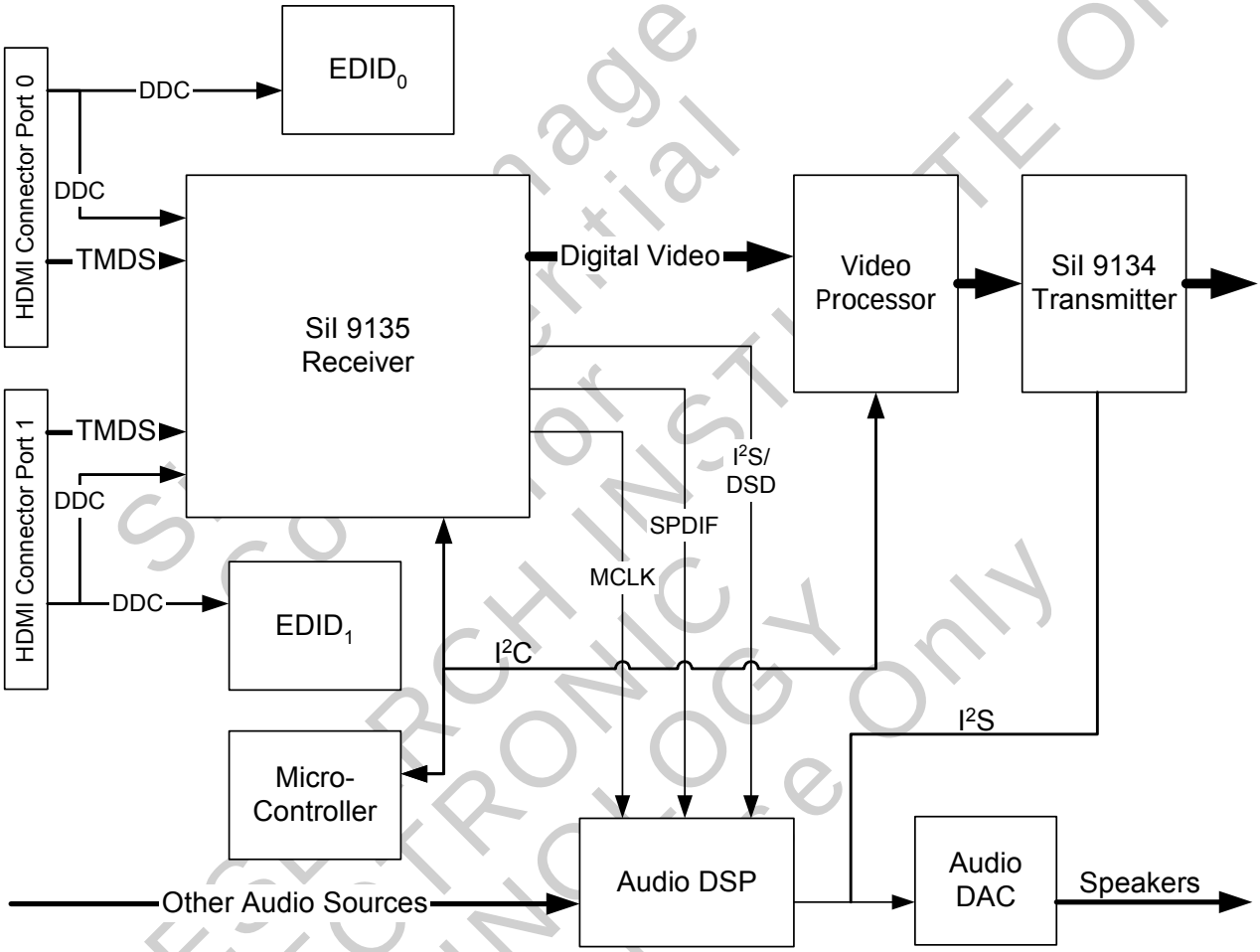


Figure 2. Digital Television Receiver Block Diagram

Comparing SiI9135 with SiI 9033 and SiI 9133

Table 1 summarizes the functional differences between the SiI 9033, the SiI 9133, and the SiI9135.

Table 1. Summary of New Features

	SiI 9033	SiI 9133	SiI 9135
HDMI Input Connections			
TMDS Input Ports	2	2	2
Color Depth	8-bit	8/10/12-bit	8/10/12-bit
DDC Input Ports	2	2	2
Maximum TMDS Input Clock	165 MHz	225 MHz	225 MHz
Output Ports			
Digital Video Output Ports	1	1	1
Maximum Output Pixel Clock	165 MHz.	165 MHz.	165 MHz.
Maximum Output Bus Width	24	36	36
Analog Video Output Ports	0	0	0
S/PDIF Output Ports	1	1	1
I^2S Output	8 channel	8 channel	8 channel
DSD Output	8 channel	8 channel	6 channel
Video Processing			
Color Space Converter	RGB to/from YCbCr	RGB to/from YCbCr	RGB to/from YCbCr
Pixel Clock Divider	0.25,0.5	0.25,0.5	0.25,0.5
Digital Video Bus Mapping	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins
Maximum Audio Sample Rate (Fs)			
2-channel (I^2S or S/PDIF)	192 kHz	192 kHz	192 kHz
8-channel (I^2S)	192 kHz	192 kHz	192 kHz
8-channel (DSD)	88.2 kHz	88.2 kHz	88.2 kHz (6 channel)
High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD	No	No	Yes
Local I^2C Device Address	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A	0x60/0x68 or 0x62/0x6A
MCLK Generation	No external connection required.	No external Connection required	No external connection required.
HDCP Repeater Support	Yes	Yes	Yes
Interlaced Format Detection Pin	Yes	Yes	Yes
TMDS R_{EXT}	Not Used	Not Used	Not Used
Package	144-pin TQFP ePad	404-pin BGA w/Heat Slug	144-pin TQFP ePad

Functional Description

The SiI9135 provides a complete solution for receiving HDMI-compliant digital audio and video. Specialized audio and video processing is available within the HDMI Receiver to add HDMI capability to consumer electronics such as AV Receivers. Figure 3 shows the functional blocks of the chip.

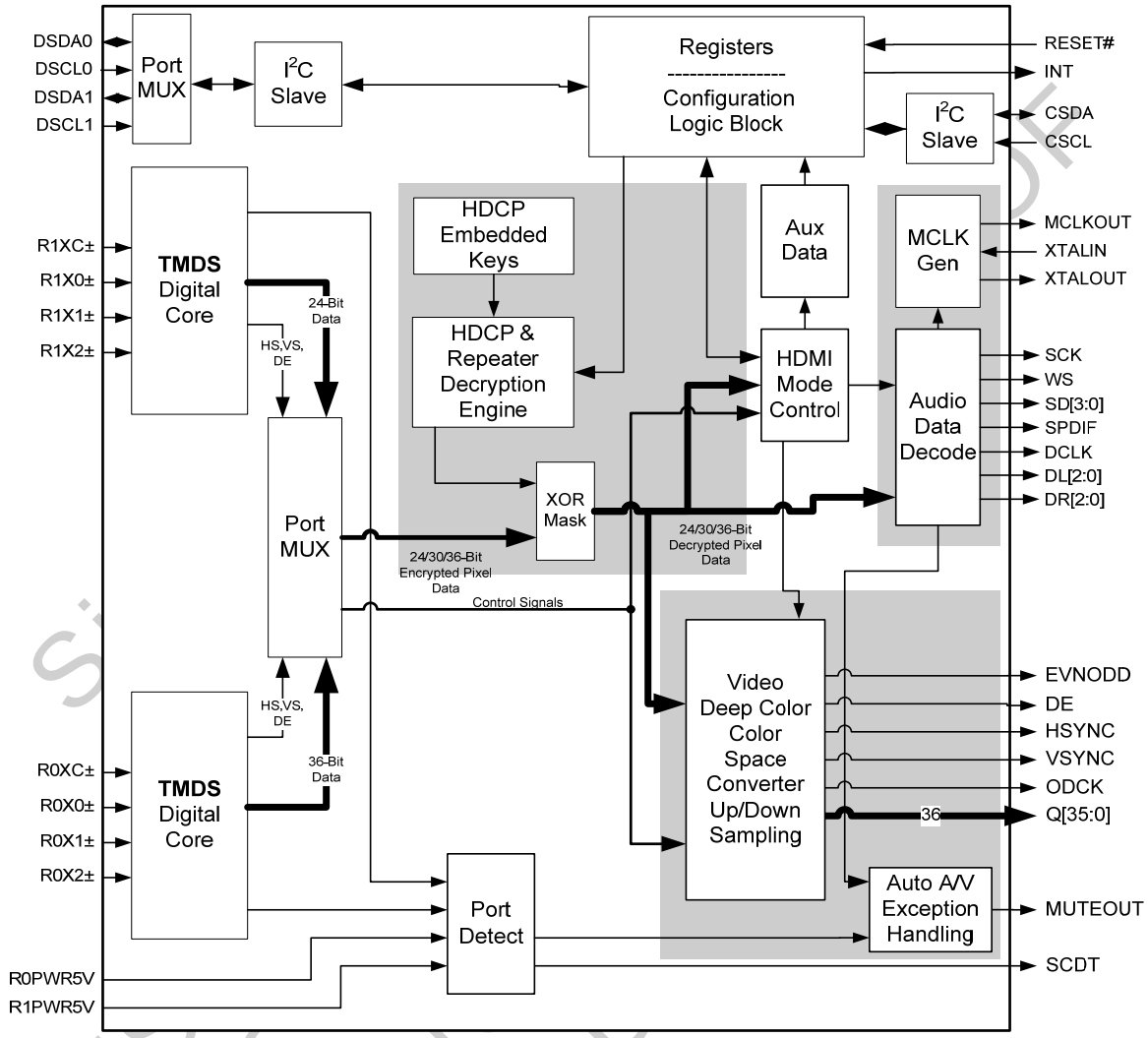


Figure 3. Functional Block Diagram

The SiI9135 supports two HDMI input ports. Only one port can be active at any time.

TMDS Digital Cores

The two TMDS Digital cores are the latest generation cores that support HDMI v1.3 and the ability to carry 10/12-bit color depth. The cores are capable of receiving TMDS data at up to 225 MHz. Each core performs 10-to-8-bit TMDS decoding on the audio and video data received from the three TMDS differential data lines along with a TMDS differential clock. The TMDS cores can sense a stopped clock or stopped video and software can put the HDMI Receiver into power-down mode.

Active Port Detection and Selection

Only one port can be active at a time, under control of the HDMI Receiver's firmware. Active TMDS signaling can arrive at both ports, but only one has internal circuitry enabled. These states are controlled with register settings by the firmware in the display.

Other control signals are associated with the TMDS signals on each HDMI port. The HDMI Receiver can monitor the +5V supply from each attached host. The firmware can poll registers to check on which ports are connected. The firmware also controls functional connection to one of the two E-DDC buses, enabling one while disabling the other. An attached host determines the active status of an attached HDMI device by polling the E-DDC bus to the HDMI Receiver.

Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for a complete description of port detection and selection.

HDCP Decryption Engine/XOR Mask

The HDCP decryption engine contains all the necessary logic to decrypt the incoming audio and video data. The decryption process is entirely controlled by the host side microcontroller/microprocessor through a set sequence of register reads and writes through the DDC channel. Pre-programmed HDCP keys and Key Selection Vector (KSV) stored in the on-chip non-volatile memory are used in the decryption process. A resulting calculated value is applied to an XOR mask during each clock cycle to decrypt the audio/video data.

The SiI9135 also contains all the necessary logic to support full HDCP Repeaters. The KSV values of downstream devices (up to 16 total) are written into the HDMI Receiver through the local I^2C bus (CSDA/CSCL). As defined in the HDCP Specification, Vi' is calculated and made available to the host on the DDC bus (DSDA/DSCL).

HDCP Embedded Keys

The SiI9135 HDMI Receiver comes pre-programmed with a set of production HDCP keys stored on-chip in non-volatile memory. System manufacturers do not need to purchase key sets from the Digital-Content LLC. All purchasing, programming, and security for the HDCP keys is handled by Silicon Image. The pre-programmed HDCP keys provide the highest level of security, as keys cannot be read out of the device after they are programmed. Before receiving samples of the SiI9135, customers must sign the HDCP license agreement (www.digital-cp.com) or a special NDA with Silicon Image.

Data Input and Conversion

Mode Control Logic

The mode control logic determines if the decrypted data is video, audio, or auxiliary information and directs it to the appropriate logic block.

Video Data Conversion and Video Output

The HDMI Receiver can output video in many different formats (see examples in Table 2) and can process the video data before it is output, as shown in Figure 4. You can bypass each of the processing blocks by setting the appropriate register bits.

Table 2. Digital Video Output Formats

Color Space	Video Format	Bus Width	HSYNC/ VSYNC	Output Clock (MHz)							Notes
				480i/576i	480p	XGA	720p	1080i	SXGA	1080p	
RGB	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	
		30	Separate	27	27	65	74.25	74.25	108	148.5	
		24	Separate	27	27	65	74.25	74.25	108	148.5	
		12/15/18	Separate	27	27	65	74.25	74.25	-	-	4
YCbCr	4:4:4	36	Separate	27	27	65	74.25	74.25	108	148.5	
		30	Separate	27	27	65	74.25	74.25	108	148.5	
		24	Separate	27	27	65	74.25	74.25	108	148.5	
		12/15/18	Separate	27	27	65	74.25	74.25	-	-	4
	4:2:2	16/20/24	Separate	27	27	—	74.25	74.25	—	148.5	
		16/20/24	Embedded	27	27	—	74.25	74.25	—	148.5	1
		8/10/12	Separate	27	54	—	148.5	148.5	-	-	
		8/10/12	Embedded	27	54	—	148.5	148.5	-	-	1
Notes				2, 3							

Notes:

1. Embedded syncs use SAV/EAV coding.
2. 480i and 576i modes can output a 13.25 MHz clock using the internal clock divider.
3. Output clock frequency depends on programming of internal registers. Differential TMDS clock is always 25 MHz or faster.
4. Output clock supports 12/15/18-bit mode by using both edges.

Color Range Scaling

The color range depends on the video format, according to the CEA-861B specification. In some applications the 8-bit input range uses the entire span of 0x00 (0) to 0xFF (255) values. In other applications the range is scaled narrower. The HDMI Receiver cannot detect the incoming video data range and there is no required range specification in the HDMI AVI packet. The HDMI Receiver chooses scaling depending on the detected video format. 10 and 12-bit color range scaling are both handled the same way. Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for more details.

When the HDMI Receiver outputs embedded syncs (SAV/EAV codes), it also limits the YCbCr data output values to 1 to 254.

Up Sample / Down Sample

Additional logic can convert from 4:2:2 to 4:4:4 (8/10/12-bit) or from 4:4:4 (8/10/12-bit) to 4:2:2 YCbCr format. All processing is done with 14-bits of accuracy for true 12-bit data.

Deep-color Packetizing and Un-packetizing

10/12-bit to 8-bit conversion of the 10/12-bit Deep-color video input data is performed by increasing TMDS clock and packetizing the extra bits into the next byte, based on the HDMI 1.3 specification. This packetizing function is performed by the HDMI transmitter. The HDMI receiver unpacks the deep-color data to output 10/12-bit data on the video bus.

For 24-bit (8 bit-per-pixel) inputs, the TMDS clock on the HDMI link is 1x the output pixel clock
For 30-bit (10 bit-per-pixel) inputs, the TMDS clock on the HDMI link is 1.25x the output pixel clock
For 36-bit (12 bit-per-pixel) inputs, the TMDS clock on the HDMI link is 1.5x the output pixel clock

Color Space Conversion

RGB to YCbCr The RGB→YCbCr color space converter (CSC) can convert from video data RGB to standard definition (ITU.601) or to high definition (ITU.709) YCbCr formats. The HDMI AVI packet defines the color space of the incoming video.

Table 3. Color Space versus Video Format

		Formulae
Video Format	**Conversion**	**CE Mode 16-235 RGB**
640 x 480	ITU-R BT.601	Y = 0.299R' + 0.587G' + 0.114B'
480i	ITU-R BT.601	Cb = –0.172R' – 0.339G' + 0.511B' + 128
576i	ITU-R BT.601	Cr = 0.511R' – 0.428G' – 0.083B' + 128
480p	ITU-R BT.601	
576p	ITU-R BT.601	
240p	ITU-R BT.601	
288p	ITU-R BT.601	
720p	ITU-R BT.709	Y = 0.213R' + 0.715G' + 0.072B'
1080i	ITU-R BT.709	Cb = –0.117R' – 0.394G' + 0.511B' + 128
1080p	ITU-R BT.709	Cr = 0.511R' – 0.464G' – 0.047B' + 128

YCbCr to RGB The YCbCr→RGB color space converter is available to interface to MPEG decoders with RGB-only inputs. The CSC can convert from YCbCr in standard-definition (ITU.601) or high-definition (ITU.709) to RGB. Refer to the detailed formulae in Table 4. Note the difference between RGB range for CE modes and PC modes.

Table 4. YCbCr-to-RGB Color Space Conversion Formulae

	Conversion	**YCbCr Input Color Range**
YCbCr 16-235 Input to RGB 16-235 Output	**601**	R' = Y + 1.371(Cr – 128) G' = Y – 0.698(Cr – 128) – 0.336(Cb – 128) B' = Y + 1.732(Cb – 128)
	709	R' = Y + 1.540(Cr – 128) G' = Y – 0.459(Cr – 128) – 0.183(Cb – 128) B' = Y + 1.816(Cb – 128)
YCbCr 16-235 Input to RGB 0-255 Output	**601**	R' = 1.164((Y-16) + 1.371(Cr – 128)) G' = 1.164((Y-16) – 0.698(Cr – 128) – 0.336(Cb – 128)) B' = 1.164((Y-16) + 1.732(Cb – 128))
	709	R' = 1.164((Y-16) + 1.540(Cr – 128)) G' = 1.164((Y-16) – 0.459(Cr – 128) – 0.183(Cb – 128)) B' = 1.164((Y-16) + 1.816(Cb – 128))

Default Video Configuration

After hardware RESET, the HDMI Receiver chip is configured in its default mode. This is summarized in Table 5. For more details and for a complete register listing, refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042).

Table 5. Default Video Processing

Video Control	Default after Hardware Reset	Note
HDCP Decryption	HDCP decryption is OFF	1
Color Space Conversion	No color space conversion	1
Color Space Selection	BT.601 selected	
Color Range Scaling	No range scaling	1
Upsampling/Downsampling	No upsampling or downsampling	
HSYNC & VSYNC Timing	No inversions of HSYNC or VSYNC	
Data Bit Width	Uses 8-bit data	1
Pixel Clock Replication	No pixel clock replication	1
Power Down	Everything is powered down	

Notes:

1. The HDMI Receiver assumes DVI mode after reset, which is RGB 24-bit 4:4:4 video with 0:255 range.

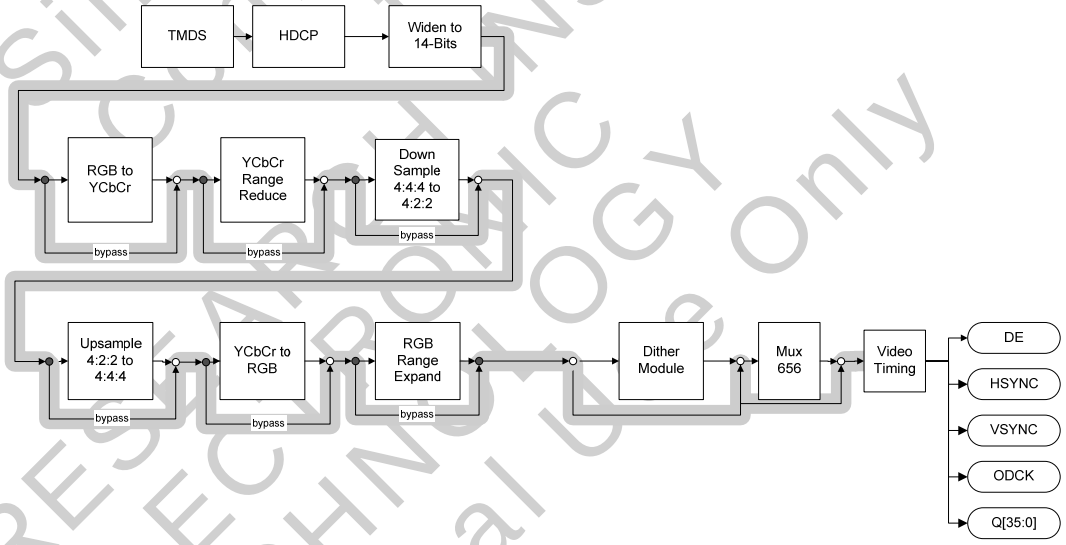


Figure 4. Default Video Processing Path

Automatic Video Configuration

The SiI9135 adds automatic video configuration to simplify the firmware's task of updating the video path whenever the incoming video changes format. Bits in the HDMI Auxiliary Video Information (AVI) InfoFrame are used to reprogram the registers in the video path.

Table 6. AVI InfoFrame Video Path Details

AVI Byte 1 Bits [6:5]		AVI Byte 2 Bits [7:6]		AVI Byte 5 Bits [3:0]	
Y[1:0]	**Color Space**	**C[1:0]**	**Colorimetric**	**PR[3:0]**	**Pixel Repetition**
00	RGB 4:4:4	00	No Data	0000	No repetition
01	YCbCr 4:4:4	01	ITU 601	0001	Pixel sent 2 times
10	YCbCr 4:2:2	10	ITU 709	0010	Pixel sent 3 times
11	Future	11	Future	0011	Pixel sent 4 times
				0100	Pixel sent 5 times
				0101	Pixel sent 6 times
				0110	Pixel sent 7 times
				0111	Pixel sent 8 times
				1000	Pixel sent 9 times
				1001	Pixel sent 10 times

Notes on Table 6:

1. The Auto Video Configuration assumes that the AVI information is accurate. If information is not available, then the SiI9135 must choose the video path based on measurement of the incoming resolution.
2. Refer to EIA/CEA-861B Specification for details.
3. The SiI9135 can support only pixel replication modes 0b0000, 0b0001, and 0b0011. Other modes are unsupported and can result in unpredictable behavior.

Output modes are specified using the OutMode register. Other modes are reserved for future expansion.

Table 7. OutMode Programming

	Digital Output				
OutMode[7:0]	**Color**		**Width**	**MUX**	**Sync**
0b00000000	RGB	4:4:4	36	N	Sep.
0b00000010	RGB	4:4:4	36	N	Sep.
0b00000100	RGB	4:4:4	36	N	Sep.
0b00000110	RGB	4:4:4	36	N	Sep.
0b00000001	RGB	4:4:4	36	N	Sep.
0b00000011	RGB	4:4:4	36	N	Sep.
0b00000101	RGB	4:4:4	36	N	Sep.
0b00000111	RGB	4:4:4	36	N	Sep.
0b10000000	YCbCr	4:4:4	36	N	Sep.
0b10000010	YCbCr	4:4:4	36	N	Sep.
0b10000100	YCbCr	4:4:4	36	N	Sep.
0b10000110	YCbCr	4:4:4	36	N	Sep.
0b10000001	YCbCr	4:4:4	36	N	Sep.
0b10000011	YCbCr	4:4:4	36	N	Sep.
0b10000101	YCbCr	4:4:4	36	N	Sep.
0b10000111	YCbCr	4:4:4	36	N	Sep.
0b11000000	YCbCr	4:2:2	8	N	Sep.
0b11001000	YCbCr	4:2:2	10	N	Sep.
0b11100000	YCbCr	4:2:2	8	Y	Sep.
0b11101000	YCbCr	4:2:2	10	Y	Sep.
0b11110000	YCbCr	4:2:2	8	Y	Emb.
0b11111000	YCbCr	4:2:2	10	Y	Emb.

Audio Data Capture Logic

The SiI9135 can accept digital audio over S/PDIF, four I^2S inputs, or eight one-bit audio inputs.

S/PDIF

The S/PDIF stream can carry 2-channel uncompressed PCM data (IEC 60958) or a compressed bit stream for multi-channel (IEC 61937) formats. The audio data capture logic forms the audio data into packets in accordance with the HDMI specification. The S/PDIF output supports audio sampling rates from 32 to 192 kHz. A separate master clock output (MCLK), coherent with the S/PDIF output, is provided for time-stamping purposes. *Coherent* means that the MCLK and S/PDIF must have been created from the same clock source. This is typically done by using the original MCLK to strobe out the S/PDIF from the sourcing chip. There is no setup or hold timing requirement on an output with respect to MCLK.

I^2S

Four I^2S inputs allow transmission of DVD-Audio or decoded Dolby Digital to A/V Receivers and high-end displays. The interface supports up to 8-channel 192 kHz. The I^2S pins must also be *coherent* with MCLK.

The audio data can be down-sampled by one half or one-fourth with register control. This allows the SiI9135 to share the audio bus with a high sample rate audio DAC, while down-sampling audio for an attached display that supports only lower rates. Conversions from 192 to 48 kHz, 176.4 to 44.1 kHz, 96 to 48 kHz, and 88.2 to 44.1 kHz are supported. Audio data can only be down-sampled on 2-ch. audio.

The appropriate registers must be configured to describe the format of audio being input into the SiI9135. This information is passed over the HDMI link in the CEA-861B Audio Info (AI) packets.

MCLK frequencies support various audio sample rates as shown in Table 8.

Table 8. Supported MCLK Frequencies

	Audio Sample Rate, Fs						
	I^2S and S/PDIF Supported Rates						
Multiple of Fs	**32 kHz**	**44.1 kHz**	**48 kHz**	**88.2 kHz**	**96 kHz**	**176.4 kHz**	**192 kHz**
128	4.096 MHz	5.645 MHz	6.144 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz
192	6.144 MHz	8.467 MHz	9.216 MHz	16.934 MHz	18.432 MHz	33.868 MHz	36.864 MHz
256	8.192 MHz	11.290 MHz	12.288 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz
384	12.288 MHz	16.934 MHz	18.432 MHz	33.864 MHz	36.864 MHz	67.737 MHz	73.728 MHz
512	16.384 MHz	22.579 MHz	24.576 MHz	45.158 MHz	49.152 MHz		
768	24.576 MHz	33.869 MHz	36.864 MHz	67.738 MHz	73.728 MHz		
1024	32.768 MHz	45.158 MHz	49.152 MHz				
1152	36.864 MHz	50.803 MHz	55.296 MHz				

One-Bit Audio Input (DSD/SACD)

DSD (direct stream digital) is an audio data format defined for SACD (Super Audio CD) applications. It consists of three data outputs for the left channel, three data outputs for the right channel, and a clock for up to 6 channel support. One bit audio sources provide MCLK. One-bit Audio supports 64*Fs, with Fs being either 44.1 kHz or 88.2 kHz.

Internally, the one bit audio inputs are sampled on the positive edge of the DSD Clock, assembled into 56-bit packets and then mapped to the appropriate FIFO. The SiI9135 generates a “static one bit audio detect” interrupt (received 28 consecutive zeros or ones), and an “invalid one bit audio detect” interrupt (received more then 24 bits out of 28 bits of the same value). For one bit audio, the sampling information is carried in the Audio InfoFrame, instead of the Channel Status bits.

High-Bitrate Audio on HDMI

The new high-bitrate compressed standards such as DTS-HD and Dolby TrueHD transmit data at bitrates as high as 18 to 24 Mbps. Because these bitrates are so high, DVD decoders and HDMI transmitters (as source devices), and DSP and HDMI receivers (as sink devices) must carry the data using four I^2S lines rather than using a single very-high-speed S/PDIF or I^2S bus (see Figure 5).

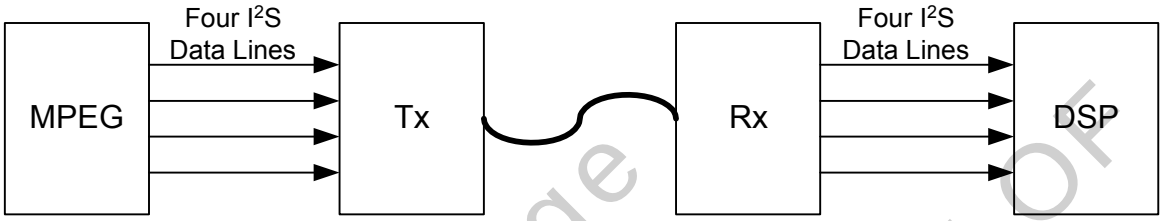


Figure 5: High Speed Data Transmission

The high-bitrate audio stream is originally encoded as a single stream. In order to send it over four I^2S lines, the DVD decoder needs to split this single stream into four streams. Because the single stream of data is being sent over four lines, the programmable ACR (Audio Clock Regeneration) rate is now four times the 96 kHz (384 kHz) or four times the 192 kHz (768 kHz) sample rate.

Figure 6 shows the high bitrate stream before it has been split into four I^2S lines, and after it has been reassembled.

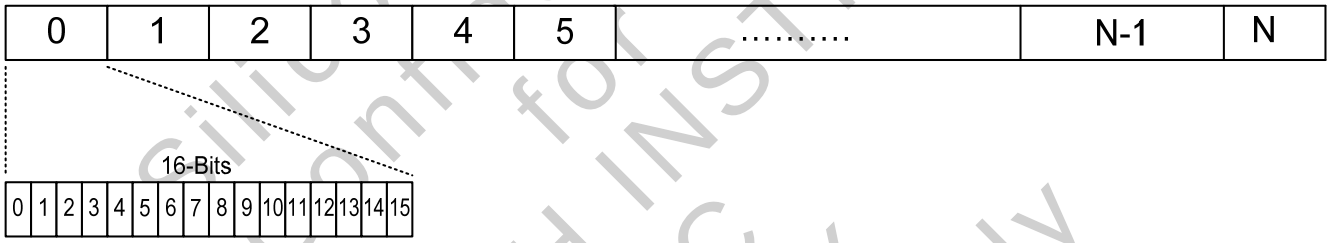


Figure 6: High Bitrate Stream Before and After Reassembly and Splitting

Figure 7 shows the same high bitrate audio stream after being split into four I^2S lines:

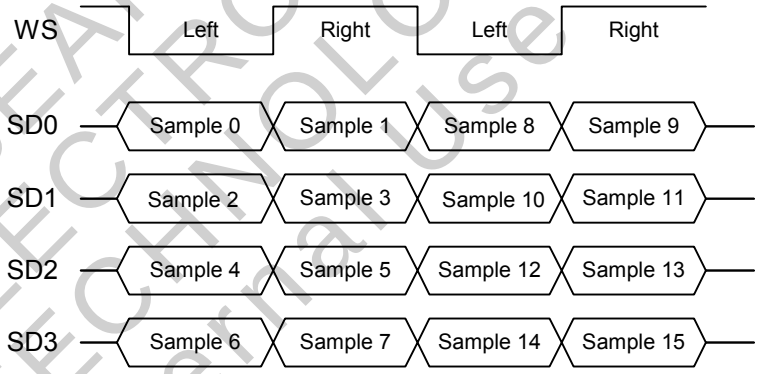


Figure 7. High Bitrate Stream After Splitting

Table 9. Maximum Audio Sampling Frequency for All Video Format Timings

Description	Format Timing	Pixel Repetition	Vertical Freq. (Hz)	Max fs 8 ch (kHz)			Max fs 2 ch (kHz)
				4:2:2 and 4:4:4 24-bit	4:4:4 Deep Color (depth in bits)		
60 Hz Formats				**Standard**	**10**	**12**	
VGA	640x480p	none	59.94/60	48	48	48	192
480i	1440x480i	2	59.94/60	48	48	48	192
480i	2880x480i	4	59.94/60	192	192	192	192
240p	1440x240p	2	59.94/60	48	48	48	192
240p	2880x240p	4	59.94/60	192	192	192	192
480p	720x480p	none	59.94/60	48	48	48	192
480p	1440x480p	2	59.94/60	96	96	96	192
480p	2880x480p	4	59.94/60	192	192	192	192
720p	1280x720p	none	59.94/60	192	192	192	192
1080i	1920x1080i	none	59.94/60	192	192	192	192
1080p	1920x1080p	none	59.94/60	192	192	192	192
50 Hz Formats				**Standard**	**10**	**12**	
576i	1440x576i	2	50	48	48	48	192
576i	2880x576i	4	50	192	192	192	192
288p	1440x288p	2	50	48	48	48	192
288p	2880x288p	4	50	192	192	192	192
576p	720x576p	none	50	48	48	48	192
576p	1440x576p	2	50	96	96	96	192
576p	2880x576p	4	50	192	192	192	192
720p/50	1280x720p	none	50	192	192	192	192
1080i/50	1920x1080i	none	50	192	192	192	192
1080p/50	1920x1080p	none	50	192	192	192	192
1080p @ 24-30 Hz				**Standard**	**10**	**12**	
1080p	1920x1080p	none	24	192	192	192	192
1080p	1920x1080p	none	25	192	192	192	192
1080p	1920x1080p	none	29.97/30	192	192	192	192

Auto Audio Configuration

The SiI9135 can control the audio output based on the current states of CablePlug, FIFO, Video, ECC, ACR, PLL, InfoFrame, and HDMI. Audio output is enabled only when all necessary conditions are met. If any critical condition is missing, then the audio output is disabled automatically.

Soft Mute

On command from a register bit or when automatically triggered with Automatic Audio Control (AAC), the SiI9135 progressively reduces the audio data amplitude to mute the sound in a controlled manner. This is useful when there is an interruption to the HDMI audio stream (or an error) to prevent any audio pop from being sent to the I^2S, S/PDIF, or DSD outputs.

Control and Configuration

Register/Configuration Logic

The register/configuration logic block incorporates all the registers required for configuring and managing the features of the SiI9135. These registers are used to perform HDCP authentication, audio/video/auxiliary format processing, CEA-861B Infoframe Packet format, and power-down control.

The registers are accessible from one of two serial ports. The first port is the DDC port, which is connected through the HDMI cable to the HDMI host. It is used to control the SiI9135 from the host device for HDCP operation. The second port is the local I²C port, which is used to control the SiI9135 from the display device. This is shown in Figure 8. The Local Bus accesses the General Registers and the Common Registers. The DDC Bus accesses the HDCP Operation registers and the Common Registers.

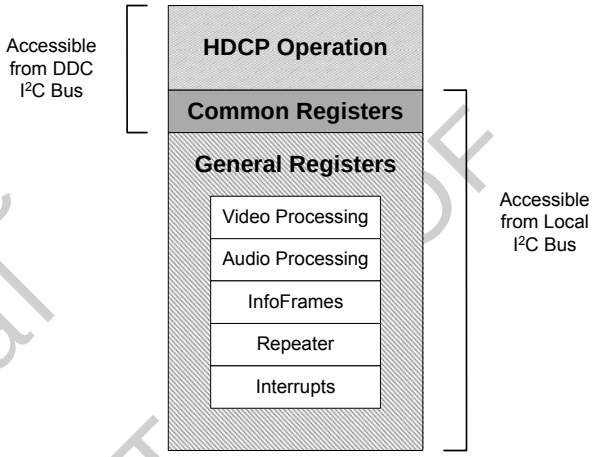


Figure 8. I²C Register Domains

Serial Ports

The SiI9135 provides three serial interfaces: two DDC ports to communicate back to the HDMI or DVI hosts; one I²C port for initialization and control by a local microcontroller in the display. Each interface is 5V tolerant.

E-DDC Bus Interface to HDMI Host

The two DDC interfaces (DSDA0, DSCL0, DSDA1, and DSCL1) on the SiI9135 are slave interfaces capable of running up to 100 kHz. Each interface is connected to one E-DDC bus and is used for HDCP authentication.

The 9135 HDMI Receiver is accessible on the E-DDC bus at device address 0x74. This is compliant with the HDCP 1.1 Specification.

I²C Interface to Display Controller

The Controller I²C interface (CSDA, CSCL) on the SiI9135 is a slave interface capable of running up to 400 kHz. This bus is used to configure the SiI9135 by reading/writing to the appropriate registers. The SiI9135 is accessible on the local I²C bus at two device addresses. Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for more information.

Electrical Specifications

Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	-0.3		4.0	V	1, 2, 3
AVCC18	TMDS PLL #0 Supply Voltage	-0.3		2.5	V	1, 2
AVCC33	TMDS Analog Supply Voltage	-0.3		4.0	V	1, 2
DVCC18	Audio PLL Supply Voltage	-0.3		2.5	V	1, 2, 3
CVCC18	Digital Core Supply Voltage	-0.3		2.5	V	1, 2, 3
XTALVCC	ACR PLL Crystal Oscillator Supply Voltage	-0.3		4.0	V	1, 2
REGVCC	ACR PLL Regulator Supply Voltage	-0.3		4.0	V	1, 2
V_I	Input Voltage	-0.3		IOVCC33+ 0.3	V	1, 2
$V_{5V\text{-}Tolerant}$	Input Voltage on 5V Tolerant Pins	-0.3		5.5	V	5
T_J	Junction Temperature			125	°C	
T_{STG}	Storage Temperature	-65		150	°C	

Notes:

1. Permanent device damage can occur if absolute maximum conditions are exceeded.
2. Functional operation should be restricted to the conditions described under Normal Operating Conditions.
3. Voltage undershoot or overshoot cannot exceed absolute maximum conditions.
4. Refer to SiI9135 Qualification Report for information on ESD performance.
5. All VCC's must be powered to the device. If the device is unpowered and 5V is applied to these inputs, damage can occur.

Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Note
IOVCC33	I/O Pin Supply Voltage	3.15	3.3	3.45	V	1, 4
AVCC33	TMDS Analog Supply Voltage	3.0	3.3	3.6	V	1, 7
AVCC18	TMDS Analog Supply Voltage	1.62	1.8	1.98	V	3, 5
CVCC18	Digital Core Supply Voltage	1.62	1.8	1.98	V	2
DVCC18	ACR Supply Voltage	1.62	1.8	1.98	V	
XTALVCC	ACR PLL Crystal Oscillator Supply Voltage	3.0	3.3	3.6	V	4
REGVCC	ACR PLL Regulator Supply Voltage	3.0	3.3	3.6	V	4, 5
RxPWR5V	DDC I^2C I/O Reference Voltage	4.75	5.00	5.25	V	
DIFF33	Difference between two 3.3V Power Pins			1.0	V	4
DIFF18	Difference between two 1.8V Power Pins			1.0	V	4
DIFF3318	Difference between any 3.3V and 1.8V Pins	-1.0		2.0	V	4, 6
V_{CCN}	Supply Voltage Noise			100	mV_{P-P}	8
T_A	Ambient Temperature (with power applied)	0	25	70	°C	
Θ_{ja}	Ambient Thermal Resistance (Theta JA)			27	°C/W	

Notes:

1. IOVCC33 and AVCC33 pins should be controlled from one power source.
2. CVCC18 should be controlled from one power source.
3. AVCC18 pin should be regulated.
4. Power supply sequencing must guarantee that power pins stay within these limits of each other. See Figure 12.
5. REGVCC is internally regulated to 1.8V and controls the audio PLL. DVCC18 supplies the audio PLL logic.
6. No 1.8V pin can be more than DIFF3318[min] higher than any 3.3V pin. No 3.3V pin can be more than DIFF3318[max] higher than any 1.8V pin.
7. The HDMI 1.0 Specification requires termination voltage (AVCC33) to be controlled to 3.3V±5%. The SiI9135 tolerates a wider range of ±300mV.
8. The supply voltage noise is measured at test point VCCTP in Figure 21 on page 39. The ferrite bead provides filtering of power supply noise. The figure is representative and applies other VCC pins as well.
9. Airflow at 0 m/s.

The schematics on page 67 show decoupling and power supply regulation.

DC Specifications

Digital I/O Specifications

Symbol	Parameter	Pin Type[3]	Conditions[2]	Min	Typ	Max	Units	Note
V_{IH}	High-level Input Voltage	LVTTL		2.0			V	
V_{IL}	Low-level Input Voltage	LVTTL				0.8	V	
V_{TH+}	Low to High Threshold RESET # Pin	Schmitt		1.46			V	5
V_{TH-}	High to Low Threshold RESET# Pin	Schmitt				0.96	V	5
DDC V_{TH+}	Low to High Threshold DSDA0, DSDA1, DSCL0 and DSCL1 pins.	Schmitt		3.0			V	
DDC V_{TH-}	High to Low Threshold DSDA0, DSDA1, DSCL0 and DSCL1 pins.	Schmitt				1.5V	V	
Local I^2C V_{TH+}	Low to High Threshold CSCL and CSDA pins	Schmitt		2.1			V	11, 13
Local I^2C V_{TH-}	High to Low Threshold CSCL and CSDA pins	Schmitt				0.86	V	11, 13
V_{OH}	High-level Output Voltage	LVTTL		2.4			V	10
V_{OL}	Low-level Output Voltage	LVTTL				0.4	V	10
I_{OL}	Output Leakage Current		High Impedance	-10		10	µA	
V_{ID}	Differential Input Voltage			75	250	780	mV	4
I_{OD4}	4mA Digital Output Drive	Output	V_{OUT} = 2.4V	4			mA	1, 6, 7
			V_{OUT} = 0.4V	4			mA	1, 6, 7
I_{OD8}	8mA Digital Output Drive	Output	V_{OUT} = 2.4V	8			mA	1, 6, 8
			V_{OUT} = 0.4V	8			mA	1, 6, 8
I_{OD12}	12mA Digital Output Drive	Output	V_{OUT} = 2.4V	12			mA	1, 6, 9
			V_{OUT} = 0.4V	12			mA	1, 6, 9
R_{PD}	Internal Pull Down Resistor	Outputs	IOVCC33=3.3V	25	50	110	KΩ	1, 12
I_{OPD}	Output Pull Down Current	Outputs	IOVCC33=3.6V		60	90	µA	1, 12
I_{IPD}	Input Pull Down Current	Input	IOVCC33=3.6V		60	90	µA	1

Notes:

1. These limits are guaranteed by design.
2. Under normal operating conditions unless otherwise specified, including output pin loading C_L=10pF.
3. Refer to *Pin Descriptions* (beginning on page 33) for pin type designations for all package pins.
4. Differential input voltage is a single-ended measurement, according to DVI Specification.
5. Schmitt trigger input pin thresholds V_{TH+} and V_{TH-} correspond to V_{IH} and V_{IL}, respectively.
6. Minimum output drive specified at ambient=70°C and IOVCC33=3.0V. Typical output drive specified at ambient=25°C and IOVCC33=3.3V. Maximum output drive specified at ambient=0°C and IOVCC33=3.6V.
7. I_{OD4} Output applies to pins SPDIF, SCK, WS, SD[3:0], DCLK, INT, CSDA,
8. I_{OD8} Output applies to pins DE, HSYNC, VSYNC, Q[35:0].and MCLK.
9. I_{OD12} Output applies to pin ODCK

10. Note that the SPDIF output drives LVTTL levels, not the low-swing levels defined by IEC958.
11. The SCL and SDA pins are not true open-drain buffers. When no VCC is applied to the chip, these pins can continue to draw a small current, and prevent the master IC from communicating with other devices on the I^2C bus. Therefore, do not power-down the SiI9135 (remove VCC) unless the attached I^2C bus is completely idle.
12. The chip includes an internal pull-down resistor on many of the output pins. When tri-stated, these pins draw a pull down current according to this specification when the signal is driven high by another source device.
13. With -10% IOVCC33 supply, the High-to-Low Threshold on DDC and I^2C bus is marginal. A - 5% tolerance on the IOVCC33 power supply is recommended.

DC Power Supply Pin Specifications

Total Power versus Power-Down Modes

				Typ[3]		Max[4]			
Symbol	**Parameter**	**Mode**	**Frequency**	**3.3V**	**1.8V**	**3.3V**	**1.8V**	**Units**	**Notes**
I_{PDQ3}	Complete Power-Down Current	A	X			4	0	mA	1, 6
I_{PDS}	Sleep Power-down Current	B	27 MHz			5	4	mA	2, 7
			74.25 MHz			6	4	mA	
			150 MHz			4	4	mA	
			225 MHz			7	5	mA	
I_{STBY}	Standby Current	C	27 MHz			13	6	mA	2, 8
			74.25 MHz			13	6	mA	
			150 MHz			11	6	mA	
			225 MHz			11	6	mA	
I_{UNS}	Unselected Current	D	27 MHz	15	25	19	33	mA	2, 9
			74.25 MHz	17	27	21	34	mA	
			150 MHz	16	28	18	36	mA	
			225 MHz	18	30	23	39	mA	
I_{CCTD}	Full Power Digital Out Current	E	27 MHz	81	76	105	88	mA	2, 10
			74.25 MHz	100	160	165	181	mA	
			150 MHz	123	279	247	337	mA	
			225 MHz	139	394	316	472	mA	

Notes:

1. Power is not related to input TMDS clock (RxC) frequency because the selected TMDS port is powered down.
2. Power is related to input TMDS clock (RxC) frequency at the selected TMDS port. Only one port can be selected.
3. Typical power specifications measured with supplies at typical normal operating conditions; and a video pattern that combines gray scale, checkerboard and text.
4. Maximum power limits measured with supplies at maximum normal operating conditions; minimum normal operating ambient temperature; and a video pattern single-pixel vertical lines.
5. Registers are always accessible on local I^2C (CSDA/CSCL) without active link clock.
6. Power Down Mode A: Minimum power. Everything is powered off. Host sees no termination of TMDS signals at either TMDS port. I2C access is still available.
7. Power Down Mode B: Powers down as in Mode C, but also powers down SCDT logic. CKDT state can be polled in register, but interrupts and the INT output pin are inactive. Host device can sense TMDS termination.
8. Power Down Mode C: Powers down core logic, ACR PLL and output pins. HDCP does not continue. Interrupts disabled. INT pin show state of SCDT for the selected TMDS port.
9. Power Down Mode D: Monitor SCDT on selected TMDS port with outputs tri-stated. HDCP continues in the selected port, but the output of the HDMI Receiver can be connected to a shared bus.
10. Digital Functional Mode E: Full Operation on one port with digital outputs

Power Down Mode Definitions

Mode		Bit States					Description
		PDTOT#	PD_12CH#	PD Clks [1]	PD Outs [2]	PD#	
A	Power Down	0	X	X	X	X	Minimum power. Everything is powered off. Host sees no termination of TMDS signals at either TMDS port. I^2C access is still available.
B	Sleep Mode Power	1	0	0	X	0	Powers down as in Mode C, but also powers down SCDT logic. CKDT state can be polled in register, but interrupts and the INT output pin are inactive. Host device can sense TMDS termination.
C	Standby Power	1	1	1	1	0	Powers down core logic, ACR PLL and output pins. HDCP does not continue. Interrupts disabled. INT pin show state of SCDT for the selected TMDS port.
D	Unselected Power	1	1	1	0	1	Monitor SCDT on selected TMDS port with outputs tri-stated. HDCP continues in the selected port, but the output of the HDMI Receiver can be connected to a shared bus.
E	Digital	1	1	1	1	1	Full operation on one port with digital outputs.

Notes:

1. PD Clks includes PD_MCLK#, PD_XTAL#, PD_APLL# and PD_PCLK# all set to zero.
2. PD Outs includes PD_AO#, and PD_VO# all set to zero.

AC Specifications

TMDS Input Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{DPS}	Intra-Pair Differential Input Skew				T_{BIT}	ps		2, 4
T_{CCS}	Channel to Channel Differential Input Skew				T_{CIP}	ns	Figure 11	2, 3
F_{RXC}	Differential Input Clock Frequency		25		225	MHz		
T_{RXC}	Differential Input Clock Period		4.44		40	ns		
T_{IJIT}	Differential Input Clock Jitter tolerance (0.3Tbit)	74.25 MHz			400	ps		2, 5, 6

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L=10pF.
2. Guaranteed by design.
3. IDCK Period (see applicable SiI HDMI Transmitter Data Sheet).
4. 1/10 of IDCK Period (see applicable SiI HDMI Transmitter Data Sheet).
5. Jitter defined per HDMI Specification
6. Jitter measured with Clock Recovery Unit per HDMI Specification. Actual jitter tolerance can be higher depending on the frequency of the jitter.

Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for more details on controlling timing modes.

Video Output Timings

12/15/18-Bit Data Output Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	Low-to-High Rise Time Transition	C_L=10pF			3	ns	Figure 14	2
D_{HLT}	High-to-Low Fall Time Transition	C_L=10pF			3	ns	Figure 14	2
R_{CIP}	ODCK Cycle Time	C_L=10pF	13		40	ns	Figure 15	8
F_{CIP}	ODCK Frequency	C_L=10pF	25		82.5	MHz		5
T_{DUTY}	ODCK Duty Cycle	C_L=10pF	40%		60%	R_{CIP}	Figure 15	3
T_{CK2OUT}	Clock-to-Output Delay	C_L=10pF	0.8		3.8	ns	Figure 15	

16/20/24/30/36-Bit Data Output Timings

Symbol	Parameter		Conditions	Min	Typ	Max	Units	Figure	Notes
D_{LHT}	Low-to-High Rise Time Transition		C_L=10pF			3	ns	Figure 14	2
D_{HLT}	High-to-Low Fall Time Transition		C_L=10pF			3	ns	Figure 14	2
T_{DUTY}	ODCK Duty Cycle		C_L=10pF	40%		60%	R_{CIP}	Figure 15	3
T_{CK2OUT}	ODCK-to-Output Delay		C_L=10pF	0.92		2.9	ns	Figure 15	
R_{CIP}	Output Clock Cycle Time	SiI9135CTU	C_L=10pF	6.06		40	ns	Figure 15	5, 8
F_{CIP}	Output Clock Frequency	SiI9135CTU	C_L=10pF	25		165	MHz	Figure 15	5

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L=10pF.
2. Rise time and fall time specifications apply to HSYNC, VSYNC, DE, ODCK, EVNODD and Q[35:0].
3. Output clock duty cycle is independent of the differential input clock duty cycle. Duty cycle is a component of output setup and hold times.
4. See Table 11 on page 32 for calculation of worst case output setup and hold times.
5. All output timings are defined at the maximum operating ODCK frequency, F_{CIP}, unless otherwise specified.
6. F_{CIP} can be the same as F_{RXC} or one-half of F_{RXC}, depending on OCLKDIV setting. F_{CIP} can also be F_{RXC} /1.25 or F_{RXC} /1.5 if deep color mode is being transmitted.
7. R_{CIP} is the inverse of F_{CIP} and is not a controlling specification.
8. Output skew specified when ODCK is programmed to divide-by-two mode.

Audio Output Timings

I²S Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{tr}	SCK Clock Period (TX)	C_L=10pF	1.00			T_{tr}	Figure 16	1
T_{HC}	SCK Clock HIGH Time	C_L=10pF	0.35			T_{tr}		1
T_{LC}	SCK Clock LOW Time	C_L=10pF	0.35			T_{tr}		1
T_{SU}	Setup Time, SCK to SD/WS	C_L=10pF	$0.4T_{TR}$ - 5			ns		1
T_{HD}	Hold Time, SCK to SD/WS	C_L=10pF	$0.4T_{TR}$ - 5			ns		1
$T_{SCKDUTY}$	SCK Duty Cycle	C_L=10pF	40%		60%	T_{tr}		1
T_{SCK2SD}	SCK to SD or WS Delay	C_L=10pF	-5		+5	ns		2
T_{AUDDLY}	Audio Pipeline Delay			40	80	µs		

Notes:

1. Refer to Figure 16. Meets timings in Philips I²S Specification.
2. Applies also to SDC-to-WS delay.

S/PDIF Output Port Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{SPCYC}	SPDIF Cycle Time	C_L=10pF		1.0		UI	Figure 17	1, 2
F_{SPDIF}	SPDIF Frequency	—	4		24	MHz		3
T_{SPDUTY}	SPDIF Duty Cycle	C_L=10pF	90%		110%	UI		2, 5
$T_{MCLKCYC}$	MCLK Cycle Time	C_L=10pF	20		250	ns	Figure 18	1, 2, 4
F_{MCLK}	MCLK Frequency	C_L=10pF	4		50	MHz		1, 2, 4
$T_{MCLKDUTY}$	MCLK Duty Cycle	C_L=10pF	40%		60%	$T_{MCLKCYC}$		2, 4
T_{AUDDLY}	Audio Pipeline Delay			40	80	µs		

Notes:

1. Guaranteed by design.
2. Proportional to unit time (UI), according to sample rate.
3. SPDIF is not a true clock, but is generated from the internal 128Fs clock, for Fs from 128 to 512 kHz.
4. MCLK refers to MCLKOUT.
5. Intrinsic jitter on S/PDIF output can limit its use as a S/PDIF transmitter. The S/PDIF intrinsic jitter is approximately 0.1UI.

Audio Crystal Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
F_{XTAL}	External Crystal Freq.		26	27	28.5	MHz	Figure 9	1, 2

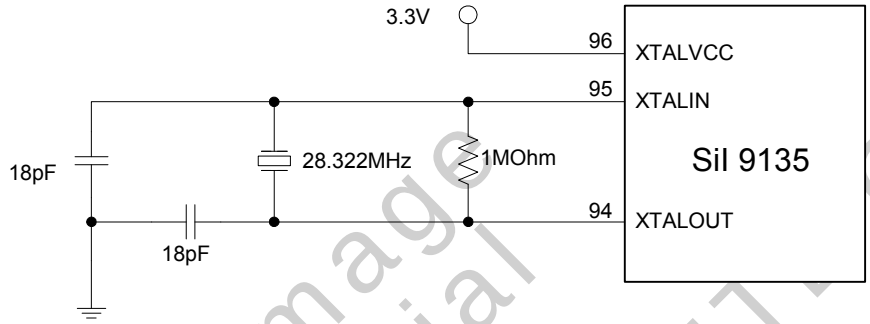


Figure 9. Audio Crystal Schematic for the SiI9135

Notes:

1. The HDMI Receiver has been fully characterized for optimum audio quality using 28.322 MHz. Use Citizen part number CSA309-28.322MABJ crystal or equivalent. A less expensive, but not fully characterized circuit, can use a TTL level clock source.
2. The XTALIN/XTALOUT pin pair must be driven with a clock in all applications.

Miscellaneous Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{I2CDVD}	SDA Data Valid delay from SCL falling edge	C_L=400pF			700	ns		
F_{DDC}	Speed on TMDS DDC Ports	C_L=400pF			100	kHz		2
F_{I^2C}	Speed on Local I^2C Port	C_L=400pF			400	kHz		3
T_{RESET}	RESET# Signal Low Time for valid reset		90			ms	Figure 13	
$T_{BKSVINIT}$	HDCP BKSV Load Time				2.2	ms		4

Notes:

1. Under normal operating conditions unless otherwise specified, including output pin loading of C_L=10 pF.
2. DDC ports are limited to 100 kHz by the HDMI Specification, and meet I^2C standard mode timings.
3. Local I^2C port (CSCL/CSDA) meet standard mode I^2C timing requirements to 400 kHz.
4. The time required to load the KSV values internal to the HDMI Receiver after a RESET# and the start of receive an active TMDS clock. An attached HDCP host device should not attempt to read the HDMI Receiver's BKSV values until after this time. The $T_{BKSVINIT}$ Min and Max values are based on the maximum and minimum allowable XCLK frequencies. The loading of the BKSV values requires a valid XCLK and TMDS clock.

Interrupt Timings

Interrupt Output Pin Timings

Symbol	Parameter	Conditions	Min	Typ	Max	Units	Figure	Notes
T_{FSC}	Link disabled (DE inactive) to SCDT low			0.15	40	ms	Figure 10	1, 2, 3, 8
T_{HSC}	Link enabled (DE active) to SCDT high				4	DE	Figure 10	1, 2, 4, 8
T_{CICD}	RXC inactive to CKDT low				100	µs	Figure 10	1, 2, 8
T_{CACD}	RXC active to CKDT high				10	µs	Figure 10	1, 2, 8
T_{INT}	Response Time for INT from Input Change				100	µs		1, 5, 8
T_{CIOD}	RXC inactive to ODCK inactive				100	ns		1, 8
T_{CAOD}	RXC active to ODCK active and stable				10	ms		1, 6, 8
T_{SRRF}	Delay from SCDT rising edge to Software Reset falling edge				100	ms	Figure 13	7

Notes:

1. Guaranteed by design.
2. SCDT and CKDT are register bits in this device.
3. SCDT changes to LOW after DE is HIGH for approximately 4096 pixel clock cycles, or after DE is LOW for approximately 1,000,000 clock cycles. At 27 MHz pixel clock, this delay for DE HIGH is approximately 150 µs, and the delay for DE LOW is approximately 40 ms.
4. SCDT changes to HIGH when clock is active (T_{CACD}) and at least 4 DE edges have been recognized. At 720p, the DE period is 22 µs, so SCDT responds approximately 50 µs after T_{CACD}.
5. The INT pin changes state after a change in input condition when the corresponding interrupt is enabled.
6. Output clock (ODCK) becomes active before it becomes stable. Use the SCDT signal as the indicator of stable video output timings, as this depends on decoding of DE signals with active RXC (see T_{FSC}).
7. Software Reset must be asserted and then deasserted within the specified maximum time after rising edge of Sync Detect (SCDT). Access to both SWRST and SCDT can be limited by the speed of the I^2C connection.
8. SCDT is HIGH only when CKDT is also HIGH. When the HDMI Receiver is in a powered-down mode, the INT output pin indicates the current state of SCDT. Thus, a power-down HDMI Receiver signals a micro connected to the INT pin whenever SCDT changes from LOW to HIGH or HIGH to LOW

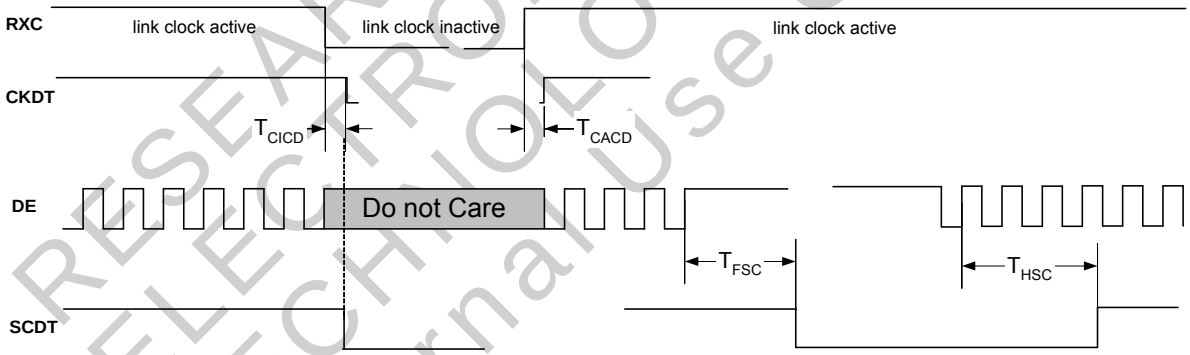


Figure 10. SCDT and CKDT Timing from DE or RXC Inactive/Active

Notes:

1. The SCDT shown in Figure 10 is a register bit. SCDT remains HIGH if DE is stuck in LOW while RXC remains active, but SCDT changes to LOW if DE is stuck HIGH while RXC remains active.
2. The CKDT shown in Figure 10 is a register bit. CKDT changes to LOW whenever RXC stops, and changes to HIGH when RXC starts. SCDT changes to LOW when CKDT changes to LOW.
3. SCDT changes to LOW when CKDT changes to LOW. SCDT changes to HIGH at T_{HSC} after CKDT changes to HIGH.
4. The INT output pin changes state after the SCDT or CKDT register bit is set or cleared if those interrupts are enabled.

Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for more details on controlling timing modes.

Timing Diagrams

TMDS Input Timing Diagrams

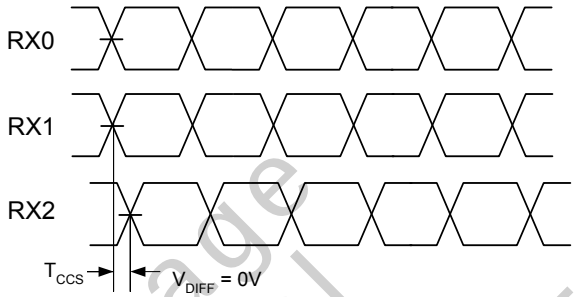


Figure 11. TMDS Channel-to-Channel Skew Timing

Power Supply Control Timings

Power Supply Sequencing

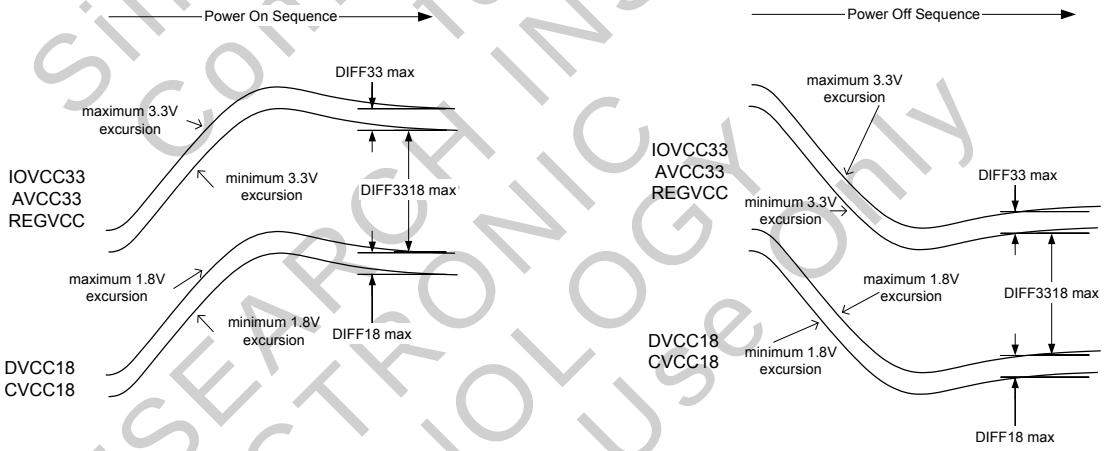
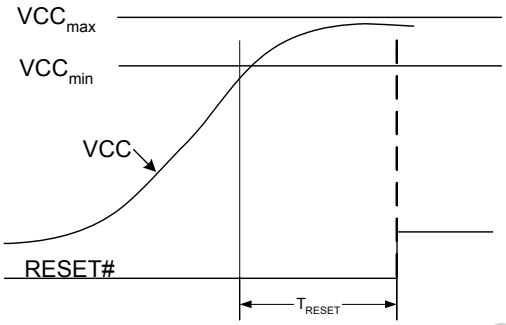
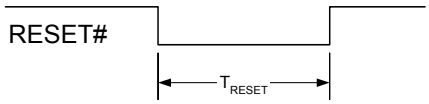


Figure 12. Power Supply Sequencing

Reset Timings



Note that VCC must be stable between its limits for Normal Operating Conditions for T_{RESET} before RESET# is high.



RESET# must be pulled LOW for T_{RESET} before accessing registers. This can be done by holding RESET# LOW until T_{RESET} after stable power (at left); OR by pulling RESET# LOW from a HIGH state (at right) for at least T_{RESET}.

Figure 13. RESET# Minimum Timings

Digital Video Output Timing Diagrams

Output Transition Times

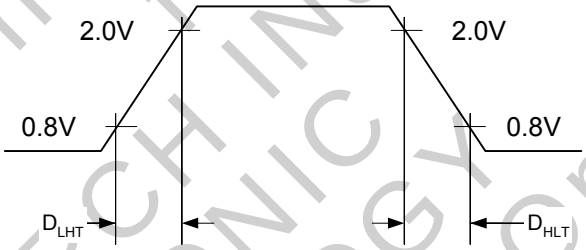


Figure 14. Video Digital Output Transition Times

Output Clock to Output Data Delay

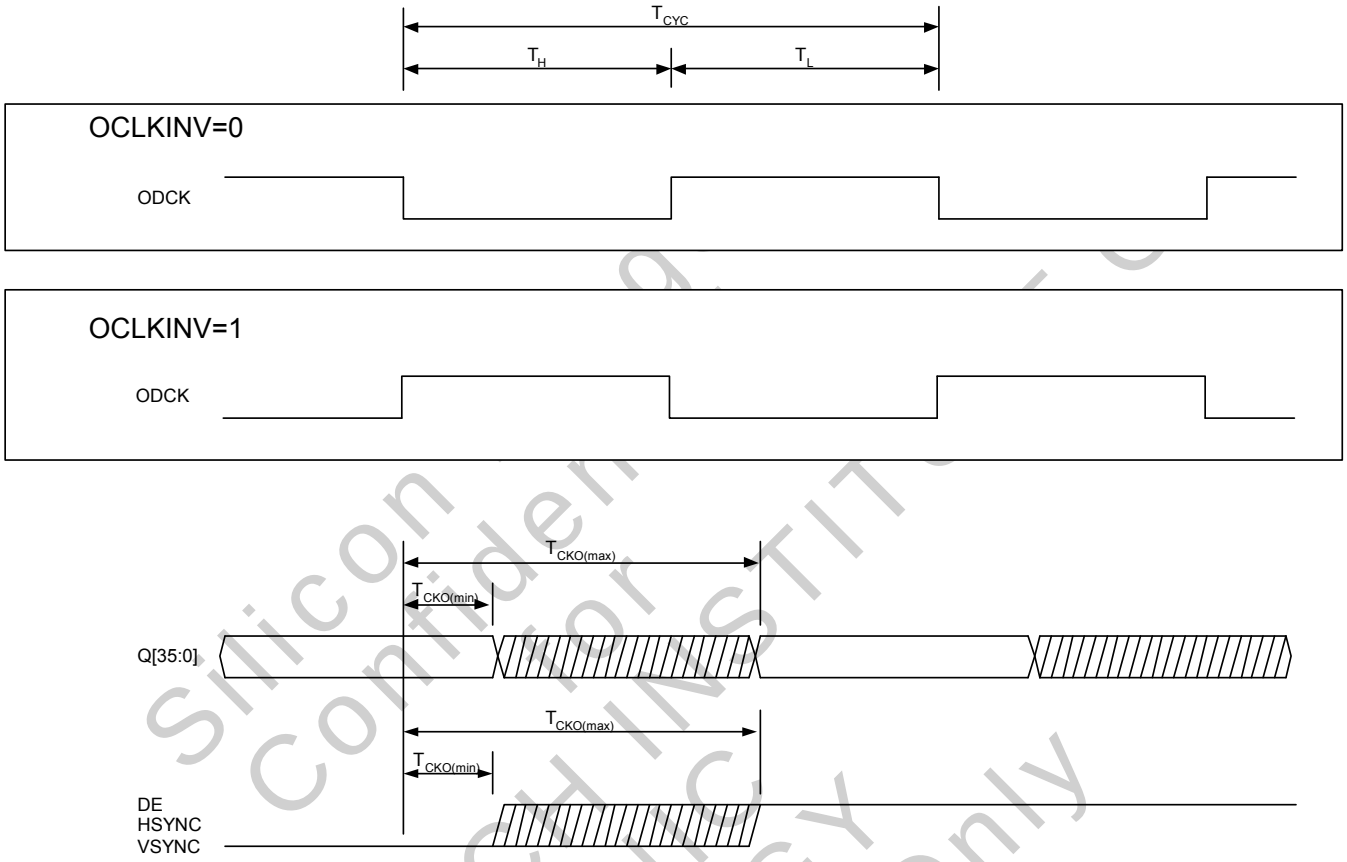


Figure 15. Receiver Clock-to-Output Delay and Duty Cycle Limits

Digital Audio Output Timings

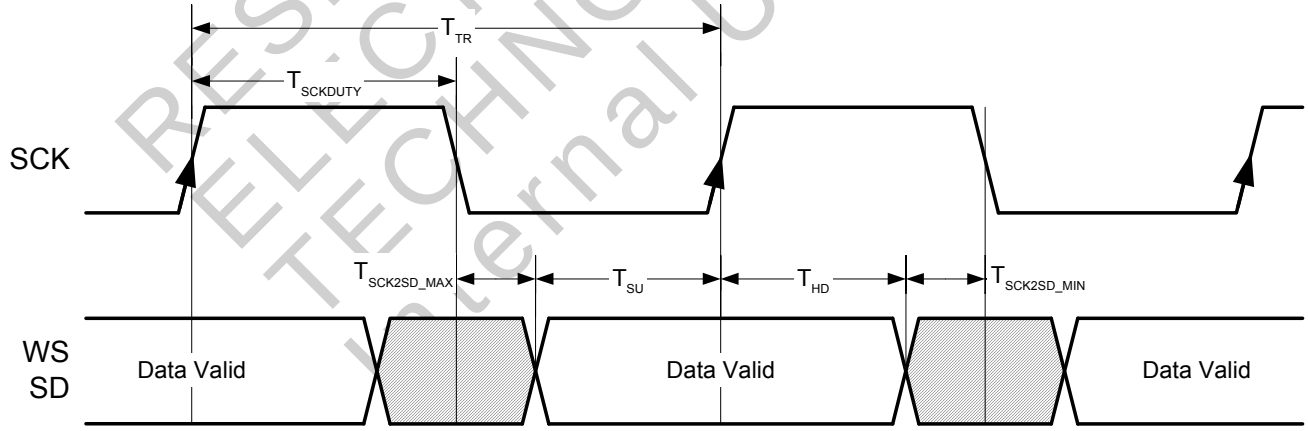


Figure 16. I²S Output Timings

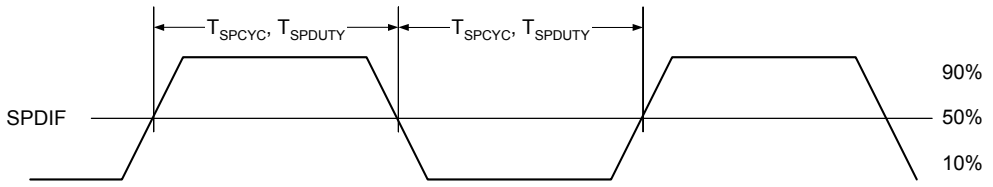


Figure 17. S/PDIF Output Timings

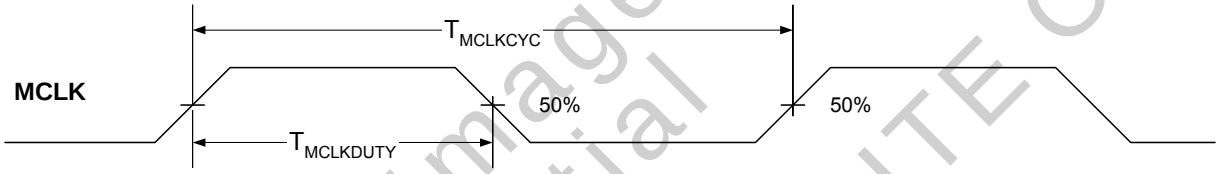


Figure 18. MCLK Timings

Calculating Setup and Hold Times for Video Bus

24/30/36-Bit Mode

Output data is clocked out on one rising (or falling) edge of ODCK, and would then be captured downstream using the same polarity ODCK edge one clock period later. The setup time of data to ODCK and hold time of ODCK to data are therefore a function of the worst case ODCK to output delay. This is shown in Figure 20. The falling active ODCK edge is shown with an arrowhead. For OCK_INV=1, reverse the logic.

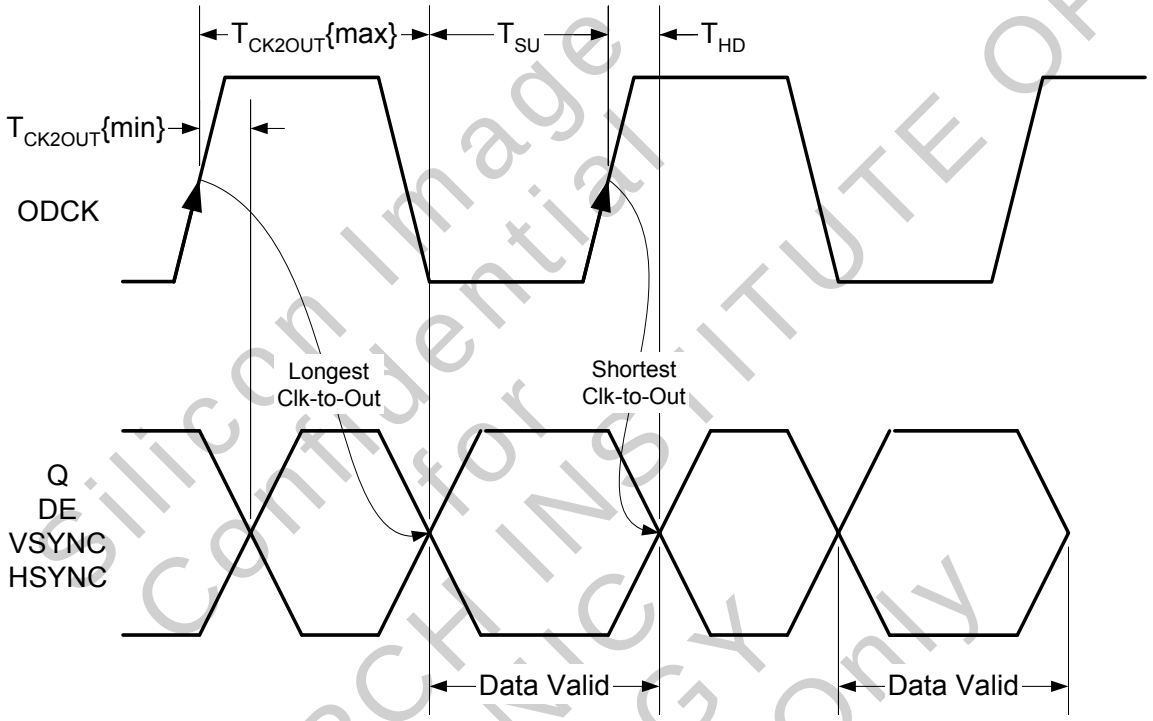


Figure 19. 24/30/36-Bit Mode Receiver Output Setup and Hold Times

Table 10 shows minimum calculated setup and hold times for commonly used ODCK frequencies. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10pF. These are approximations. Hold time is not related to ODCK frequency.

Table 10. Calculation of 24/30/36-Bit Output Setup and Hold Times

	Symbol	Parameter	T_{ODCK}		Min
24/30/36-Bit Mode	T_{SU}	Setup Time to ODCK	27 MHz	37.0 ns	33.2 ns
		$=T_{ODCK}-T_{CK2OUT}${max}	74.25 MHz	13.5 ns	9.7 ns
	T_{HD}	Hold Time from ODCK = T_{CK2OUT}{min}	27 MHz	37.0 ns	0.8 ns

12/15/18-Bit Dual-Edge Mode

Output data is clocked out on each edge of ODCK (both rising and falling), and would then be captured downstream using the opposite ODCK edge. The setup time of data to ODCK is a function of the shortest duty cycle and the longest ODCK to output delay. The hold time does not depend on duty cycle (since every edge is used), and is a function only of the longest ODCK to output delay.

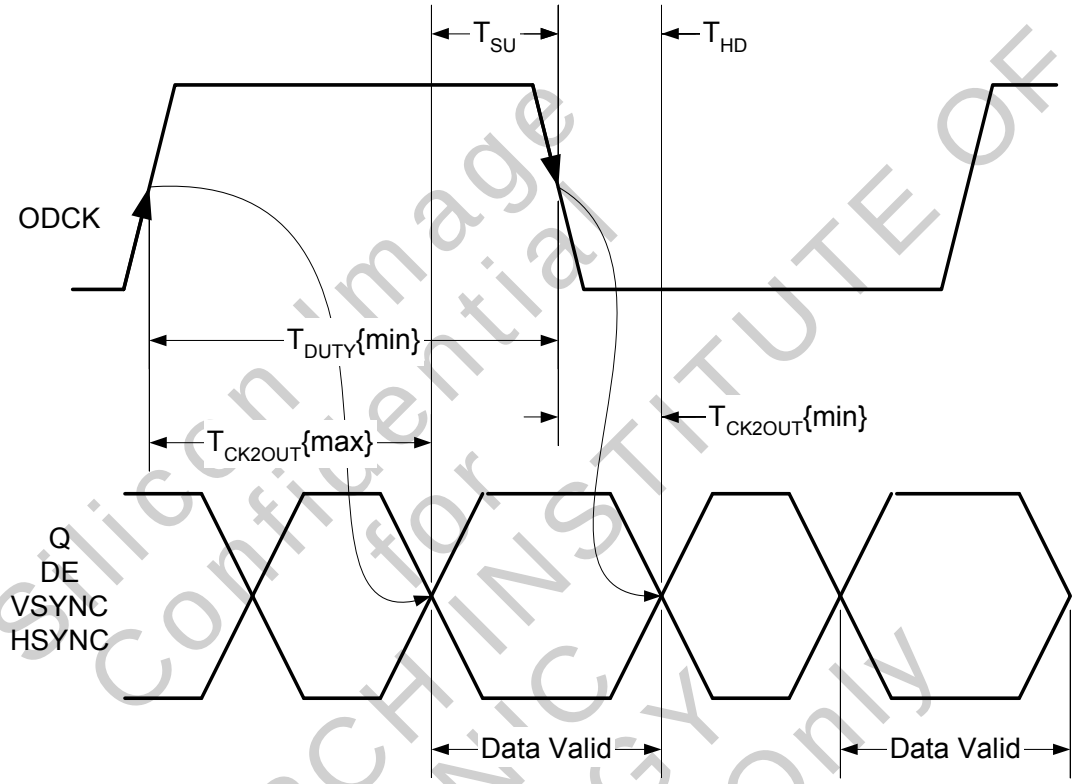


Figure 20. 12/15/18-Bit Mode Receiver Output Setup and Hold Times

Table 11 shows minimum calculated setup and hold times for commonly used ODCK frequencies, up to the maximum allowed for 12/15/18-bit mode. The setup and hold times apply to DE, VSYNC, HSYNC and Data output pins, with output load of 10pF. These are approximations. Hold time is not related to ODCK frequency.

Table 11. Calculation of 12/15/18-Bit Output Setup and Hold Times

	Symbol	Parameter	T_{ODCK}		Min
12/15/18-Bit Mode	T_{SU}	Setup Time to ODCK $=T_{ODCK}*T_{DUTY}${min}$-T_{CK2OUT}${max}	27 MHz	37.0 ns	34.1 ns
			74.25 MHz	13.5 ns	10.6 ns
	T_{HD}	Hold Time from ODCK = T_{CK2OUT}{min}	27 MHz	37.0 ns	0.8ns

Calculating Setup and Hold Times for I²S Audio Bus

Valid serial data is available at Tsck2sd after the falling edge of the first SCK cycle, and then captured downstream using the active rising edge of SCK one clock period later. The setup time of data to SCK (Tsu) and hold time of SCK to data (Thd) are therefore a function of the worst case SCK-to-output data delay (Tsck2sd). Figure 16 illustrates this timing relationship. Note that the active SCK edge (rising edge) is shown with an arrowhead. For a falling edge sampling clock, the logic is reversed.

Table 12 shows the setup and hold time calculation examples for various audio sample frequencies. The formula used in these examples also applies when calculating the setup and hold times for other audio sampling frequencies.

Table 12. I²S Setup and Hold Time Calculations

Symbol	Parameter	FWS (kHz)	FSCLK (MHz)	Ttr	Min
T_{SU}	Setup Time, SCK to SD/WS $= T_{TR} – (T_{SCKDUTY\_WORST} + T_{SCK2SD\_MAX})$ $= T_{TR} – (0.6T_{TR} + 5ns)$ $= 0.4T_{TR} - 5ns$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns
T_{HD}	Hold Time, SCK to SD/WS $= (T_{SCKDUTY\_WORST} - T_{SCK2SD\_MIN})$ $= 0.4T_{TR} - 5ns$	32 kHz	2.048	488 ns	190 ns
		44.1 kHz	2.822	354 ns	136 ns
		48 kHz	3.072	326 ns	125 ns
		96 kHz	6.144	163 ns	60 ns
		192 kHz	12.288	81 ns	27 ns

Note: The sample calculations shown in Table 12 are based on WS=64 SCLK rising edges.

144-Pin TQFP Pin Descriptions

Digital Video Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
Q0	16	8 mA	LVTTL	Output	36-Bit Output Pixel Data Bus. Q35:0 is highly configurable using the VDD_CONFIG register. It supports a wide array of output formats, including multiple RBG and YCbCr bus formats. Using the appropriate bits in the PD register, the output drivers can be put into a high impedance (tri-state) mode. A weak, internal pull-down device brings each output to ground.
Q1	15		LVTTL	Output	
Q2	14		LVTTL	Output	
Q3	13		LVTTL	Output	
Q4	10		LVTTL	Output	
Q5	9		LVTTL	Output	
Q6	8		LVTTL	Output	
Q7	7		LVTTL	Output	
Q8	3		LVTTL	Output	
Q9	2		LVTTL	Output	
Q10	1		LVTTL	Output	
Q11	144		LVTTL	Output	
Q12	141		LVTTL	Output	
Q13	140		LVTTL	Output	
Q14	139		LVTTL	Output	
Q15	138		LVTTL	Output	
Q16	135		LVTTL	Output	
Q17	134		LVTTL	Output	
Q18	133		LVTTL	Output	
Q19	132		LVTTL	Output	
Q20	129		LVTTL	Output	
Q21	128		LVTTL	Output	
Q22	127		LVTTL	Output	
Q23	126		LVTTL	Output	
Q24	123		LVTTL	Output	
Q25	122		LVTTL	Output	
Q26	121		LVTTL	Output	
Q27	120		LVTTL	Output	
Q28	117		LVTTL	Output	
Q29	116		LVTTL	Output	
Q30	115		LVTTL	Output	
Q31	114		LVTTL	Output	
Q32	111		LVTTL	Output	
Q33	110		LVTTL	Output	
Q34	109		LVTTL	Output	
Q35	108		LVTTL	Output	
DE	19	8 mA	LVTTL	Output	Data Enable.
HSYNC	20	8 mA	LVTTL	Output	Horizontal Sync Output
VSYNC	21	8 mA	LVTTL	Output	Vertical Sync Output
EVNODD	22	8 mA	LVTTL	Output	Indicates Even or Odd Field for Interlaced Formats.
ODCK	5	12 mA	LVTTL	Output	Output Data Clock.

Notes:

1. HSYNC and VSYNC outputs carry sync signals for both embedded and explicit sync configurations.
2. When transporting video data that uses fewer than 36 bits, the unused bits on the Q[] bus can still carry switching pixel data signals. Unused Q[35:0] bus pins should be unconnected, masked or ignored by downstream devices. For example, carrying YCbCr 4:2:2 data with 16-bit width (see page 48), the bits Q[0] through Q[7] output switching signals.
3. The output data bus, Q0 to Q35, can be wire-ORed to another device such that one device is always tri-stated. However, the Q0-Q35 pins do not have bus hold internal pull-ups or pull-downs, and so cannot pull the bus when all connected devices are tri-stated.

Digital Audio Output Pins

Pin Name	Pin #	Strength	Type	Dir	Description
XTALIN	95	—	5V Tolerant LVTTL	In	Crystal Clock Input. Also allows LVTTL input. Frequency required: 26-28.5 MHz
XTALOUT	94	4 mA	LVTTL	Out	Crystal Clock Output
MCLK	89	8 mA	LVTTL	Out	Audio Master Clock Output
SCK/DCLK	86	4 mA	LVTTL	Out	I^2S Serial Clock Output.
					DSD Clock Out.
WS/DR0	85	4 mA	LVTTL	Out	I^2S Word Select Output.
					DSD Serial Right Ch0 Data Output
SD0/DL0	81	4 mA	LVTTL	Out	I^2S Serial Data Output / DSD Audio Output Configurable to be shared with DSD. SD0 = DSD Serial Left Ch0 Data Output SD1 = DSD Serial Right Ch1 Data Output SD2 = DSD Serial Left Ch1 Data Output
SD1/DR1	82	4 mA	LVTTL	Out	
SD2/DL1	83	4 mA	LVTTL	Out	
SD3/DR2	84	4 mA	LVTTL	Out	
SPDIF/DL2	78	4 mA	LVTTL	Out	S/PDIF Audio Output. Configurable to be shared with DSD
					DSD Serial Left Ch2 Data Output
MUTEOUT	75	4 mA	LVTTL	Out	Mute Audio Output. Signal to the external downstream audio device, audio DAC, etc. to mute audio output.

Note: The XTALIN pin can either be driven at LVTTL levels by a clock (leaving XTALOUT unconnected), or connected through a crystal to XTALOUT. Refer to the schematic on page 70.

Configuration/Programming Pins

Pin Name	Pin #	Strength	Type	Dir	Description
INT	102	4 mA	LVTTL	Out	Interrupt Output. Configurable polarity and push-pull output. Multiple sources of interrupt can be enabled through the INT_EN register. See Note 1.
RESET#	100	—	Schmitt	In	Reset Pin. Active LOW. 5V Tolerant
DSCL0	34	—	SchmittOD	In	DDC I^2C Clock for Port 0. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C port during authentication. True open drain, so does not pull to GND if R0PWR5V is not applied.
DSDA0	33	3 mA	SchmittOD	Bi-Di	DDC I^2C Data for Port 0. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C during authentication. True open drain, so does not pull to GND if R0PWR5V is not applied.
DSCL1	29	—	SchmittOD	In	DDC I^2C Clock for Port 1. 5V Tolerant. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C port during authentication. True open drain, so does not pull to GND if R1PWR5V is not applied.
DSDA1	28	3 mA	SchmittOD	Bi-Di	DDC I^2C Data for Port 1. 5V Tolerant. 5V Tolerant. HDCP KSV, An and Ri values are exchanged over an I^2C port during authentication. True open drain, so does not pull to GND if R1PWR5V is not applied.
CSCL	27	—	Schmitt	In	Configuration/Status I^2C Clock. 5V Tolerant. Chip configuration/status, CEA-861 support and downstream HDCP repeater-specific registers are accessed via this I^2C port. True open drain, so does not pull to GND if power is not applied.
CSDA	26	3 mA	Schmitt	Bi-Di	Configuration/Status I^2C Data. 5V Tolerant. Chip configuration/status, CEA-861 support and downstream HDCP repeater-specific registers are accessed via this I^2C port. True open drain, so does not pull to GND if power is not applied.
CI2CA	105		LLVTTL	In	Local I^2C Address Select. 5V Tolerant. Low = Addresses 0x60/0x68 High = Addresses 0x62/0x6A
SCDT	101	12 mA	LVTTL	Out	Indicates Active Video at HDMI Input Port. Sync detection indicator.
R0PWR5V	35	—	LVTTL	In	Port 0 Transmitter Detect. 5V Tolerant. Used for MUTEIN function. See Note 2, 3.
R1PWR5V	30	—	LVTTL	In	Port 1 Transmitter Detect. 5V Tolerant. Used for MUTEIN function. See Note 2,3.
RSVDNC	98, 77, 76, 55				Reserved, must be left unconnected
RSVDL	99			In	Reserved, must be tied to ground

Note:

1. The INT pin can be programmed to be either a push-pull LVTTL output or an open-drain output.
2. There is no power sequence requirement on RxPWR5V pins.
3. The operation condition of the RxPWR5V pins is 5V +/- 5%.

Differential Signal Data Pins

Pin Name	Pin #	Type	Description	
R0XC+	40	Analog	TMDS Input Clock Pair	HDMI Port 0
R0XC-	39	Analog		
R0X0+	44	Analog	TMDS Input Data Pair	
R0X0-	43	Analog		
R0X1+	48	Analog	TMDS Input Data Pair	
R0X1-	47	Analog		
R0X2+	52	Analog	TMDS Input Data Pair	
R0X2-	51	Analog		
R1XC+	58	Analog	TMDS Input Clock Pair	HDMI Port 1
R1XC-	57	Analog		
R1X0+	62	Analog	TMDS Input Data Pair	
R1X0-	61	Analog		
R1X1+	66	Analog	TMDS Input Data Pair	
R1X1-	65	Analog		
R1X2+	70	Analog	TMDS Input Data Pair	
R1X2-	69	Analog		

Power and Ground Pins

Pin Name	Pin #	Type	Description	Supply
CVCC18	12, 24, 25, 80, 91, 107, 119, 131, 143	Power	Digital Logic VCC	1.8V
CGND	11, 23, 79, 90, 106, 118, 130, 142	Ground	Digital Logic GND	
IOVCC33	6, 18, 32, 74, 88, 104, 113, 125, 137	Power	Input/Output Pin VCC	3.3V
IOGND	4, 17, 31, 73, 87, 103, 112, 124, 136	Ground	Input/Output Pin GND	
AVCC33	38, 42, 46, 50, 56, 60, 64, 68	Power	TMDS Analog VCC 3.3V	3.3V
AGND	36, 41, 45, 49, 53, 59, 63, 67, 71	Ground	TMDS Analog GND	
AVCC18	37, 54, 72	Power	TMDS Analog VCC 1.8V	1.8V
DVCC18	92	Power	Audio Clock Regeneration PLL Analog VCC. Must be connected to 1.8V	1.8V
DGND	93	Ground	Audio Clock Regeneration PLL Analog Ground.	
XTALVCC	96	Power	Audio Clock Regeneration PLL Crystal Oscillator Power. Must be connected to 3.3V	3.3V
REGVCC	97	Power	Audio Clock Regeneration PLL Crystal Regulator Power. Must be connected to 3.3V	3.3V

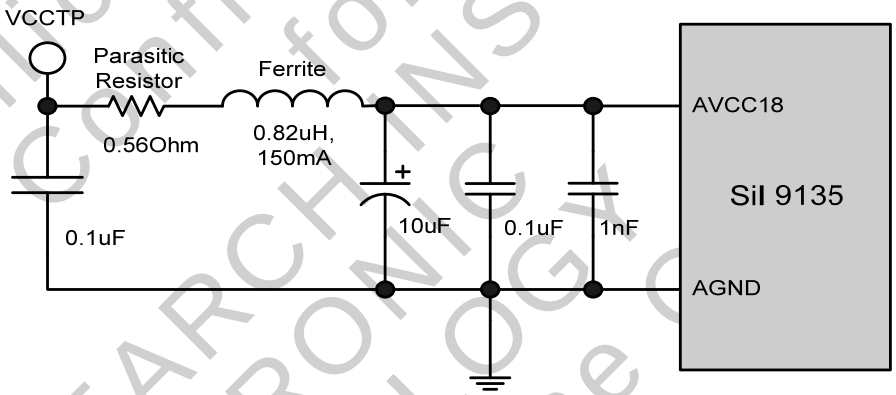


Figure 21. Test Point VCCTP for VCC Noise Tolerance Spec

Notes:

1. The Ferrite (0.82uH, 150mA) attenuates the PLL power supply noise at 10's of KHz and above.
2. The optional parasitic resistor minimizes the peaking. The typical value used here is 0.56 Ohm. 1 Ohm is the maximum.
3. The LC filter can be used to help lowering the cost of the power supplies filter circuit. The separated voltage regulator might not be needed when using the power supply LC filter.

Video Path

The SiI9135 accepts all valid HDMI input formats and can transform that video in a variety of ways to produce the proper video output format. The following pages describe how to control the video path formatting and how to assign output pins for each video output format.

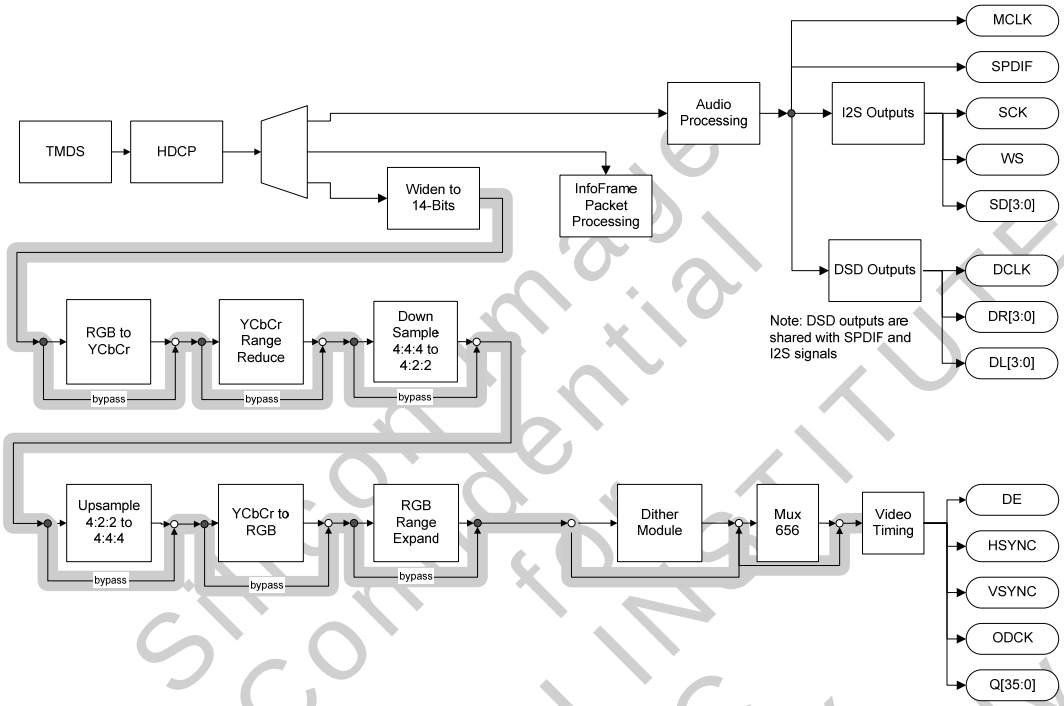


Figure 22. Receiver Video and Audio Data Processing Paths

The processing blocks in the figure above correspond to those shown in Figure 23 through Figure 25.

HDMI Input Modes to SiI9135 Output Modes

The HDMI link supports transport of video in any of three modes: RGB 4:4:4, YCbCr 4:4:4 or YCbCr 4:2:2. The flexible video path in the SiI9135 allows reformatting of video data to a set of output modes. Table 13 lists the supported transformations and points to the Figure for each. In every case, the HDMI link itself carries separate syncs.

Table 13. Translating HDMI Formats to Output Formats

		Output Format						
		Digital						
		RGB 4:4:4	YCbCr 4:4:4	YCbCr 4:2:2	YCbCr 4:2:2	YC Mux	YC Mux	
	Output Syncs	Separate	Separate	Separate	Encoded	Separate	Encoded	Note
HDMI Input Mode	RGB 4:4:4	Figure 23A	Figure 23B	Figure 23C	Figure 23D	Figure 23E	Figure 23F	
	YCbCr 4:4:4	Figure 24A	Figure 24B	Figure 24C	Figure 24D	Figure 24E	Figure 24F	
	YCbCr 4:2:2	Figure 25A	Figure 25B	Figure 25C	Figure 25D	Figure 25E	Figure 25F	

HDMI RGB 4:4:4 Input Processing

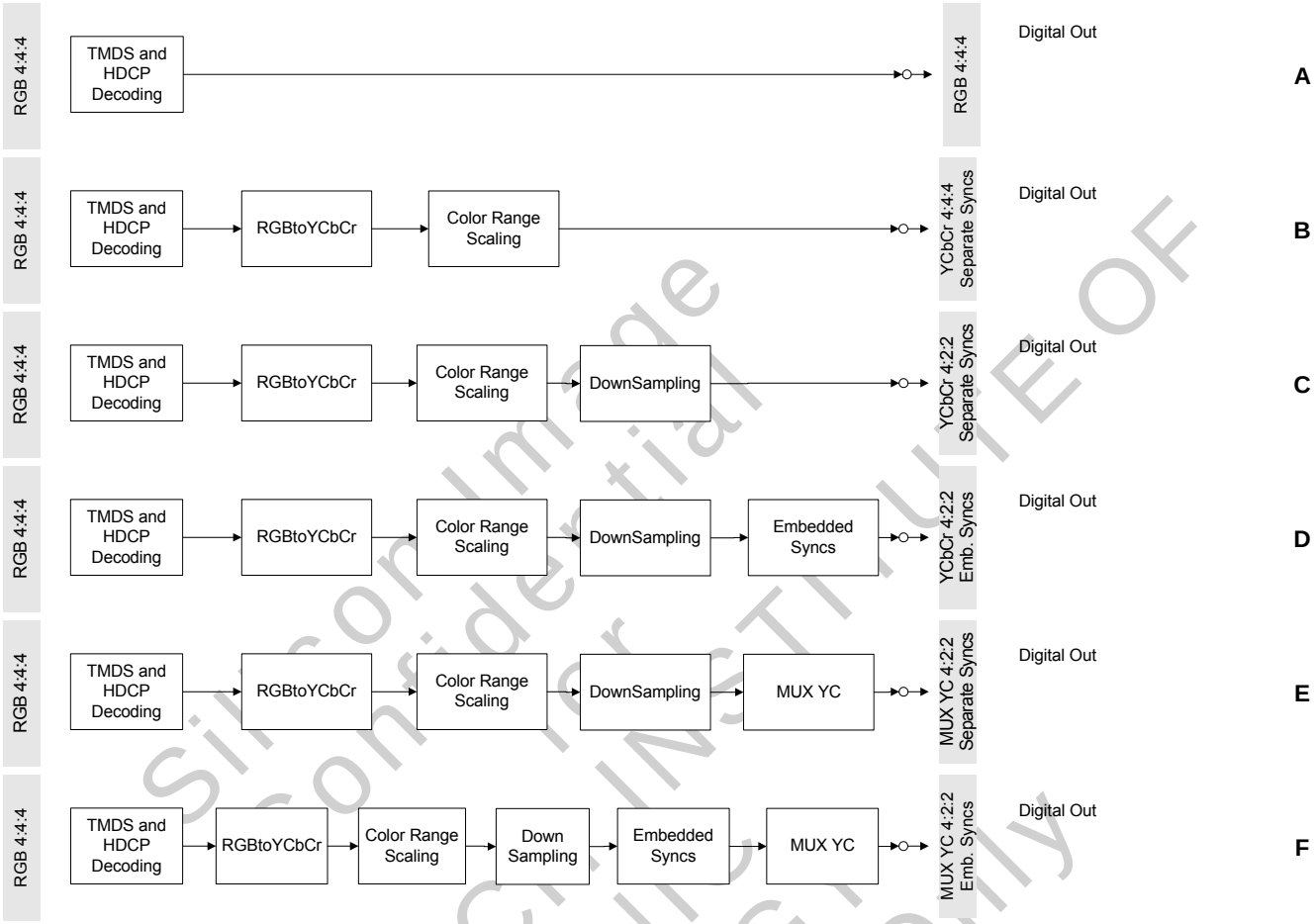


Figure 23. HDMI RGB 4:4:4 Input to Video Output Transformations

HDMI YCbCr 4:4:4 Input Processing

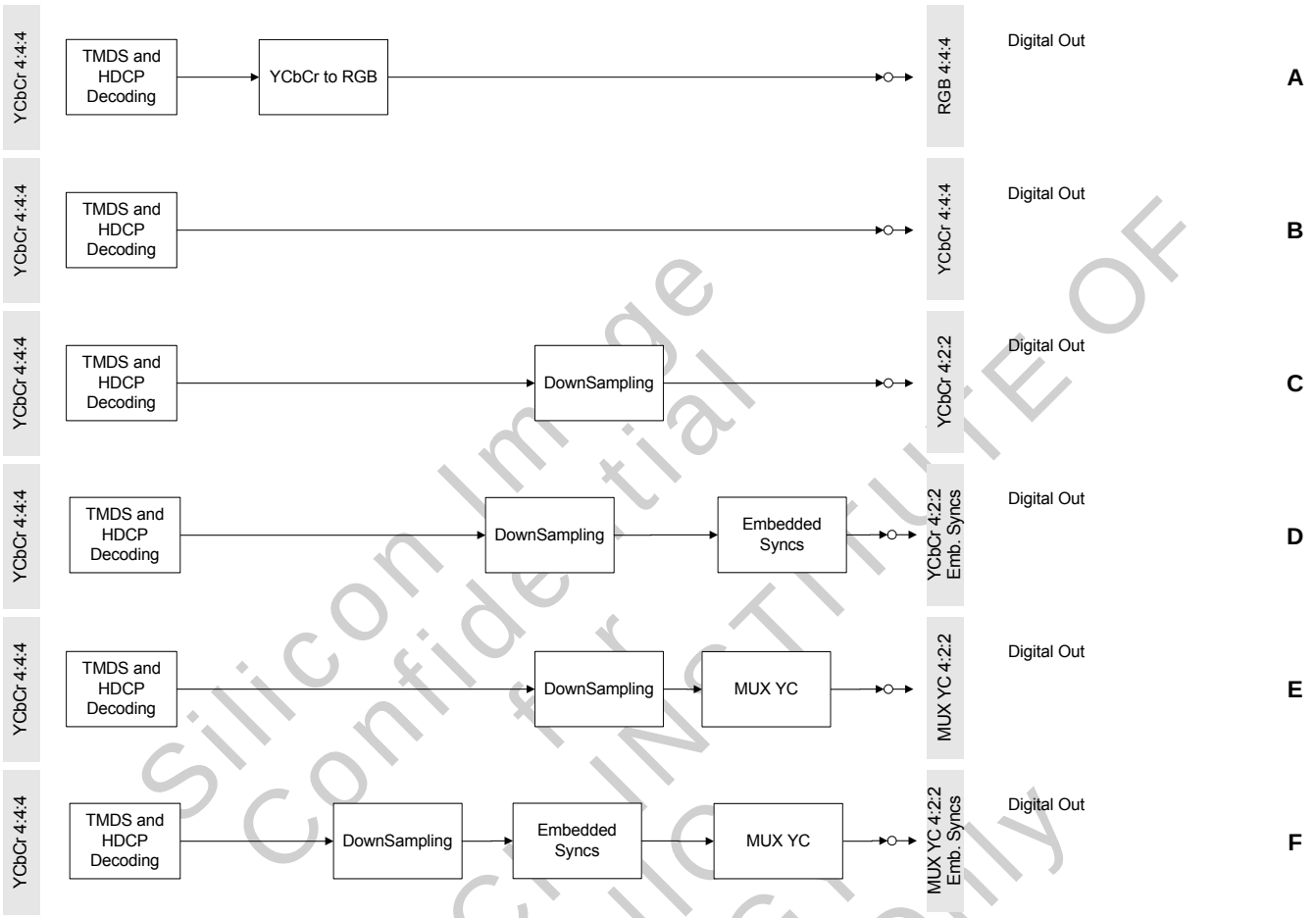


Figure 24. HDMI YCbCr 4:4:4 Input to Video Output Transformations

HDMI YCbCr 4:2:2 Input Processing

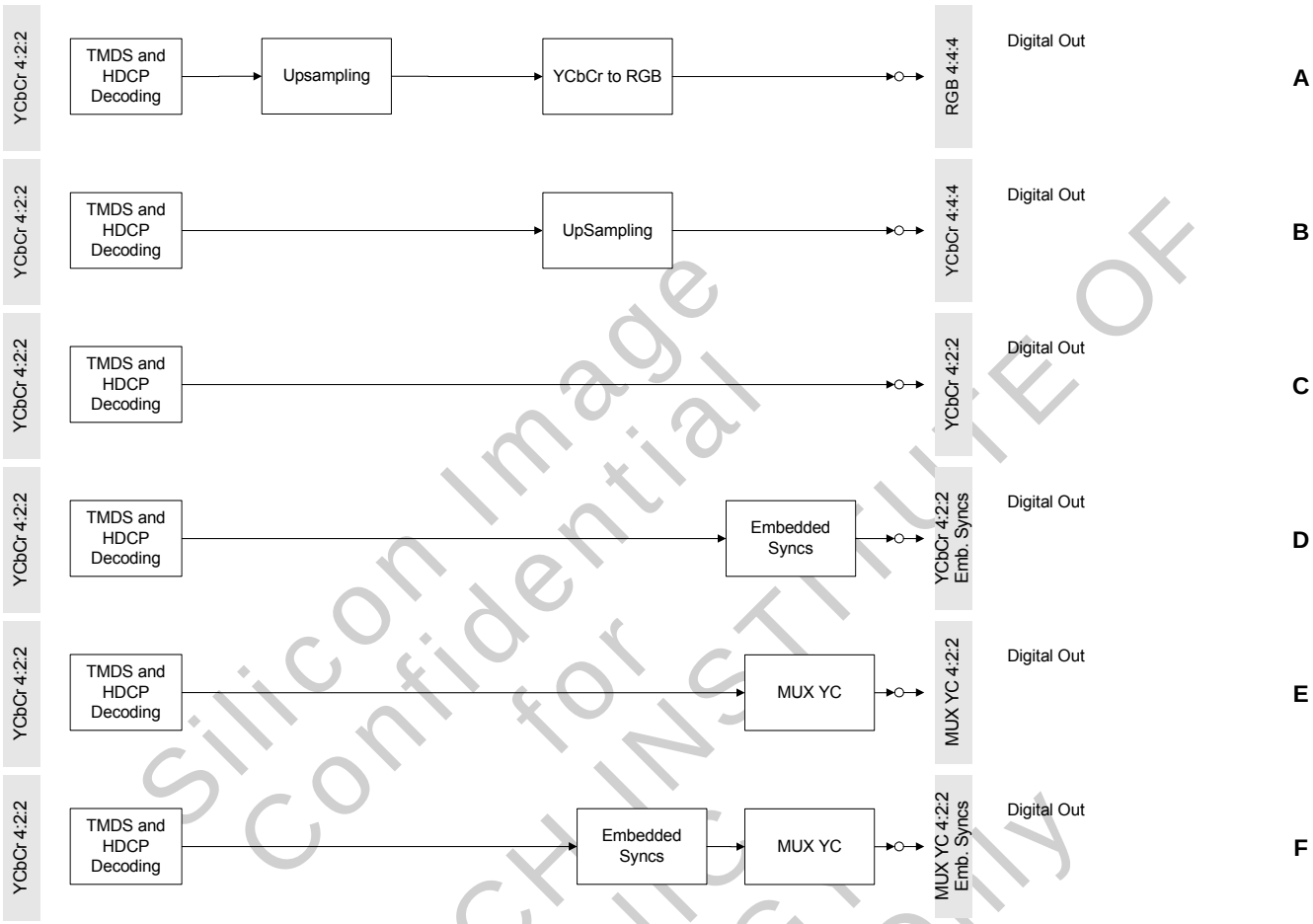


Figure 25. HDMI YCbCr 4:2:2 Input to Video Output Transformations

SiI9135 Output Mode Configuration

The SiI9135 supports multiple output data mappings. Some have explicit control signals while some have embedded control signals. The selection of data mapping mode should be consistent at the pins and in the corresponding register settings. Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for more details.

Table 14. Output Video Formats

Output Mode	Data Widths	Pixel Replication	Syncs	Page	Notes
RGB 4:4:4	24, 30, 36	1x	Explicit	46	3, 7
YCbCr 4:4:4	24, 30, 36	1x	Explicit	46	1, 3, 7
YC 4:2:2 Sep. Syncs	16, 20, 24	1x	Explicit	48	2, 3
YC 4:2:2 Sep. Syncs	16, 20, 24	2x	Explicit	48	2, 3, 8
YC 4:2:2 Emb. Syncs	16, 20, 24	1x	Embedded	51	2, 5
YC MUX 4:2:2	8, 10, 12	2x	Explicit	54	2, 4, 8
YC MUX 4:2:2 Emb. Syncs	8, 10, 12	2x	Embedded	56	2, 5, 6, 8, 9

Notes:

1. YC 4:4:4 data contains one Cr, one Cb and one Y value for every pixel.
2. YC 4:2:2 data contains one Cr and one Cb value for every two pixels; and one Y value for every pixel.
3. These formats can be carried across the HDMI link. Refer to HDMI Specification, Section 6.2.3. The link clock must be within the specified range of the SiI9135.
4. In YC MUX mode data is output on one or two 8/10/12-bit channels.
5. YC MUX with embedded SAV/EAV signal
6. Syncs are embedded using SAV/EAV codes.
7. A 2x clock can also be sent with 4:4:4 data.
8. When sending a 2x clock the HDMI source must also send AVI InfoFrames with an accurate pixel replication field. Refer to HDMI Spec 1.0, Section 6.4.
9. 2x clocking does not support YC 4:2:2 Embedded Sync timings for 720p or 1080i, as the output clock frequency would exceed the range allowed for the SiI9135.

The SiI9135 can output video in various formats on its parallel digital output bus. Some transformation of the data received over HDMI is necessary in some modes. Digital output is used with either 4:4:4 or 4:2:2 data.

The diagrams do not include separation of the audio and InfoFrame packets from the HDMI stream, which occurs immediately after the TMDS and (optional) HDCP decoding. The HDMI link always carries explicit HSYNC and VSYNC and DE. Therefore the SAV/EAV sync encoder must be used whenever the output mode includes embedded sync.

The timing diagrams in Figure 26 through Figure 30 show only a representation of the DE, HSYNC and VSYNC timings. These timings are specific to the video resolution, as defined by EIA/CEA-861B and other specs. The number of pixels shown per DE high time is representative, to show the data formatting.

RGB and YCbCr 4:4:4 Formats with Separate Syncs

The pixel clock runs at the pixel rate and a complete definition of each pixel is output on each clock. Figure 26 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in Table 15. Figure 26 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 15. 4:4:4 Mappings

Pin Name	36-bit RGB	36-bit YCbCr	30-bit RGB	30-bit YCbCr	24-bit RGB	24-bit YCbCr
Q0	B0	Cb0	NC	NC	NC	NC
Q1	B1	Cb1	NC	NC	NC	NC
Q2	B2	Cb2	B0	Cb0	NC	NC
Q3	B3	Cb3	B1	Cb1	NC	NC
Q4	B4	Cb4	B2	Cb2	B0	Cb0
Q5	B5	Cb5	B3	Cb3	B1	Cb1
Q6	B6	Cb6	B4	Cb4	B2	Cb2
Q7	B7	Cb7	B5	Cb5	B3	Cb3
Q8	B8	Cb8	B6	Cb6	B4	Cb4
Q9	B9	Cb9	B7	Cb7	B5	Cb5
Q10	B10	Cb10	B8	Cb8	B6	Cb6
Q11	B11	Cb11	B9	Cb9	B7	Cb7
Q12	G0	Y0	NC	NC	NC	NC
Q13	G1	Y1	NC	NC	NC	NC
Q14	G2	Y2	G0	Y0	NC	NC
Q15	G3	Y3	G1	Y1	NC	NC
Q16	G4	Y4	G2	Y2	G0	Y0
Q17	G5	Y5	G3	Y3	G1	Y1
Q18	G6	Y6	G4	Y4	G2	Y2
Q19	G7	Y7	G5	Y5	G3	Y3
Q20	G8	Y8	G6	Y6	G4	Y4
Q21	G9	Y9	G7	Y7	G5	Y5
Q22	G10	Y10	G8	Y8	G6	Y6
Q23	G11	Y11	G9	Y9	G7	Y7
Q24	R0	Cr0	NC	NC	NC	NC
Q25	R1	Cr1	NC	NC	NC	NC
Q26	R2	Cr2	R0	Cr0	NC	NC
Q27	R3	Cr3	R1	Cr1	NC	NC
Q28	R4	Cr4	R2	Cr2	R0	Cr0
Q29	R5	Cr5	R3	Cr3	R1	Cr1
Q30	R6	Cr6	R4	Cr4	R2	Cr2
Q31	R7	Cr7	R5	Cr5	R3	Cr3
Q32	R8	Cr8	R6	Cr6	R4	Cr4
Q33	R9	Cr9	R7	Cr7	R5	Cr5
Q34	R10	Cr10	R8	Cr8	R6	Cr6
Q35	R11	Cr11	R9	Cr9	R7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

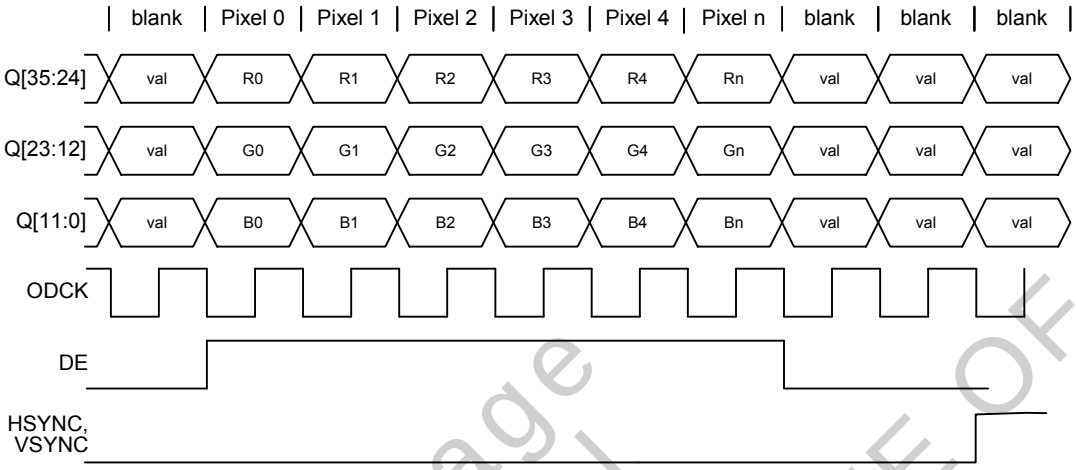


Figure 26. 4:4:4 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9135 registers, as no pixel data is carried on HDMI during blanking.

YC 4:2:2 Formats with Separate Syncs

The YC 4:2:2 formats output one pixel for every pixel clock period. A luminance (Y) value is output for every pixel, but the chrominance values (Cb and Cr) are sent over two pixels. Pixel data can be 24-bit, 20-bit or 16-bit. HSYNC and VSYNC are output explicitly on their own pins. The DE high time must contain an even number of pixel clocks. Figure 27 shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 16. YC 4:2:2 Non-Encoded-Sync Pin Mappings

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

Table 17. YC 4:2:2 (Pass Through Only) Non-Encoded-Sync Pin Mapping*

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

* This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. None of any video processing block shall be enabled when this pin mapping is used.

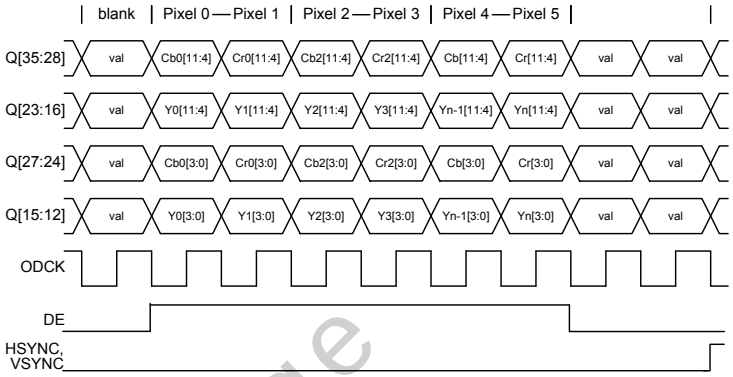


Figure 27. YC Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9135 registers, as no pixel data is carried on HDMI during blanking.

YC 4:2:2 Formats with Embedded Syncs

The YC 4:2:2 embedded sync format is identical to the previous format (YC 4:2:2), except that the syncs are embedded and not explicit. Pixel data can be 24-bit, 20-bit or 16-bit. DE is always output. Figure 28 shows the "start of active video" (SAV) preamble, the "end of active video" (EAV) suffix, and shows timings with OCLKDIV = 0 and OCKINV = 1.

Table 18. YC 4:2:2 Embedded Sync Pin Mappings

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	NC	NC
Q5	NC	NC	NC	NC	NC	NC
Q6	NC	NC	NC	NC	NC	NC
Q7	NC	NC	NC	NC	NC	NC
Q8	NC	NC	NC	NC	NC	NC
Q9	NC	NC	NC	NC	NC	NC
Q10	NC	NC	NC	NC	NC	NC
Q11	NC	NC	NC	NC	NC	NC
Q12	NC	NC	NC	NC	Y0	Y0
Q13	NC	NC	NC	NC	Y1	Y1
Q14	NC	NC	Y0	Y0	Y2	Y2
Q15	NC	NC	Y1	Y1	Y3	Y3
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	Cb0	Cr0
Q25	NC	NC	NC	NC	Cb1	Cr1
Q26	NC	NC	Cb0	Cr0	Cb2	Cr2
Q27	NC	NC	Cb1	Cr1	Cb3	Cr3
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

Table 19. YC 4:2:2 (Pass Through Only) Embeded Sync Pin Mapping*

Pin	16-bit YC		20-bit YC		24-bit YC	
Name	Pixel #0	Pixel #1	Pixel #0	Pixel #1	Pixel #0	Pixel #1
Q0	NC	NC	NC	NC	NC	NC
Q1	NC	NC	NC	NC	NC	NC
Q2	NC	NC	NC	NC	NC	NC
Q3	NC	NC	NC	NC	NC	NC
Q4	NC	NC	NC	NC	Y0	Y0
Q5	NC	NC	NC	NC	Y1	Y1
Q6	NC	NC	Y0	Y0	Y2	Y2
Q7	NC	NC	Y1	Y1	Y3	Y3
Q8	NC	NC	NC	NC	Cb0	Cr0
Q9	NC	NC	NC	NC	Cb1	Cr1
Q10	NC	NC	Cb0	Cr0	Cb2	Cr2
Q11	NC	NC	Cb1	Cr1	Cb3	Cr3
Q12	NC	NC	NC	NC	NC	NC
Q13	NC	NC	NC	NC	NC	NC
Q14	NC	NC	NC	NC	NC	NC
Q15	NC	NC	NC	NC	NC	NC
Q16	Y0	Y0	Y2	Y2	Y4	Y4
Q17	Y1	Y1	Y3	Y3	Y5	Y5
Q18	Y2	Y2	Y4	Y4	Y6	Y6
Q19	Y3	Y3	Y5	Y5	Y7	Y7
Q20	Y4	Y4	Y6	Y6	Y8	Y8
Q21	Y5	Y5	Y7	Y7	Y9	Y9
Q22	Y6	Y6	Y8	Y8	Y10	Y10
Q23	Y7	Y7	Y9	Y9	Y11	Y11
Q24	NC	NC	NC	NC	NC	NC
Q25	NC	NC	NC	NC	NC	NC
Q26	NC	NC	NC	NC	NC	NC
Q27	NC	NC	NC	NC	NC	NC
Q28	Cb0	Cr0	Cb2	Cr2	Cb4	Cr4
Q29	Cb1	Cr1	Cb3	Cr3	Cb5	Cr5
Q30	Cb2	Cr2	Cb4	Cr4	Cb6	Cr6
Q31	Cb3	Cr3	Cb5	Cr5	Cb7	Cr7
Q32	Cb4	Cr4	Cb6	Cr6	Cb8	Cr8
Q33	Cb5	Cr5	Cb7	Cr7	Cb9	Cr9
Q34	Cb6	Cr6	Cb8	Cr8	Cb10	Cr10
Q35	Cb7	Cr7	Cb9	Cr9	Cb11	Cr11
HSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded	Embedded	Embedded	Embedded

* This pin mapping is only valid when the input video format is YC 4:2:2 and the output video format is YC 4:2:2 also. None of any video processing block shall be enabled when this pin mapping is used.

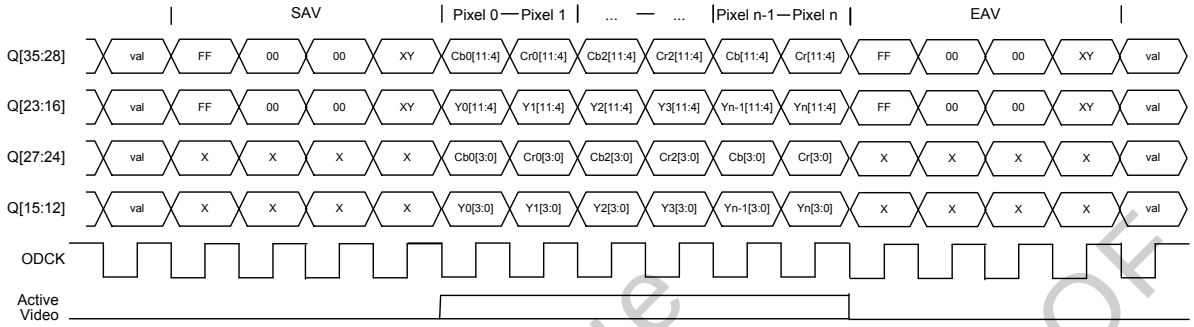


Figure 28. YC 4:2:2 Embedded Sync Timing Diagram

Note: The val data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9135 registers, as no pixel data is carried on HDMI during blanking. SAV/EAV codes appear as an 8-bit field on both Q[35:28] (per SMPTE) and Q[23:16].

YC Mux (4:2:2) Formats with Separate Syncs

The video data is multiplexed onto fewer pins than the mapping in Table 20, but complete luminance (Y) and chrominance (Cb and Cr) data is still provided for each pixel because the output pixel clock runs at twice the pixel rate. Figure 29 shows the 24-bit mode. The 16- and 20-bit mappings use fewer output pins for the pixel data. Note the explicit syncs. Figure 29 shows OCLKDIV = 0 and OCKINV = 1.

Table 20. YC Mux 4:2:2 Mappings

Pin Name	8-bit YCbCr	10-bit YCbCr	12-bit YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE

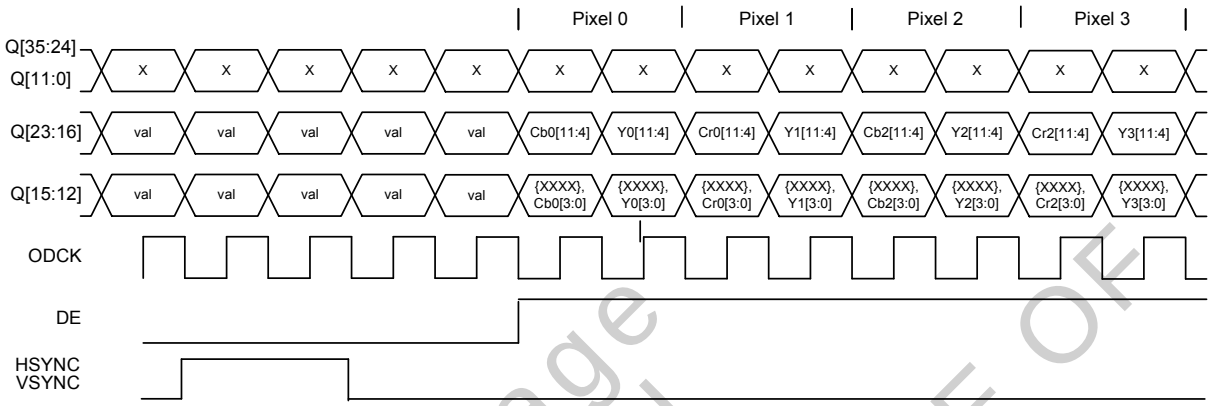


Figure 29. YC Mux 4:2:2 Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9135 registers, as no pixel data is carried on HDMI during blanking.

YC Mux 4:2:2 Formats with Embedded Syncs

This mode is similar to that on page 54, but with embedded syncs. It is similar to YC 4:2:2 with embedded syncs, but also multiplexes the luminance (Y) and chrominance (Cb and Cr) onto the same pins on alternating pixel clock cycles. Normally this mode is used only for 480i, 480p, 576i and 576p modes. Output clock rate is half the pixel clock rate on the link. SAV code is shown before rise of DE. EAV follows fall of DE. See ITU-R BT.656 Specification. 480p 54 MHz output can be achieved if the input differential clock is 54 MHz. Figure 30 shows OCLKDIV = 0 and OCKINV = 1.

Table 21. YC Mux 4:2:2 Embedded Sync Pin Mapping

Pin	8-bit	10-bit	12-bit
Name	YCbCr	YCbCr	YCbCr
Q0	NC	NC	NC
Q1	NC	NC	NC
Q2	NC	NC	NC
Q3	NC	NC	NC
Q4	NC	NC	NC
Q5	NC	NC	NC
Q6	NC	NC	NC
Q7	NC	NC	NC
Q8	NC	NC	NC
Q9	NC	NC	NC
Q10	NC	NC	NC
Q11	NC	NC	NC
Q12	NC	NC	D0
Q13	NC	NC	D1
Q14	NC	D0	D2
Q15	NC	D1	D3
Q16	D0	D2	D4
Q17	D1	D3	D5
Q18	D2	D4	D6
Q19	D3	D5	D7
Q20	D4	D6	D8
Q21	D5	D7	D9
Q22	D6	D8	D10
Q23	D7	D9	D11
Q24	NC	NC	NC
Q25	NC	NC	NC
Q26	NC	NC	NC
Q27	NC	NC	NC
Q28	NC	NC	NC
Q29	NC	NC	NC
Q30	NC	NC	NC
Q31	NC	NC	NC
Q32	NC	NC	NC
Q33	NC	NC	NC
Q34	NC	NC	NC
Q35	NC	NC	NC
HSYNC	Embedded	Embedded	Embedded
VSYNC	Embedded	Embedded	Embedded
DE	Embedded	Embedded	Embedded

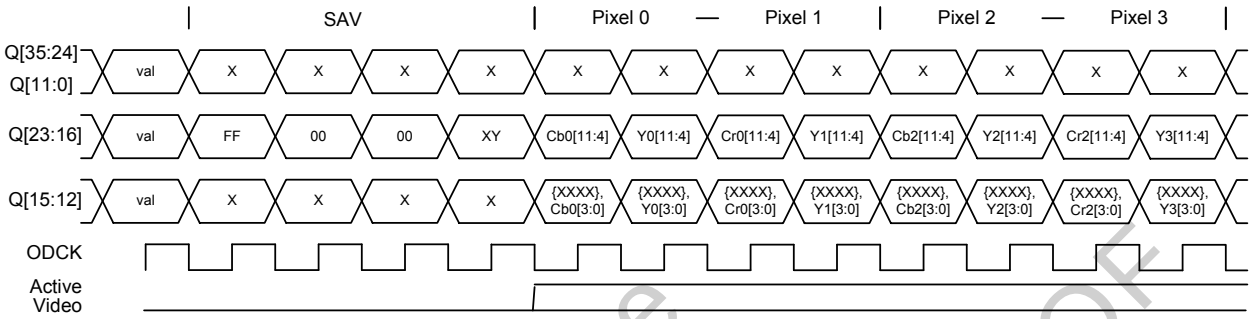


Figure 30. YC Mux 4:2:2 Embedded Sync Encoding Timing Diagram

Note: The *val* data is defined in various specifications to specific values. These values are controlled by setting the appropriate SiI9135 registers, as no pixel data is carried on HDMI during blanking. Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for details.

12/15/18-Bit RGB and YCbCr 4:4:4 Formats with Separate Syncs

The output clock runs at the pixel rate and a complete definition of each pixel is output on each clock. One clock edge drives out half the pixel data on 12/15/18 pins. The opposite clock edge drives out the remaining half of the pixel data on the same 12/15/18 pins. Figure 31 shows RGB data. The same timing format is used for YCbCr 4:4:4 as listed in the columns of Table 22. Control signals (DE, HSYNC and VSYNC) change state with respect to the first edge of ODCK.

Table 22. 12/15/18-Bit Output 4:4:4 Mappings

	24-bit				30-bit				36-bit			
Pin	**RGB**		**YCbCr**		**RGB**		**YCbCr**		**RGB**		**YCbCr**	
Name	**First Edge**	**Second Edge**	**First Edge**	**Second Edge**	**First Edge**	**Second Edge**	**First Edge**	**Second Edge**	**First Edge**	**Second Edge**	**First Edge**	**Second Edge**
Q0	NC	NC	NC	NC	NC	NC	NC	NC	B0	G6	Cb0	Y6
Q1	NC	NC	NC	NC	NC	NC	NC	NC	B1	G7	Cb1	Y7
Q2	NC	NC	NC	NC	NC	NC	NC	NC	B2	G8	Cb2	Y8
Q3	NC	NC	NC	NC	B0	G5	Cb0	Y5	B3	G9	Cb3	Y9
Q4	NC	NC	NC	NC	B1	G6	Cb1	Y6	B4	G10	Cb4	Y10
Q5	NC	NC	NC	NC	B2	G7	Cb2	Y7	B5	G11	Cb5	Y11
Q6	B0	G4	Cb0	Y4	B3	G8	Cb3	Y8	B6	R0	Cb6	Cr0
Q7	B1	G5	Cb1	Y5	B4	G9	Cb4	Y9	B7	R1	Cb7	Cr1
Q8	B2	G6	Cb2	Y6	B5	R0	Cb5	Cr0	B8	R2	Cb8	Cr2
Q9	B3	G7	Cb3	Y7	B6	R1	Cb6	Cr1	B9	R3	Cb9	Cr3
Q10	B4	R0	Cb4	Cr0	B7	R2	Cb7	Cr2	B10	R4	Cb10	Cr4
Q11	B5	R1	Cb5	Cr1	B8	R3	Cb8	Cr3	B11	R5	Cb11	Cr5
Q12	B6	R2	Cb6	Cr2	B9	R4	Cb9	Cr4	G0	R6	Y0	Cr6
Q13	B7	R3	Cb7	Cr3	G0	R5	Y0	Cr5	G1	R7	Y1	Cr7
Q14	G0	R4	Y0	Cr4	G1	R6	Y1	Cr6	G2	R8	Y2	Cr8
Q15	G1	R5	Y1	Cr5	G2	R7	Y2	Cr7	G3	R9	Y3	Cr9
Q16	G2	R6	Y2	Cr6	G3	R8	Y3	Cr8	G4	R10	Y4	Cr10
Q17	G3	R7	Y3	Cr7	G4	R9	Y4	Cr9	G5	R11	Y5	Cr11
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

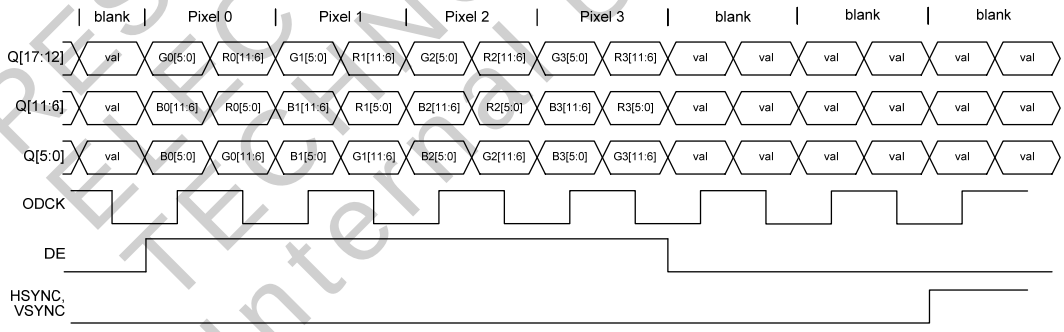


Figure 31. 18-Bit Output 4:4:4 Timing Diagram

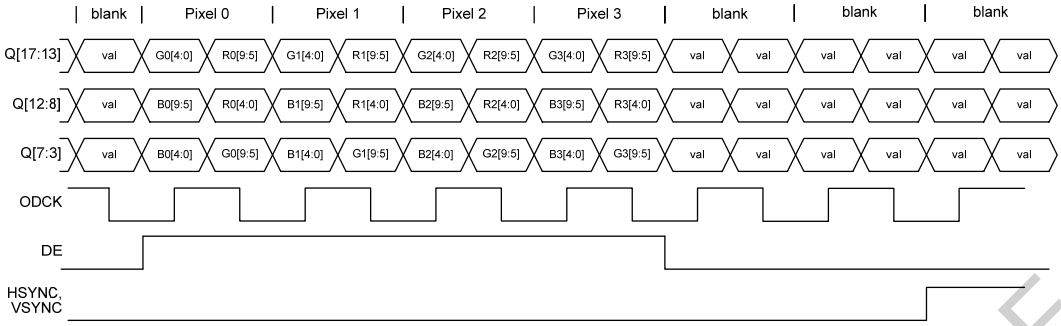


Figure 32. 15-Bit Output 4:4:4 Timing Diagram

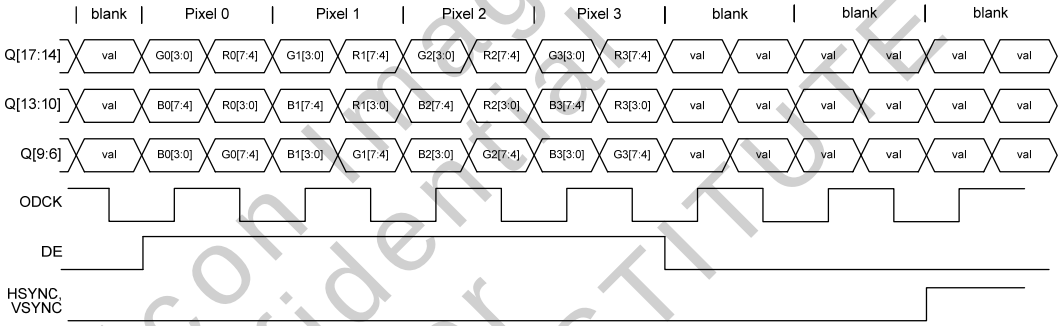


Figure 33. 12-Bit Output 4:4:4 Timing Diagram

I²C Interfaces

HDCP E-DDC / I²C Interface

The HDCP protocol requires values to be exchanged between the video Transmitter and video Receiver. These values are exchanged over the DDC channel of the DVI interface. The E-DDC channel follows the I²C serial protocol. In a SiI9135 design, the SiI9135 is the video Receiver and has a connection to the E-DDC bus with a slave address of 0x74 The I²C read operation is shown in Figure 34, and the write operation in Figure 35.

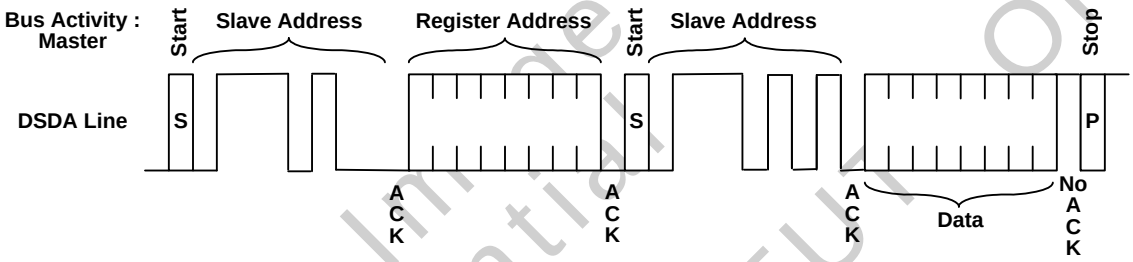


Figure 34. I²C Byte Read

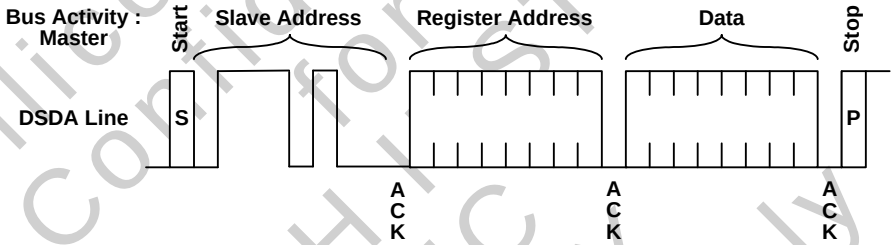


Figure 35. I²C Byte Write

Multiple bytes can be transferred in each transaction, regardless of whether a read or a write. The operations are similar to those in Figure 34 and Figure 35 except that there is more than one data phase. An ACK follow each byte except the last byte in a read operation. Byte addresses increment, with the least significant byte transferred first, and the most significant byte last. See the I²C specification for more information.

There is also a “Short Read” format, designed to improve the efficiency of Ri register reads (which must be done every two seconds while encryption is enabled). This transaction is shown in Figure 36. Note that there is no register address phase (only the slave address phase), since the register address is reset to 0x08 (Ri) after a hardware or software reset, and after the STOP condition on any preceding I²C transaction.

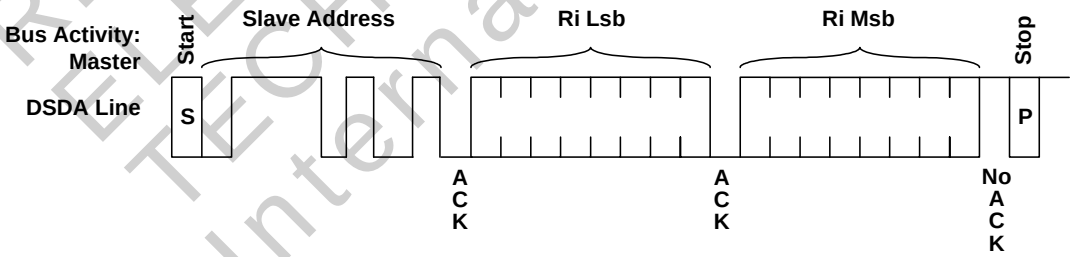


Figure 36. Short Read Sequence

Local I²C Interface

The SiI9135 has a second I²C port accessible only to the controller in the display device. It is separate from the E-DDC bus. The HDMI Receiver is a slave device that responds to two seven-bit binary I²C device addresses: 0x60 and 0x68. Two device addresses are used to accommodate the long list of registers in the SiI9135, since I²C can access only 256 registers at any one device address. This I²C interface only supports the read operation in Figure 34, and the write operation in Figure 35. It does not support the short read operation shown in Figure 36.

Note that the I²C data pin for the local I²C bus is CSDA, instead of the DSDA pin shown in these figures.

Video Requirement for I²C Access

The SiI9135 does not require an active video clock to access its registers from either the E-DDC port or the local I²C port. Read-Write registers can be written and then read back. Read-only registers that provide values for an active video or audio stream return indeterminate values if there is no video clock and no active syncs.

Use the SCDT and CKDT register bits to determine when active video is being received by the chip.

I²C Registers

The register values that are exchanged over the HDMI DDC I²C serial interface with the SiI9135 for HDCP are described in the HDCP 1.0 Specification (February 2000) in *Section 2.6 – HDCP Port*. Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for details on these and all other SiI9135 registers.

Design Recommendations

The following information is provided as recommendations that are based on the experience of Silicon Image engineers and customers. If you choose to deviate from these recommendations for a particular application, it is strongly suggested that you contact your Silicon Image technical representative for an evaluation of the change.

Power Control

The low-power standby state feature of the SiI9135 provides a design option of leaving the chip always powered, as opposed to powering it on and off. Leaving the chip powered and using the PD# register bit to put it in a lower power state can result in faster system response time, depending on the system Vcc supply ramp-up delay.

Power Pin Current Demands

The limits shown in Table 23 indicate the current demanded by each group of power pins on the SiI9135. These limits were characterized at maximum VCC, 0° C ambient temperature and for fast-fast silicon. Actual application current demands can be lower than these figures, and varies with video resolution and audio clock frequency.

Table 23. Maximum Power Domain Currents versus Video Mode

		3.3V Power Domain Currents (mA)			
Mode	**ODCK (MHz)**	**IOVCC33**	**AVCC33**	**XTALVCC**	**REGVCC**
480p	27.0	39	51	7	6
1080i	74.25	100	51	7	6
1080p	148.5	182	51	7	6
1080p@12-bit[1]	225	252	51	7	6

		1.8V Power Domain Currents (mA)		
Mode	**ODCK (MHz)**	**AVCC18**	**CVCC18**	**DVCC18**
480p	27.0	36	52	1
1080i	74.25	54	127	1
1080p	148.5	84	253	1
1080p@12-bit[1]	225	129	343	1

Notes:

1. Measured with 12-bits/pixel video data.
2. Measured with 192 kHz, 8-channel audio, except for 480p mode which used 48 kHz, 8-channel audio.
3. Measured with RGB input, vertical black-white/1-pixel stripe (Moire2) pattern, converting to YCbCr output (digital for IOVCC33).
4. Only one core can be selected at a time. The TMDSxSEL register bit turns off the unselected core, except for the termination to AVCC33.

AVCC33 current includes 40 mA for the unselected TMDS core. Only 5 mA of this current is dissipated as power in the HDMI Receiver; the remainder is dissipated in the HDMI transmitter. The AVCC33 current on the unselected core can be reduced to 5 mA by asserting the corresponding PD_TERMx# register bit.

HDMI Receiver DDC Bus Protection

The I^2C pins on the VESA DDC Specification (available at http://www.vesa.org) defines the DDC interconnect bus to be a 5V signaling path. The I^2C pins on the HDMI Receiver chip are 5V-tolerant. And these pins are true open-drain I/O. The pull-up resistors on the DDC bus should be pulled up using the 5V supply from the HDMI connector. Refer to Figure 45 on page 71.

Decoupling Capacitors

Designers should include decoupling and bypass capacitors at each power pin in the layout. These are shown schematically in Figure 40 on page 68. Place these components as closely as possible to the SiI9135 device pins and avoid routing through. Figure 37 shows the various types of power pins on the HDMI Receiver.

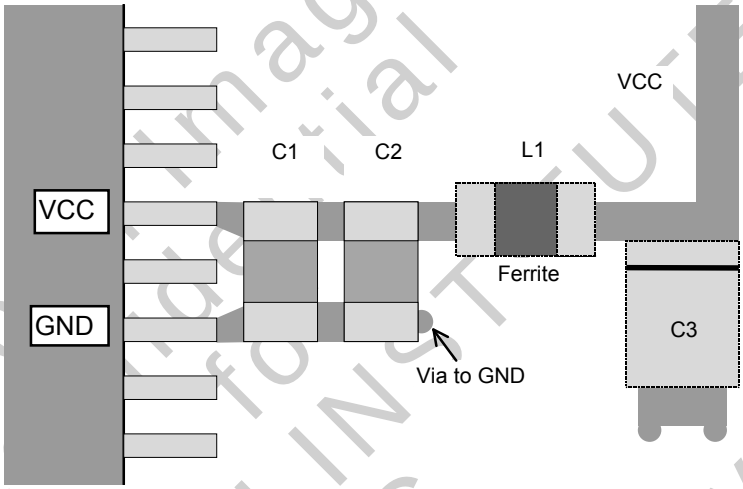


Figure 37. Decoupling and Bypass Capacitor Placement

ESD Protection

The HDMI Receiver chip is target to withstand electrostatic discharge to 2kV. In applications where higher protection levels are required, ESD limiting components can be placed on the differential lines coming into the chip. These components typically have a capacitive effect, reducing the signal quality at higher clock frequencies on the link. Use of the lowest capacitance devices is suggested; in no case should the capacitance value exceed 5pF.

Series resistors can be included on the TMDS lines (see Figure 45 on page 71) to counteract the impedance effects of ESD protection diodes. The diodes typically lower the impedance because of their capacitance. The resistors raise the impedance to stay within the HDMI specification centered around 100Ω differential.

HDMI Receiver Layout

The HDMI Receiver chip should be placed as closely as possible to the input connectors that carry the TMDS signals. For a system using industry-standard HDMI connectors (see http://www.hdmi.org), the differential lines should be routed as directly as possible from connector to HDMI Receiver. Silicon Image HDMI receivers are tolerant of skews between differential pairs, so spiral skew compensation for path length differences is not required. Each differential pair should be routed together, minimizing the number of vias through which the signal lines are routed. The distance separating the two traces of the differential pair should be kept to a minimum.
In order to achieve the optimal input TMDS signal quality, please follow the layout guidelines below:

1. Layout all differential pairs (+/-) with controlled impedance of 100 ohm differential.
2. Cut-out all copper planes (ground and power) that are less than 45 mil distance underneath the TMDS traces near the HDMI receiver with dimensions as shown below.

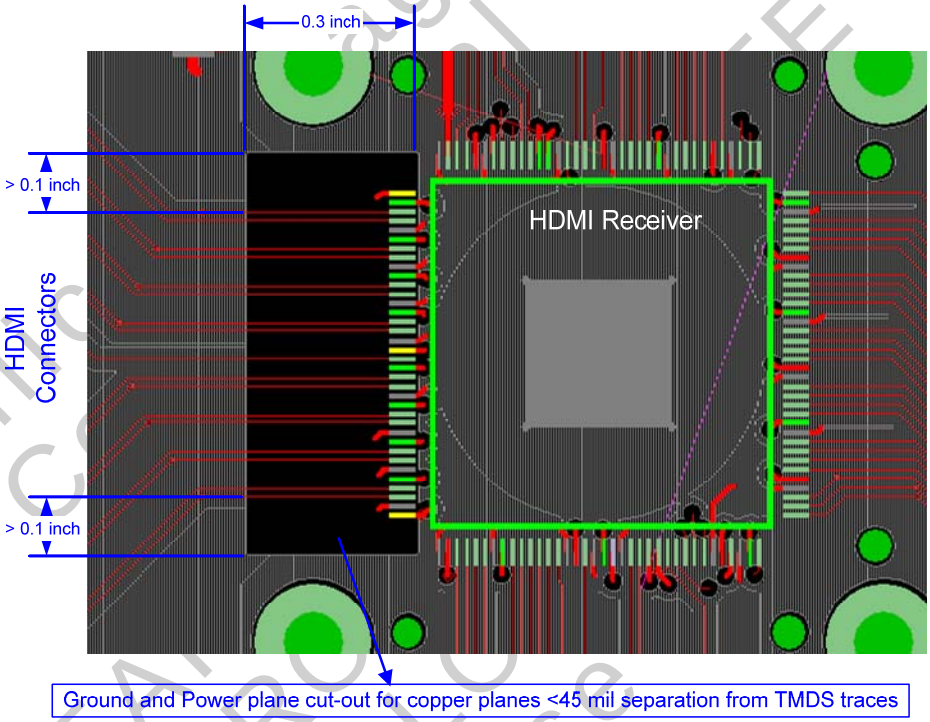


Figure 38. Cut-out Reference Plane Dimensions

3. If ESD suppression devices or common mode chokes are used, place them near the HDMI connector, away fro the HDMI Receiver IC. Do not place them over the ground and power plane cutout near the HDMI receiver.

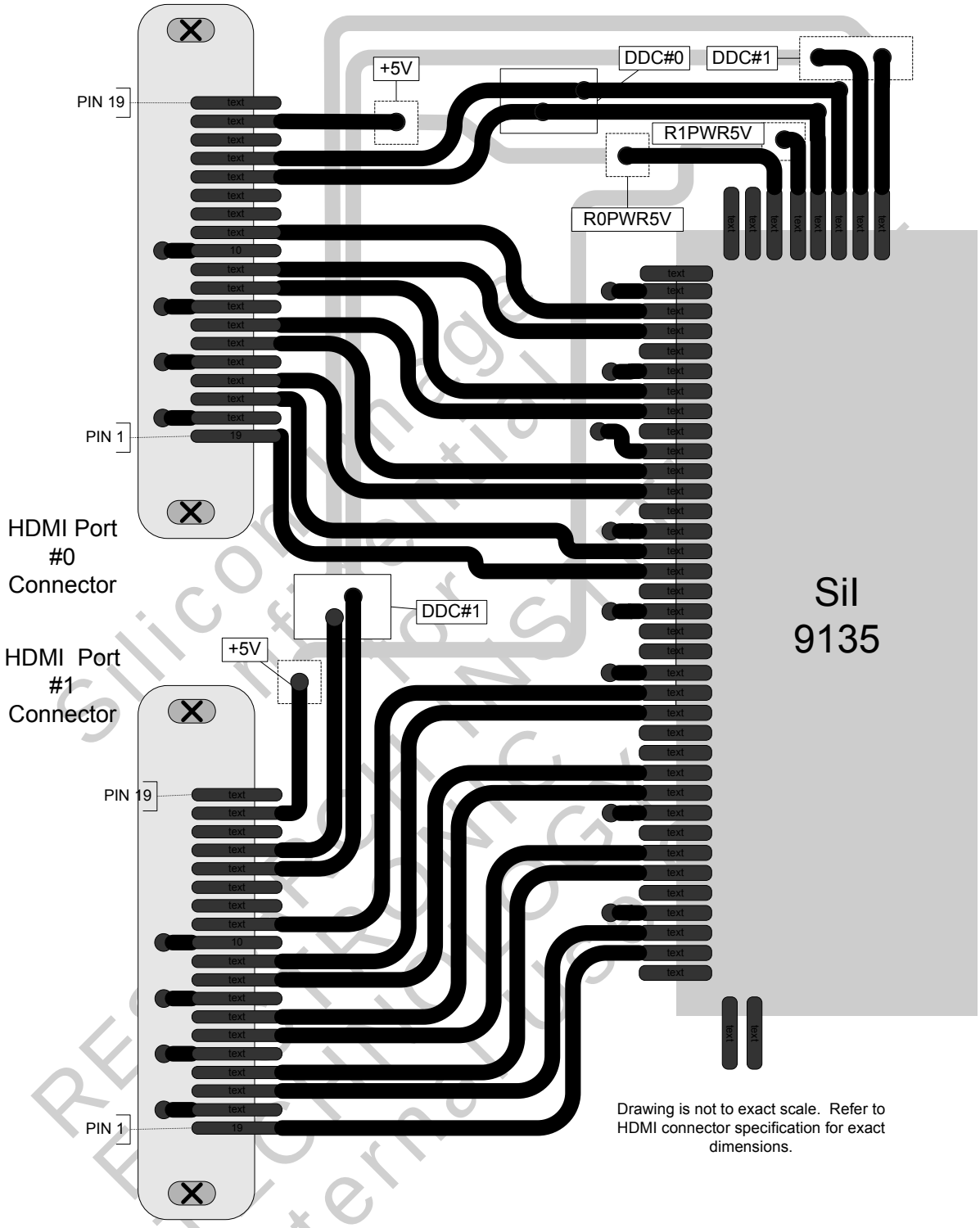


Figure 39. HDMI to Receiver Routing – Top View

Note the sixteen TMDS traces connected directly from the HDMI connectors (left) to the pins on the SiI9135 (right). Trace impedance should be 100 ohms differential in each pair, and 50 ohm single-ended if possible. Trace width and pitch depends on the PCB construction. Not all connections are shown — the drawing demonstrates routing of TMDS lines without crossovers, vias, or ESD protection. See also Figure 45.

EMI Considerations

Electromagnetic interference is a function of board layout, shielding, HDMI Receiver component operating voltage, frequency of operation, etc. When attempting to control emissions, it is important not to place any passive components on the differential signal lines (aside from any essential ESD protection as described earlier). The differential signaling used in HDMI is inherently low in EMI as long as the routing recommendations noted in the Receiver Layout section are followed.

The PCB ground plane should extend unbroken under as much of the HDMI Receiver chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

XTALIN Clock Required in All Designs

Description

The SiI9135 uses the clock at the XTALIN/XTALOUT pin pair to control the internal audio pipeline. This clock is also used to control the interrupt processing and the internal reading of HDCP keys.

The XTALIN/XTALOUT pin pair must be driven with a clock in all applications, even when the design does not support audio processing. The clock frequency must be within the range of 26–28.5 MHz.

Recommendation

For designs that do not support audio, the XTALIN pin can be connected to an ordinary 27 MHz LVTTL clock source, which is commonly available on HDMI sink designs. There is no requirement that this clock source be low jitter. The XTALOUT pin can be left unconnected when XTALIN is driven with a LVTTL clock.

Typical Circuit

Representative circuits for application of the SiI9135 HDMI Receiver chip are shown in Figure 40 through Figure 44. For a detailed review of your intended circuit implementation, contact your Silicon Image representative.

Power Supply Decoupling

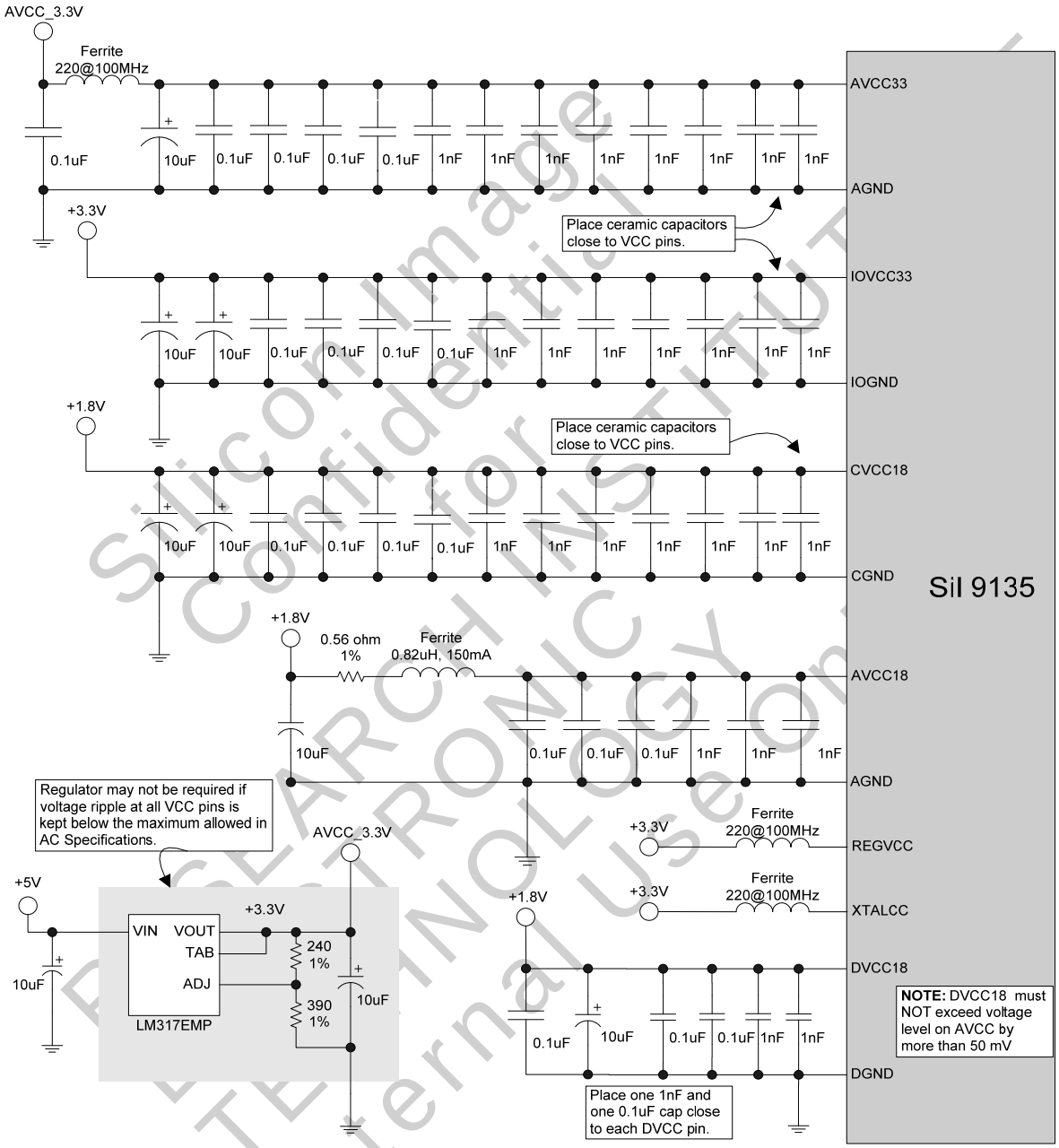


Figure 40. Power Supply Decoupling and PLL Filtering Schematic

The ferrite on AVCC18 attenuates noise at 10's of kHz and above. A parasitic resistor is helpful to minimize the peaking. An example device (surface mount, 0805 package) is part number MLF2012DR82 from TDK. A data sheet is available at http://www.tdk.co.jp/tefe02/e511_MLF2012.pdf

HDMI Port TMDS Connections

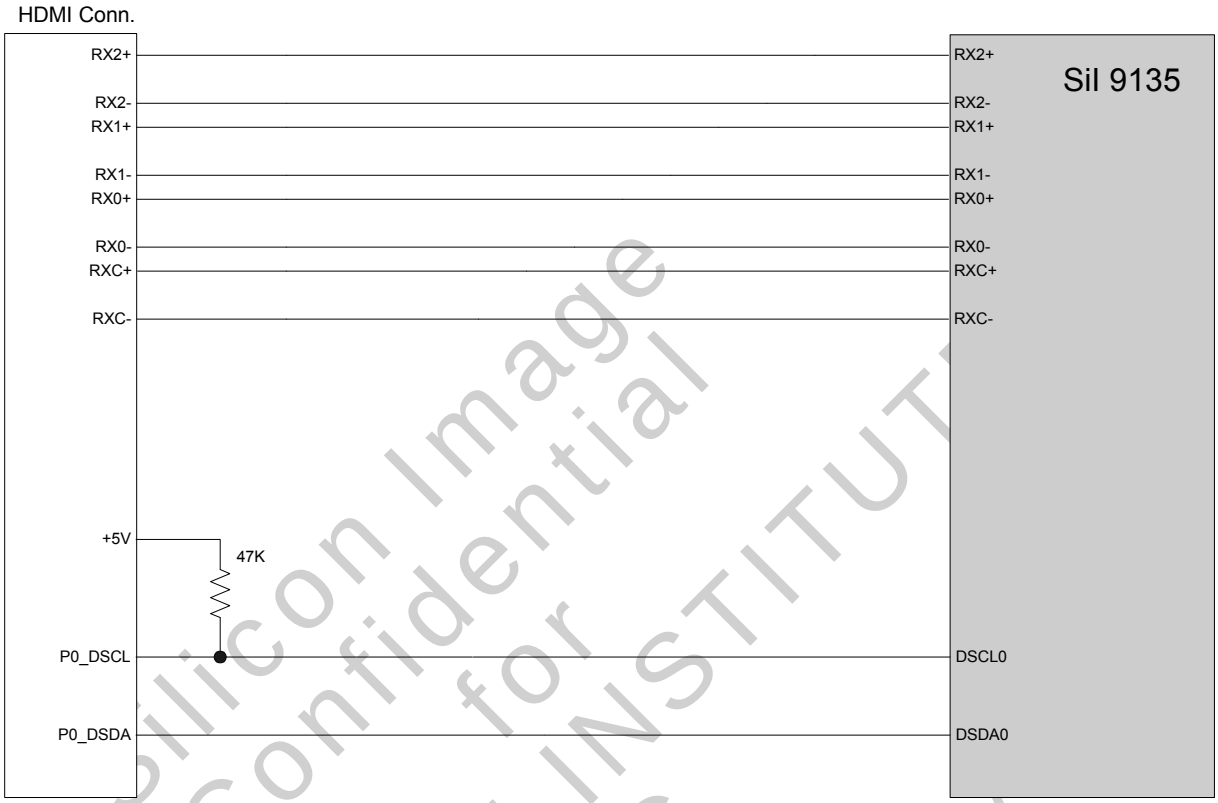


Figure 41. HDMI Port Connections Schematic

Notes:

1. Repeat the schematic for each HDMI input port on the SiI9135.

Digital Video Output Connections

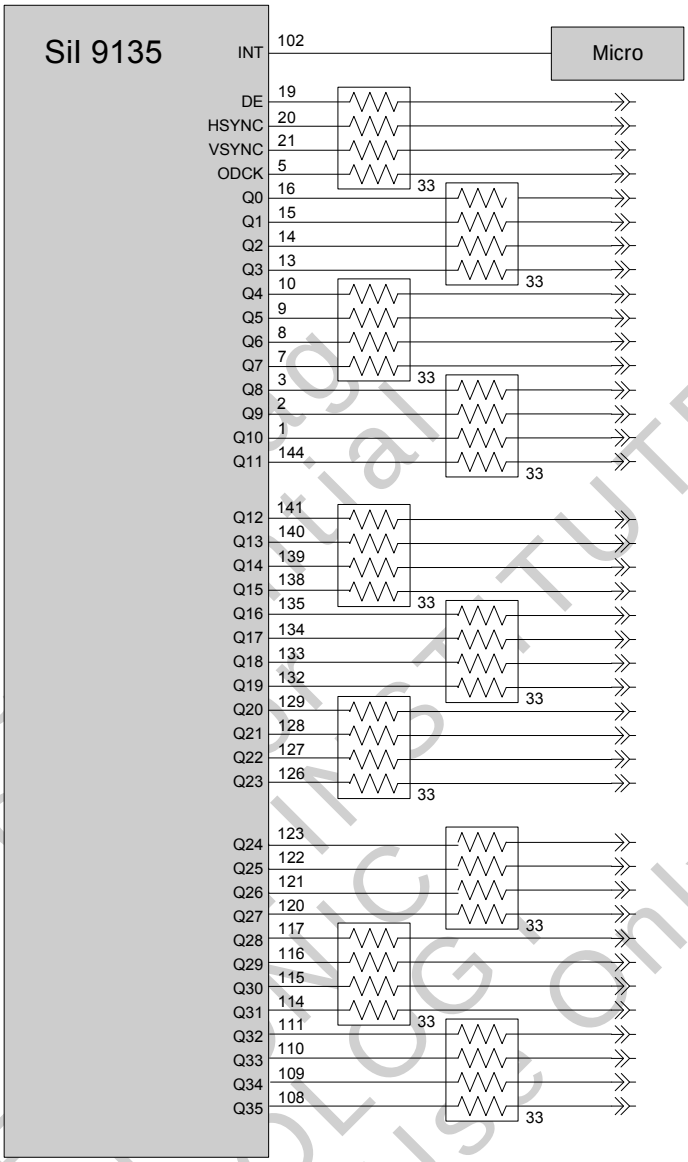


Figure 42. Digital Display Schematic

The 3.3V to the level-shifters and pull-up resistors should be powered-down whenever the 3.3V is powered-down on the HDMI Receiver itself.

The HDMI Receiver's INT output can be connected as an interrupt to the microcontroller, or the microcontroller can poll register 0x70 (INTR_STATE) to determine if any of the enabled interrupts have occurred. Refer to the SiI 9135 Programmers Reference Guide (SiI-PR-0042) for details. The HDMI Receiver's VSYNC output can be connected to the micro if it is necessary to monitor the vertical refresh rate of the incoming video.

Digital Audio Output Connections

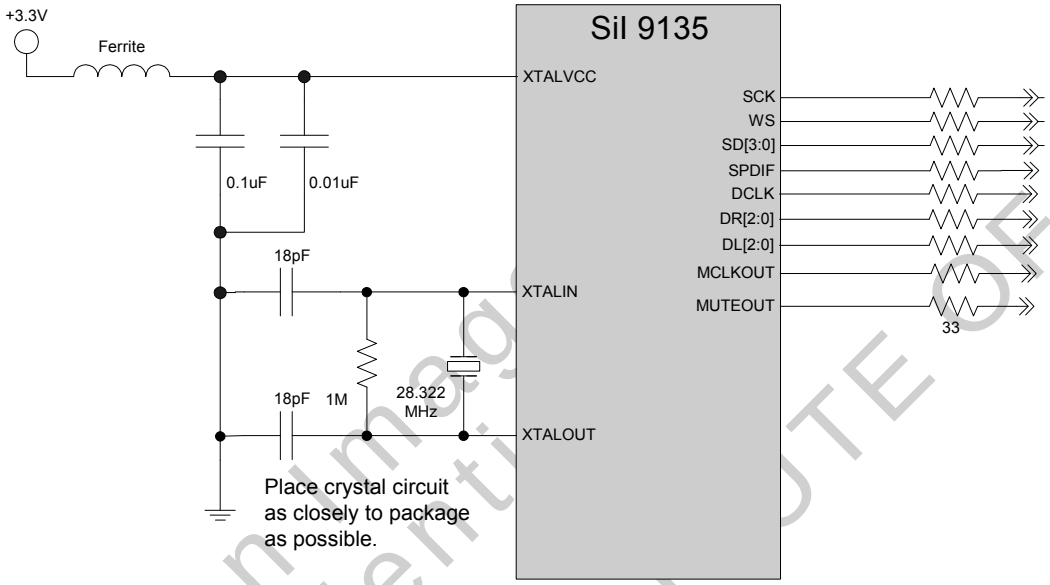


Figure 43. Audio Output Schematic

Control Signal Connections

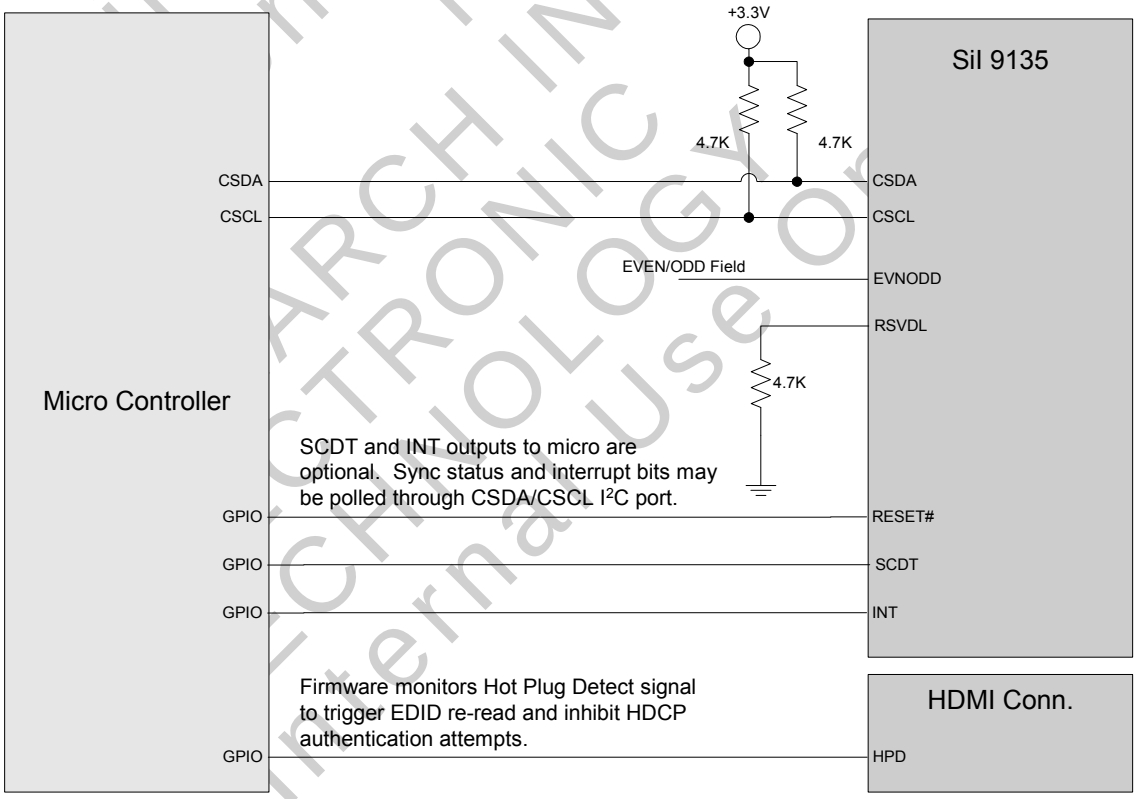


Figure 44. Controller Connections Schematic

Layout

Figure 45 shows an example of routing TMDS lines between the SiI9135 and the HDMI connector.

TMDS Input Port Connections

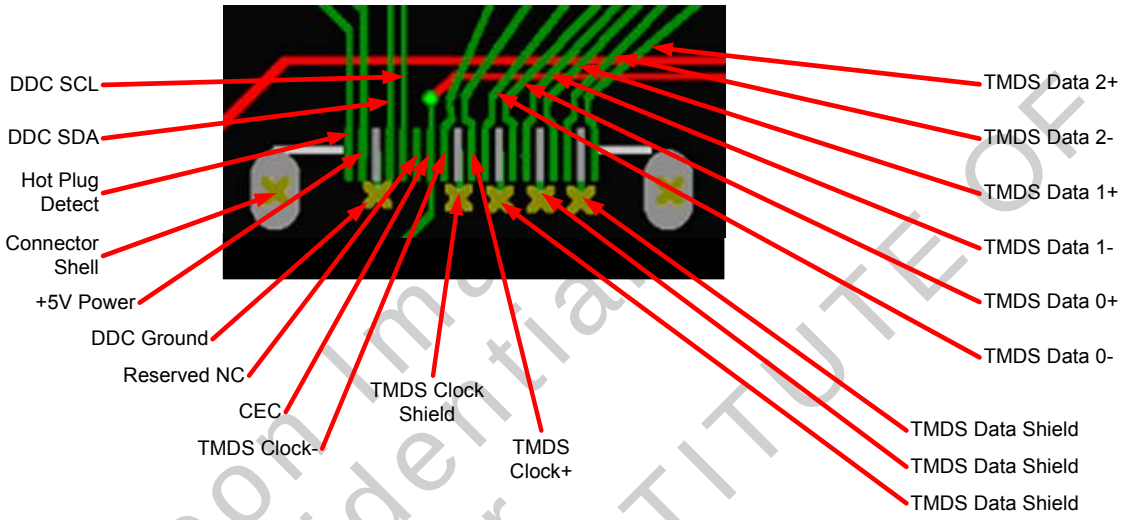
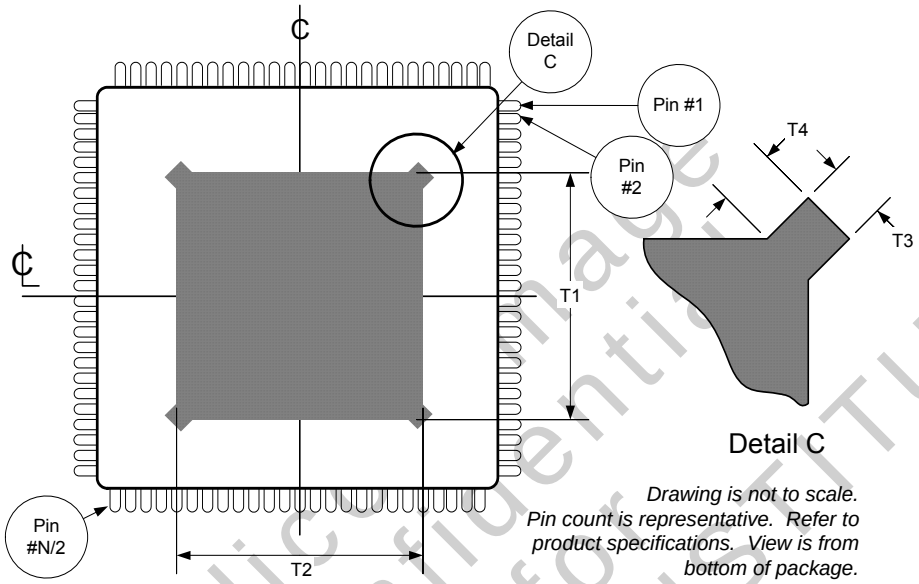


Figure 45. TMDS Input Signal Assignments

Packaging

ePad Enhancement

The SiI9135 is packaged in a TQFP package with ePad. The ePad dimensions are shown in Figure 46.



Drawing is not to scale.
Pin count is representative. Refer to product specifications. View is from bottom of package.

Silicon Image recommends that the ePad be soldered to the PCB and electrically grounded on the PCB. The ePad must not be electrically connected to any other voltage level except ground (GND).

ePad Dimensions

		typ	max
T1	ePad Height		5.2
T2	ePad Width		5.2
ΔT	ePad tolerance		±.05
T3	ePad Tab Width		0.254
T4	ePad Tab Height		0.2

All dimensions are in millimeters.

EPad is centered on the package center lines with the tolerance shown.

A clearance of at least 0.25mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid any electrical shorts. Note also the 'ear' protrusions in the corners of the ePad.

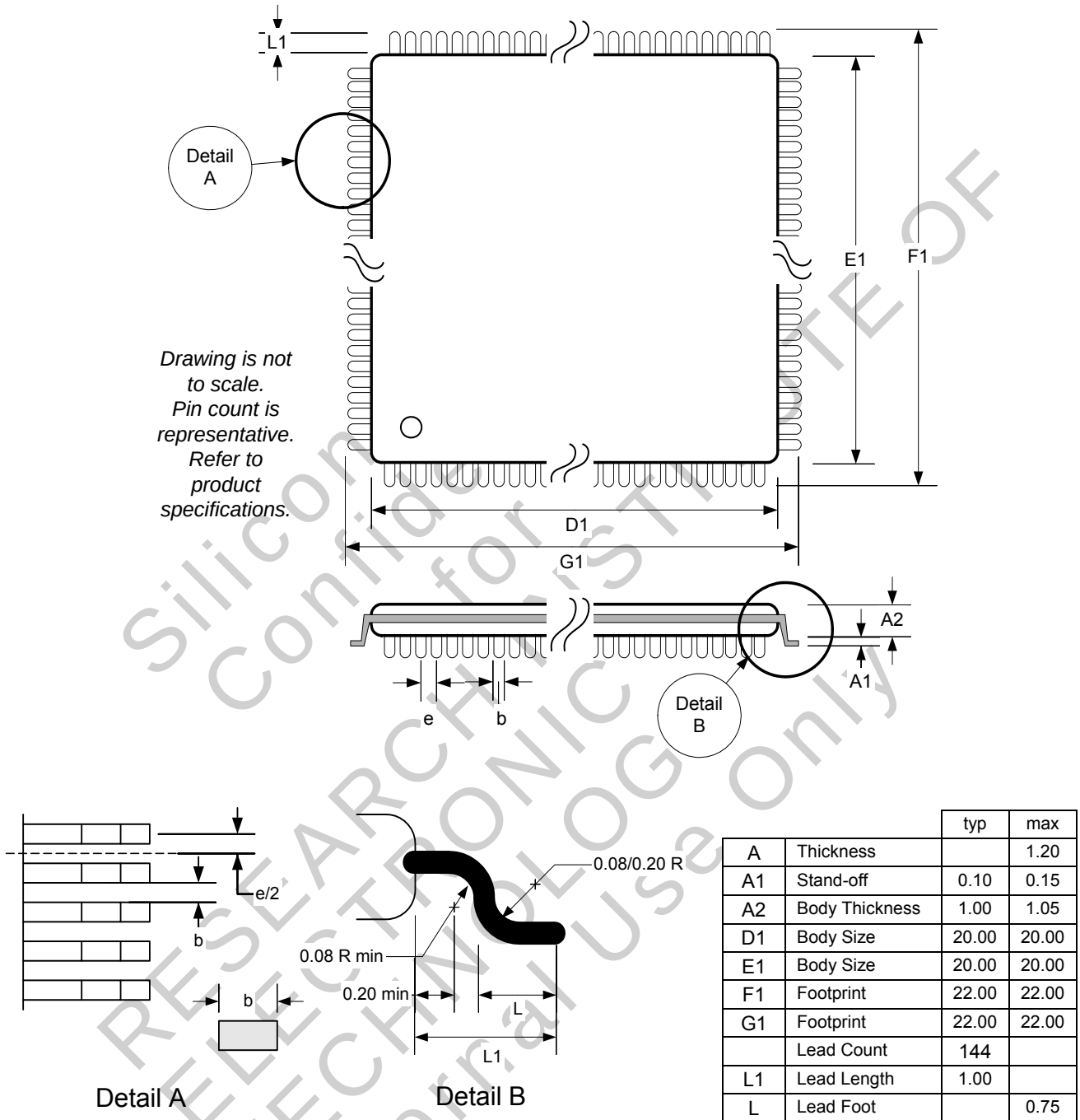
Tabs may have smaller dimensions than the maximums shown above, and may not appear at all, since minimum width and height are 0.0mm.

Figure 46. ePad Diagram

PCB Layout Guidelines

Please refer to Silicon Image document SiI-AN-0129 (PCB Layout Guidelines: Designing with Exposed Pads) for basic PCB design guidelines when designing with thermally enhanced packages using the exposed pad. This application note is intended for use by PCB layout designers.

144-pin TQFP Package Dimensions



JEDEC Package Code MS-026-AFB

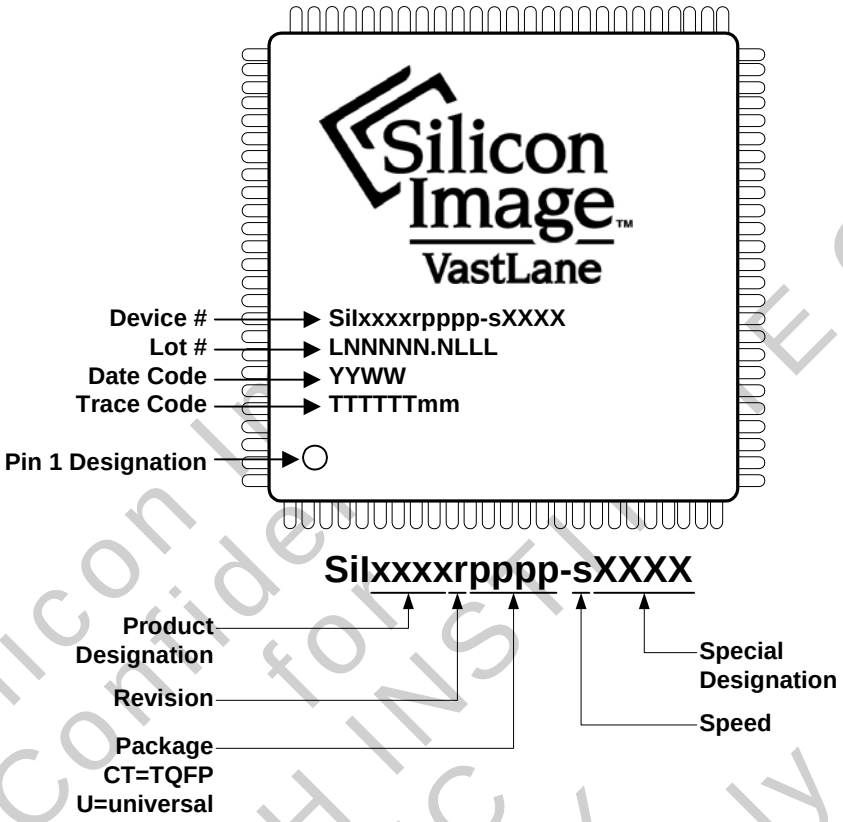
		typ	max
A	Thickness		1.20
A1	Stand-off	0.10	0.15
A2	Body Thickness	1.00	1.05
D1	Body Size	20.00	20.00
E1	Body Size	20.00	20.00
F1	Footprint	22.00	22.00
G1	Footprint	22.00	22.00
	Lead Count	144	
L1	Lead Length	1.00	
L	Lead Foot		0.75
b	Lead Width		0.27
c	Lead Thickness		0.20
e	Lead Pitch	0.50	

Dimensions in millimeters.
Overall thickness A=A1+A2.

Figure 47. Package Diagram

Marking Specification

Drawing is not to scale and pin count shown is representative. Refer to specifics in Figure 47 on page 73.



The universal package may be used in Pb-free and ordinary process lines.

Figure 48. Marking Diagram

Ordering Information

Production Part Numbers:

TMDS Input Clock Range	Part Number
25 – 225 MHz	SiI9135CTU

References

Standards Documents

Table 24 lists the abbreviations used in this document. Contact the responsible standards groups listed below for more information on these specifications.

Table 24. Referenced Documents

HDMI	*High Definition Multimedia Interface*, Revision 1.2, HDMI Consortium
HCTS	*HDMI Compliance Test Specification,* Revision 1.1, HDMI Consortium, June 2004.
HDCP	*High-bandwidth Digital Content Protection*, Revision 1.1, Digital-CP, LLP; February 2000.
DVI	*Digital Visual Interface*, Revision 1.0, Digital Display Working Group; April 1999.
E-EDID	*Enhanced Extended Display Identification Data Standard*, Release A Revision 1, VESA; Feb. 2000.
CEA861	*A DTV Profile for Uncompressed High Speed Digital Interfaces*, EIA/CEA; January 2001.
CEA861B	*A DTV Profile For Uncomp. High Speed Digital Interfaces*, Draft 020328, EIA/CEA; March 2002.
EDDC	*Enhanced Display Data Channel Standard*, Version 1, VESA; September 1999.

These documents are available from the following standards groups:

ANSI/EIA/CEA Standards:

http://global.ihs.com, or by e-mail to global@ihs.com, or telephone at 800-854-7179.

VESA Standards:

http://www.vesa.org, or by telephone at 408-957-9270.

DVI Standard:

http://www.ddwg.org or by e-mail to ddwg.if@intel.com .

HDCP Standard:

http://www.digital-cp.com or by e-mail to info@digital-cp.com .

HDMI Standard:

http://www.hdmi.org or by e-mail to admin@hdmi.org .

Silicon Image Documents

The following are available from your Silicon Image sales representative.

SiI-AN-0118	*SiI 9021/9031 HDMI Receiver Software Application Note*
SiI-PR-0042	*SiI 9125/9135 HDMI Receiver Programmer's Reference*
SiI-AN-0129	*PCB Layout Guidelines: Designing with Exposed Pads*

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