Features

- LIN 2.x/ISO 17987-4:2016 (12V)/SAE J2602 compliant
- Compatible with K line
- Built-in over-temperature protection function (thermal shutdown
- Built-in 30KΩ bus pull-up slave resistor
- Bus current limiting protection function
- Battery power failure detection function
- Very low power consumption sleep mode and standby mode
- Support remote wake-up
- Baud rate up to 20 kBd
- High ElectroMagnetic Immunity (EMI)
- Available in SOP8 and HVSON8 packages

Outline

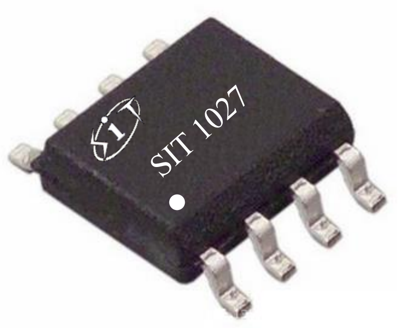


Fig 1. Provide green and environmentally friendly lead-free package

Description

SIT1027 is a local interconnect network (LIN) physical layer transceiver that complies with LIN2.0, LIN2.1, LIN2.2, LIN2.2A, ISO 17987-4:2016 (12V) and SAE J2602 standards. It is mainly suitable for in-vehicle networks with a transmission rate of 1kbps to 20kbps. SIT1027 controls the state of the LIN bus through the TXD pin, and can convert the data stream sent by the protocol controller into a bus signal with the best slew rate and waveform shaping to minimize electromagnetic radiation emission (EME). The LIN bus output pin has an internal pull-up resistor. Only when used as a master node, the LIN bus port needs to be pulled up to V_{BAT} through an external resistor in series with a diode. SIT1027 receives the data stream on the bus through the LIN pin, and transmits the data to the external microcontroller through the receiver's output pin RXD.

SIT1027 can operate in the range of 5.5V~27V and supports 12V applications. SIT1027 has an extremely low quiescent current consumption in sleep mode and standby mode. It can quickly minimize power consumption in the event of a failure. The device can be placed in normal mode via a signal on the pin SLP_N.

Pin Configuration

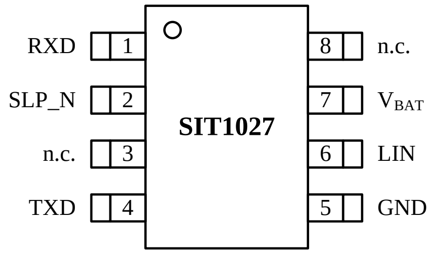


Fig 2. SIT1027 pin configuration diagrams

Pin description

Table 1. Pin description

Pin	Symbol	Description
1	RXD	receive data output (open-drain); active LOW after a wake-up event
2	SLP_N	sleep control input (active LOW); controls inhibit output; resets wake-up source flag on TXD and wake-up request on RXD
3	n.c.	No contact
4	TXD	transmit data input
5	GND	ground
6	LIN	LIN bus line input/output
7	V_{BAT}	battery supply voltage
8	n.c.	No contact

NOTE: In the DFN3*3-8/HVSON8 package, the pad on the back is connected to the GND pin of the chip. In order to obtain better heat dissipation performance, the pad on the back can be connected to a suitable "ground" on the PCB board.

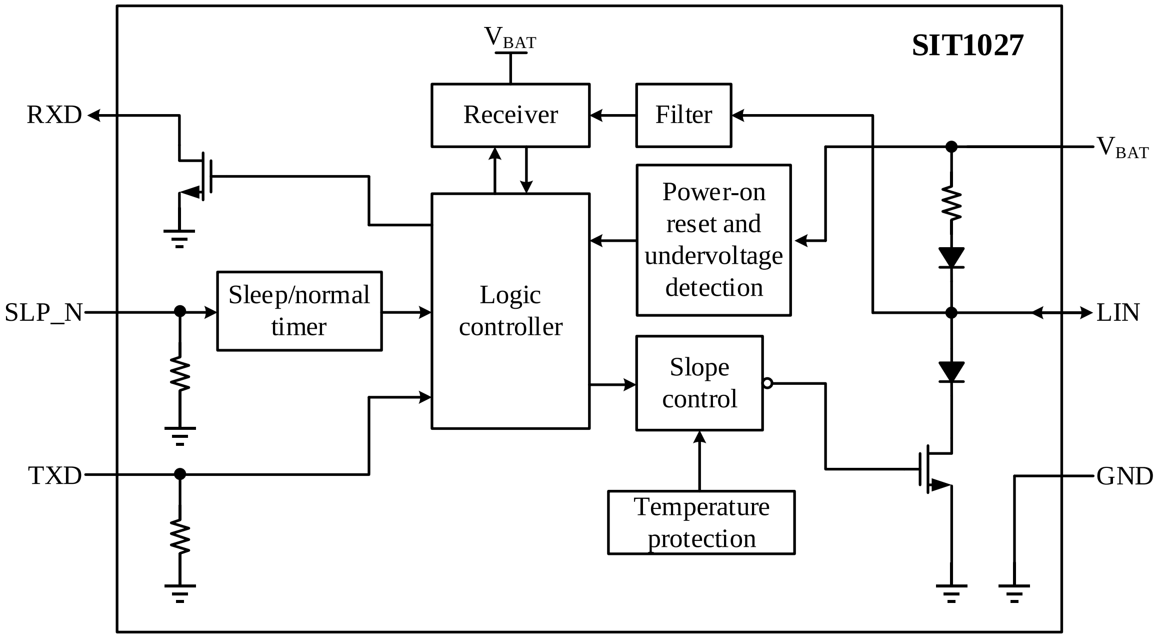


Fig 3. Block diagram

Feature Description

1 Overview

The SIT1027 is an interface device used between the LIN protocol controller and the physical bus. It can be used in trucks, buses, cars and industrial control with a data rate up to 20kBd. The SIT1027 receives the data stream sent by protocol controller at the pin TXD, and converts it into a bus signal with appropriate slew rate and waveform shaping. The input data on LIN bus is output to external microcontroller by pin RXD. This device is compliant with LIN2.0/LIN2.1/LIN2.2/LIN2.2A/ISO 17987-4:2016 (12V) and SAE J2602 standards.

2 Short-circuit protection

Pin TXD provides an internal pull-down to GND to apply a predefined level on TXD when it is not enabled. The pin SLP_N also provides an internal pull-down to force the transceiver to enter sleep mode when SLP_N is not enabled.

Pin RXD will be left floating and limit the output current of transmitter to prevent a short-circuit between LIN and VBAT or GND if the supply on pin VBAT is turned off. There is no reverse current at the bus terminal, and the connection between LIN supply can be shut off without affecting the bus.

3 Thermal Shutdown

In normal mode, the over-temperature protection circuit will disable the output driver when the junction temperature of SIT1027 exceeds the shutdown junction temperature Tj(sd). the over-temperature protection circuit will disable the output driver; when the junction temperature is lower than the hysteresis temperature, the driver is enabled again.

4 Undervoltage detection on V_{BAT}

If V_{BAT} is lower than $V_{th(VBATL)L}$ during use, the protection circuit will disable the output driver; when V_{BAT}> $V_{th(VBATL)H}$, the driver will be enabled again.

5 Operating modes

As shown in Fig 4, the SIT1027 supports four functional modes for normal operation (Normal mode), power-up (Power-on mode), standby operation (Standb mode) and very-low-power operation (Sleep mode). The operating states in each mode are shown in Table 2.

Sleep mode: This mode is the most power saving mode of the SIT1027. It can be woken up remotely via pin LIN, or activated directly via pin SLP_N. In order to prevent SIT1027 from waking up due to accidental wake-up events caused by automotive transients or EMI, filters are designed at the receiver's input (LIN pin) and SLP_N pin. The necessary condition for SIT1027 to be awakened in sleep mode is: the time to wake it up remotely through the LIN pin must be greater than $t_{wake(dom)LIN}$ (the wake-up time of LIN); the time to wake up directly through the SLP_N pin must be greater than $t_{gotonorm}$.
In normal mode, when SLP_N pin has a falling edge and SLP_N remains low for longer than $t_{gotosleep}$, SIT1027 enters sleep mode.

Standby mode: SIT1027 has very low static power consumption in this mode. When SIT1027 is in sleep mode, if a remote wake-up event is detected, the device will automatically enter standby mode immediately, and the low level on the RXD pin will indicate that the wake-up process is used to send an interrupt flag to the MCU.
Setting pin SLP_N high during Standby mode results in the following events:

(1) A change into Normal mode if the high level on pin SLP_N has been maintained for a certain time period ($t_{gotonorm}$).

(2) An immediate reset of the wake-up request signal on pin RXD.

Normal mode: Only in Normal mode the receiver and transmitter are active and the SIT1027 is able to transmit and receive data via the LIN bus. The high level of bus represents recessive and low level represents dominant. The receiver detects the data stream on the LIN bus and outputs it to the microcontroller via pin RXD. Normal mode is entered as a high level on pin SLP_N and maintained for a time of at least $t_{gotonorm}$ while the SIT1027 is in Sleep, Power-up or Standby mode. The Sleep mode is entered by setting pin SLP_N low for longer than $t_{gotosleep}$.

Power-on mode: If the voltage on V_{BAT} is less than the low-level reset threshold $V_{th(VBATL)L}$ when powering on, the SIT1027 is in power-on reset mode and all input and output functions are disabled; when the voltage on V_{BAT} is greater than the high-level reset threshold $V_{th(VBAT)\,H}$, SIT1027 enters sleep mode.

6 Wake Up Events

In sleep mode, the device can be waken up by the following two ways:

(1) Remote wake-up via pin LIN;

(2) Wake up directly via mode transition. If SLP_N is held HIGH for $t_{gotonorm}$, the device will switch from sleep mode to normal mode.

7 Remote Wake Up Events

LIN pin remote wake-up: When the LIN pin is pulled down to a low level through a falling edge, a rising edge appears at the next moment, and the low-level hold time between the rising edge and the falling edge at the previous moment is greater than $t_{wake\,(dom)\,LIN}$, The process is regarded as effective remote wake-up (as shown in Figure 5).

After the remote wake-up, the wake-up request event interrupts the microcontroller with the low level of the RXD pin as the indicator signal.

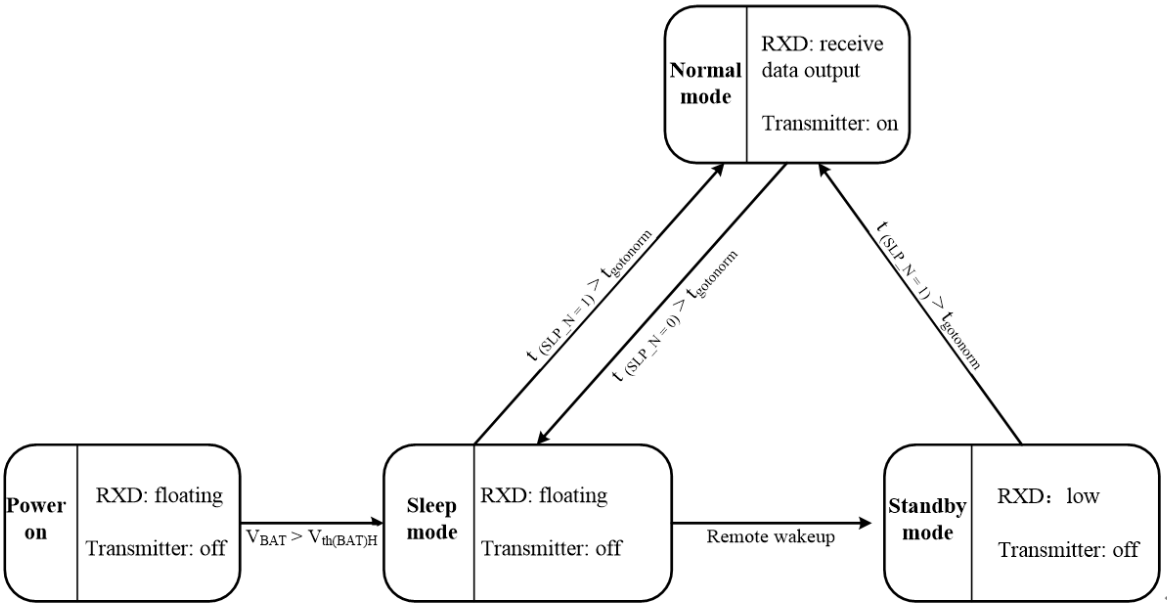


Fig 4. State diagram

Table 2. Working status of SIT1027 in each mode

Mode	SLP_N	RXD	Transmitter	Remarks
Sleep	low	floating	off	no wake-up request detected
Standby	low	low	off	wake-up requestdetected
Normal	high	recessive: high dominant: low	on	Enable bus signal shaping
Power-on	low	floating	off	Disable all input and output functions

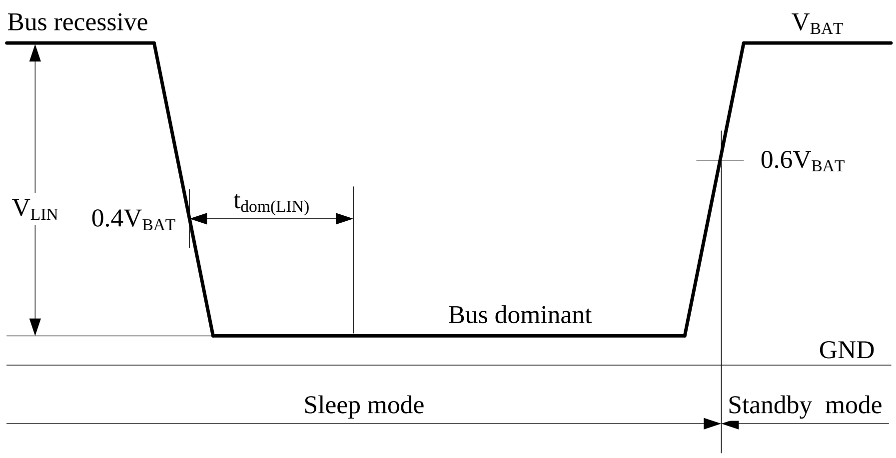


Fig 5. Remote wake-up behavior

Limiting values

Parameter	Symbol	Conditions	Range	Unit
battery supply voltage	V_{BAT}	with respect to GND	-0.3 ~ +42	V
voltage on pin TXD	V_{TXD}	I_{SLP_N} no limitation	-0.3 ~ +6	V
		$I_{SLP\_N} < 500\mu A$	-0.3 ~ +7	
voltage on pin RXD	V_{RXD}	I_{SLP_N} no limitation	-0.3 ~ +6	V
		$I_{SLP\_N} < 500\mu A$	-0.3 ~ +7	
voltage on pin SLP_N	V_{SLP_N}	I_{SLP_N} no limitation	-0.3 ~ +6	V
		$I_{SLP\_N} < 500\mu A$	-0.3 ~ +7	
voltage on pin LIN	V_{LIN}	with respect to GND	-42 ~ +42	V
virtual junction temperature	T_{vj}		-40 ~ 150	°C
storage temperature	T_{stg}		-55 ~ 150	°C

The maximum limit parameters means that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal opration of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

Static characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply						
battery supply current	I_{BAT}	Sleep mode bus recessive (V_{LIN}=V_{BAT}; V_{SLP_N}=0V)	1	4	10	µA
		Sleep mode bus dominant (V_{LIN}=V_{BAT}; V_{SLP_N}=0V)	100	400	1000	µA
		Standby mode; bus recessive (V_{LIN}=V_{BAT}; V_{SLP_N}=0V)	1	4	10	µA
		Standby mode; bus dominant (V_{BAT}=12V; V_{LIN}=0V; V_{SLP_N}=0V)	100	400	1000	µA
		Normal mode; bus recessive (V_{LIN}=V_{BAT}; V_{TXD}=5V; V_{SLP_N}=5V)	100	130	300	µA
		Normal mode; bus dominant (V_{BAT}=12V; V_{TXD}=0V; V_{SLP_N}=5V)	0.5	1.1	2	mA
Power-on reset						
low-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})L$		3.9	4.4	4.7	V
high-level V_{BAT} reset threshold voltage	$V_{th}(V_{BATL})H$		4.2	4.7	5.1	V
V_{BAT} reset hysteresis voltage	$V_{hys}(V_{BATL})$		0.05	0.3	1	V
Pin TXD						

high-level input voltage	V_{IH}		2		7	V
low-level input voltage	V_{IL}		-0.3		+0.8	V
hysteresis voltage	V_{hys}		50	200	400	mV
pull-down resistance on pin TXD	$R_{PD(TXD)}$	V_{TXD}=5V	50	125	400	kΩ
Pin SLP_N						
high-level input voltage	V_{IH}		2		7	V
low-level input voltage	V_{IL}		-0.3		0.8	V
hysteresis voltage	V_{hys}		50	200	400	mV
pull-down resistance on pin SLP_N	$R_{PD(SLP\_N)}$	V_{SLP_N}=5V	100	250	650	kΩ
Pin RXD						
low-level output current	I_{OL}	Normal mode; V_{RXD}=0.4V; V_{LIN}=0V	2	-	-	mA
high-level leakage current	I_{LH}	Normal mode; V_{RXD}=5V; V_{LIN}=V_{BAT}	-5	-	5	µA
Pin LIN						
current limitation for driver dominant state	I_{BUS_LIM}	V_{TXD}=0V; V_{LIN}=V_{BAT}=18V	40	-	100	mA
receiver recessive input leakage current	$I_{BUS\_PAS\_rec}$	V_{TXD}=5V; V_{LIN}=18V; V_{BAT}=5.5V	-	-	10	µA
receiver dominant input leakage current including pull-up resistor	$I_{BUS\_PAS\_dom}$	正常模式; V_{TXD}=5V; V_{LIN}=0V; V_{BAT}=12V	-600	-	-	µA
loss-of-ground bus current	$I_{L(log)}$	V_{BAT}=18V; V_{LIN}=0V	-1000	-	10	µA
loss-of-battery bus current	$I_{L(lob)}$	V_{BAT}=0V; V_{LIN}=18V	-	-	10	µA
receiver dominant input voltage	$V_{th(dom)RX}$				0.4V_{BAT}	V
receiver recessive input voltage	$V_{th(rec)RX}$		0.6V_{BAT}			V

receiver center voltage	$V_{th(RX)cntr}$	$V_{th(RX)\ cntr}$= ($V_{th(rec)RX}$+ $V_{th(dom)RX}$)/2	0.475V_{BAT}	0.5 V_{BAT}	0.525V_{BAT}	V
receiver hysteresis voltage	$V_{th(hys)RX}$	$V_{th(hys)RX}$= $V_{th(rec)RX}$-$V_{th(dom)RX}$			0.175V_{BAT}	V
slave resistance	R_{slave}	connected between pins LIN and V_{BAT}; V_{LIN}=0V; V_{BAT}=12V; V_{TXD}=V_{SLP_N}=5V	20	30	60	kΩ
capacitance on pin LIN	C_{LIN}				30	pF
dominant output voltage	$V_{o(dom)}$	Normal mode; V_{TXD}=0V; V_{BAT}=7V			1.4	V
		Normal mode; V_{TXD}=0V; V_{BAT}=18V			2.0	V
Thermal shutdown						
shutdown junction temperature	$T_{j(sd)}$		150	175	200	°C

(Unless specified otherwise; 5.5V≤V_{BAT}≤27V, -40°C≤T_{vj}≤150°C; typical in V_{BAT}=12V, T_{vj}＝25°C.)

Dynamic characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Duty cycles						
duty cycle 1	δ1 [1][2]	$V_{th(rec)(max)}$=0.744×V_{BAT}; $V_{th(dom)(max)}$=0.581×V_{BAT}; t_{bit}=50μs; V_{BAT}=7V~18V Fig 6	0.396			
		$V_{th(rec)(max)}$=0.76×V_{BAT}; $V_{th(dom)(max)}$=0.593×V_{BAT}; t_{bit}=50μs; V_{BAT}=5.5V~7V Fig 6	0.396			
duty cycle 2	δ2 [2][3]	$V_{th(rec)(min)}$=0.422×V_{BAT}; $V_{th(dom)(min)}$=0.284×V_{BAT}; t_{bit}=50μs; V_{BAT}=7.6V~18V Fig 6			0.581	
		$V_{th(rec)(min)}$=0.41×V_{BAT}; $V_{th(dom)(min)}$=0.275×V_{BAT}; t_{bit}=50μs; V_{BAT}=6.1V~7.6V Fig 6			0.581	
duty cycle 3	δ3 [1][2]	$V_{th(rec)(max)}$=0.778×V_{BAT}; $V_{th(dom)(max)}$=0.616×V_{BAT}; t_{bit}=96μs; V_{BAT}=7V~18V Fig 6	0.417			
		$V_{th(rec)(max)}$=0.797×V_{BAT}; $V_{th(dom)(max)}$=0.630×V_{BAT}; t_{bit}=96μs; V_{BAT}=5.5V~7V Fig 6	0.417			
duty cycle 4	δ4 [2][3]	$V_{th(rec)(min)}$=0.389×V_{BAT}; $V_{th(dom)(min)}$=0.251×V_{BAT}; t_{bit}=96μs; V_{BAT}=7.6V~18V Fig 6			0.590	
		$V_{th(rec)(min)}$=0.378×V_{BAT}; $V_{th(dom)(min)}$=0.242×V_{BAT}; t_{bit}=96μs; V_{BAT}=6.1V~7.6V Fig 6			0.590	
Timing characteristics						
receiver propagation delay	$t_{PD(RX)}$ [4]				6	μs

receiver propagation delay symmetry	$t_{PD(RX)sym}$ [4]		-2		2	μs
LIN dominant wake-up time	$t_{wake(dom)LIN}$	Sleep mode	30	80	150	μs
go to normal time	$t_{gotonorm}$		2	5	10	μs
go to sleep time	$t_{gotosleep}$		2	5	10	μs

(Unless specified otherwise; 5.5V≤V_{BAT}≤27V, -40°C≤T_{vj}≤150°C; typical in V_{BAT}=12V, T_{vj}=25°C.)

[1] $\delta 1, \delta 3 = \frac{t_{bus(rec)(\min)}}{2 \times t_{bit}}$

[2] Bus load conditions are: (1) C_L=1nF, R_L=1kΩ; (2) C_L=6.8nF, R_L=660Ω; (3) C_L=10nF, R_L=500Ω

[3] $\delta 2, \delta 4 = \frac{t_{bus(rec)(\max)}}{2 \times t_{bit}}$

[4] Load condition pin RXD: C_{TXD}=20pF, R_{RXD}=2.4kΩ

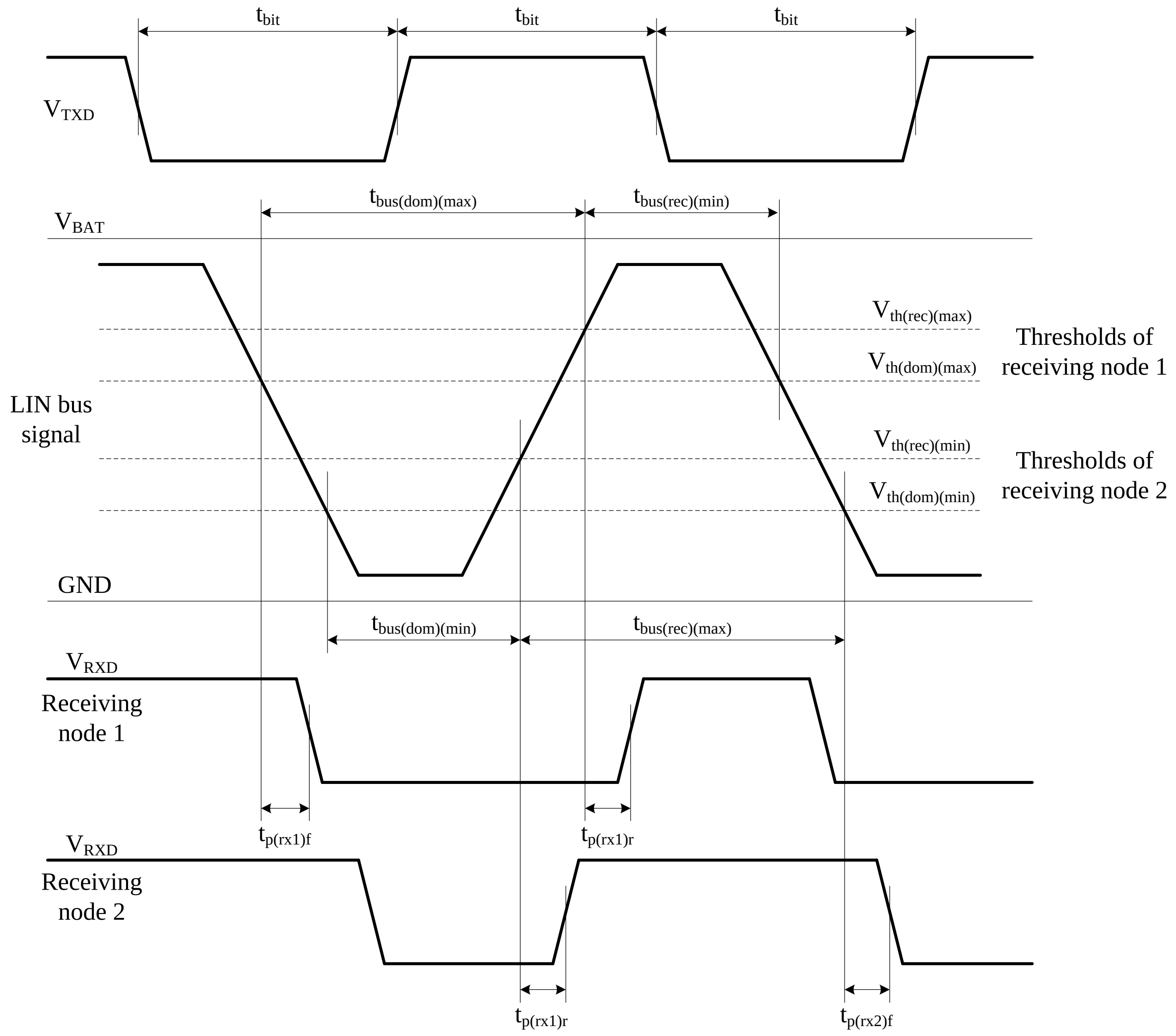


Fig 6. Timing diagram LIN transceiver

Typical Application

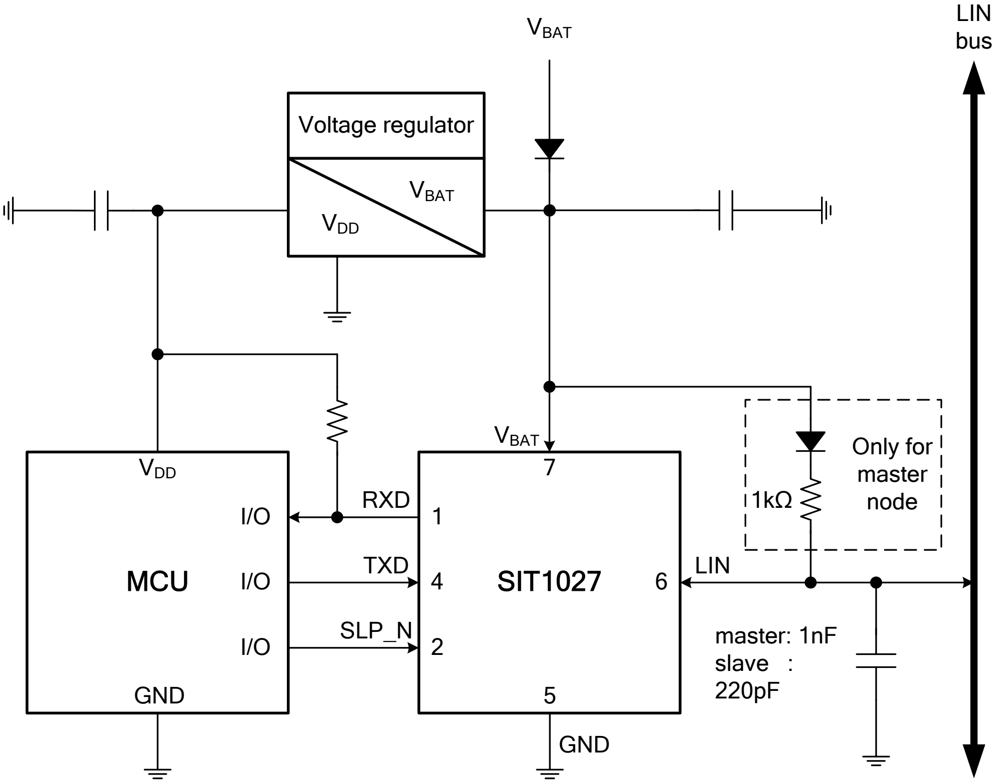


Fig 7. Typical application of the SIT1027

Timing test circuit

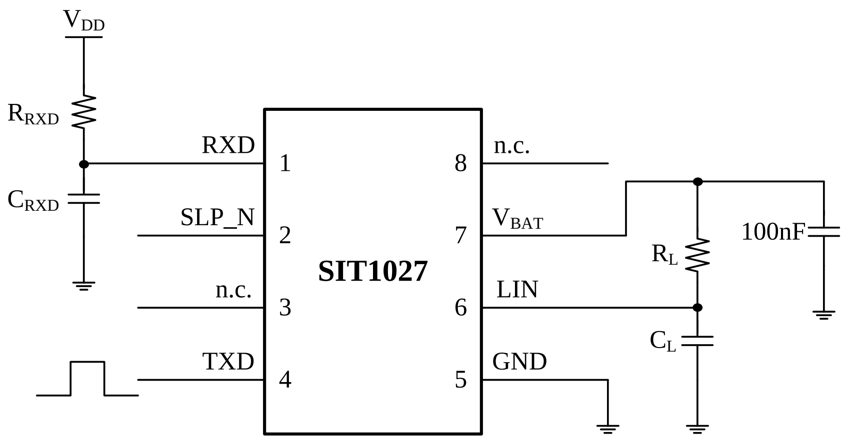
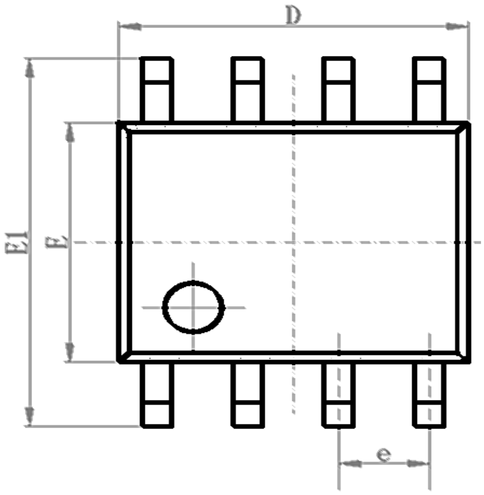


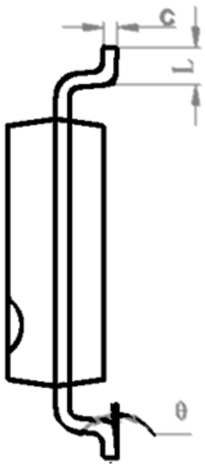
Fig 8. Timing test circuit for LIN transceiver

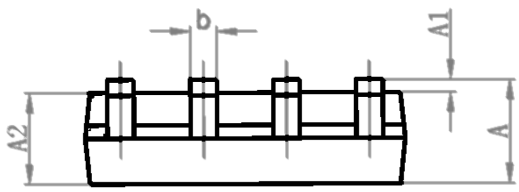
SOP8 Dimensions

PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.50	1.60	1.70
A1	0.1	0.15	0.2
A2	1.35	1.45	1.55
b	0.355	0.400	0.455
D	4.800	4.900	5.00
E	3.780	3.880	3.980
E1	5.800	6.000	6.200
e		1.270BSC	
L	0.40	0.60	0.80
c	0.153	0.203	0.253
θ	-2°	-4°	-6°



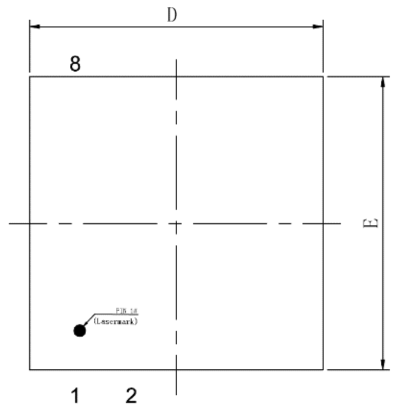


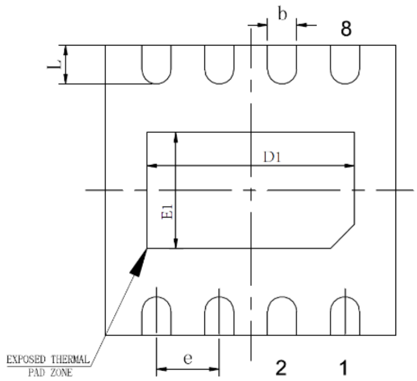


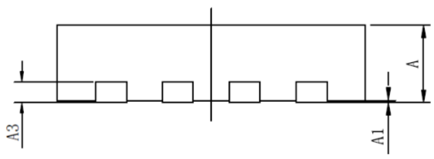
HVSON8 / DFN3*3-8 Dimensions

PACKAGE SIZE

SYMBOL	MIN/mm	TYP /mm	MAX/mm
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.05	2.15	2.25
E1	1.10	1.20	1.30
b	0.25	0.30	0.35
e	0.65 TYP		
L	0.35	0.40	0.45







Ordering Information

TYPE NUMBER	TEMPERATURE	PACKAGE
SIT1027T	-40℃~150℃	SOP8
SIT1027TK	-40℃~150℃	HVSON8 / DFN3*3-8，small outline package, no pin

SOP8 is packed with 2500 pieces/disc in braided packaging, with small outline package and 5000 pieces / disc in lead free packaging.

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.