

FEATURES

- Input voltage range: 3V to 40V
- Ultra-low quiescent current $<6\mu\text{A}$
- Low dropout voltage: 200mV @ 100mA
- Maximum output current: 300mA Ultra-low power sleep mode
- Shutdown current $<1\mu\text{A}$
- High PSRR 60dB @ 100Hz
- Stable with low-ESR ceramic output-stability capacitor (2.2 μF)
- Enable Pin (EN) withstand voltage: 40V
- Overcurrent protection, short-circuit protection
- Virtual junction temperature range: -40°C to 150°C
- Thermal shutdown and automatic restart recovery
- Built-in soft start
- Support ESOP8, EMSOP8 and SOT89-5 packages

PRODUCT APPEARANCE

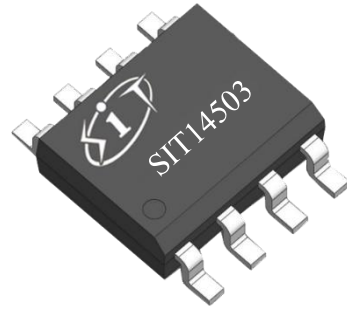


Fig 1 provides green, lead-free packaging

DESCRIPTION

The SIT14503 series is a low dropout linear regulator (LDO) with ultra-low quiescent current and a wide input voltage range of 3V to 40V. SIT14503 provides fixed output of 5V. In addition, the product family is available with fixed outputs of 2.5V, 3.3V and 15V, or adjustable outputs from 0.65V to 24V ⁽¹⁾, providing load currents up to 300mA. The quiescent current of the SIT14503 series is less than 1 μA when disabled and less than 6 μA at light loads. The power-good delay can be adjusted by external components, allowing the delay time to be configured to fit application-specific systems. It can be applied to the power management of automotive electronics, industrial control system and wide voltage battery power supply system.

NOTE ⁽¹⁾: If you need any other versions of the SIT14503 series except for the fixed 5V output, please contact the sales.

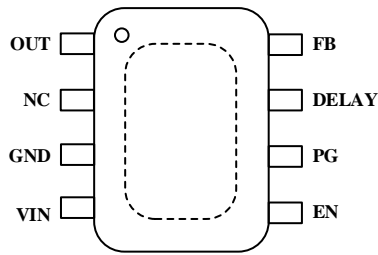
PIN CONFIGURATION


Fig 2 ESOP8 package pin configuration

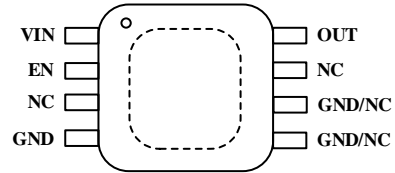


Fig 3 EMSOP8 package pin configuration

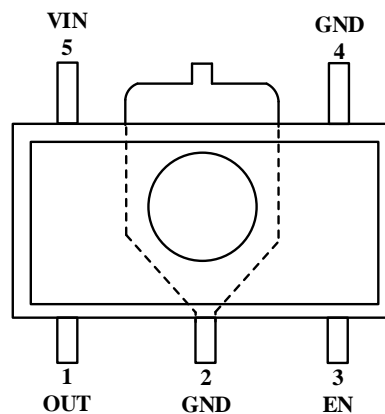


Fig 4 SOT89-5 package pin configuration

PIN DESCRIPTION

Table 1 ESOP8 package pin description

Pin	Symbol	Pin description
1	OUT	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use a 2.2- μ F or larger ceramic capacitor from OUT to GND.
2	NC	NC pin. This pin can either be left floating or connected to GND.
3	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
4	VIN	Input power-supply voltage pin. For best transient response and to minimize input impedance, place a 1- μ F or larger ceramic capacitor between the VIN and GND.
5	EN	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). Do not leave this pin floating because this pin is high impedance. If left floating, this pin

Pin	Symbol	Pin description
		may cause the device to enable or disable.
6	PG	Power-good pin. Power-good pin. This pin has an internal pullup resistor. Do not connect this pin to V_{OUT} or any other biased voltage rail. V_{PG} is logic level high when V_{OUT} is above the power-good threshold.
7	DELAY	Power-good delay adjustment pin. Connect a capacitor from this pin to GND to set the PG reset delay
8	FB	This pin is a feedback pin when using an external resistor divider. When using the adjustable device, this pin must be connected through a resistor divider to the output for the device to function.

Table 2 EMSOP8 package pin description

Pin	Symbol	Pin description
1	VIN	Input power-supply voltage pin. For best transient response and to minimize input impedance, place a 1- μ F or larger ceramic capacitor between the VIN and GND.
2	EN	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). Do not leave this pin floating because this pin is high impedance. If left floating, this pin may cause the device to enable or disable.
3	NC	NC pin. This pin can either be left floating or connected to GND.
4	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
5	GND/NC	Ground pin. Connect this pin to the thermal pad with a low-impedance connection or not connected.
6	GND/NC	Ground pin. Connect this pin to the thermal pad with a low-impedance connection or not connected.
7	NC	NC pin. This pin can either be left floating or connected to GND.
8	OUT	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use a 2.2- μ F or larger ceramic capacitor from OUT to GND.

Table 3 SOT89-5 package pin definition

Pin	Symbol	Pin description
1	OUT	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, use a 2.2- μ F or larger ceramic capacitor from OUT to GND.

Pin	Symbol	Pin description
2	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
3	EN	Enable pin. The device is disabled when the enable pin becomes lower than the enable logic input low level (V_{IL}). Do not leave this pin floating because this pin is high impedance. If left floating, this pin may cause the device to enable or disable.
4	GND	Ground pin. Connect this pin to the thermal pad with a low-impedance connection.
5	VIN	Input power-supply voltage pin. For best transient response and to minimize input impedance, place a 1 μ F or larger ceramic capacitor between the VIN and GND.

Note: for all packages, it is recommended that the thermal pad is soldered to board ground.

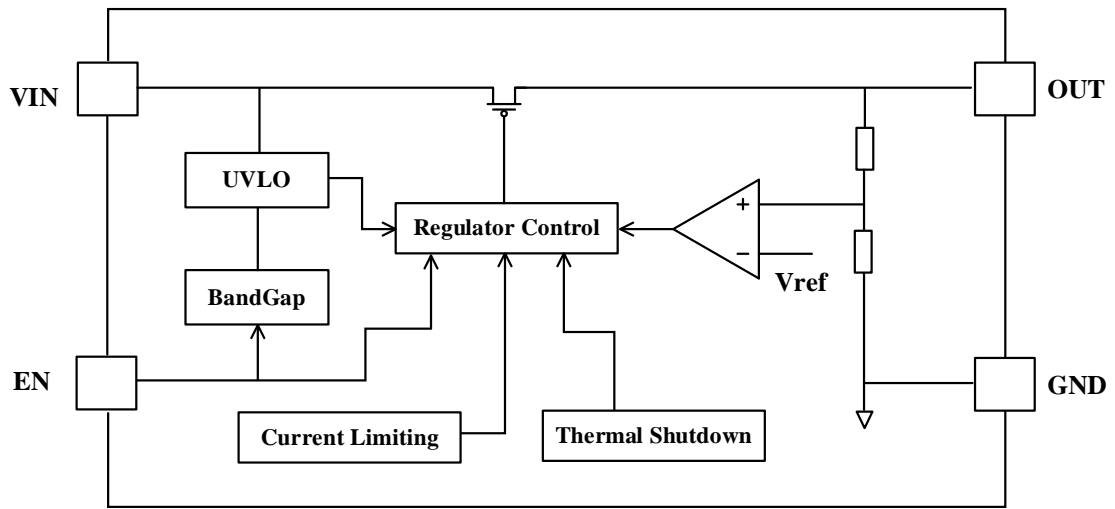
FUNCTIONAL BLOCK DIAGRAM


Fig 7 Internal block diagram of SIT14503 fixed output series

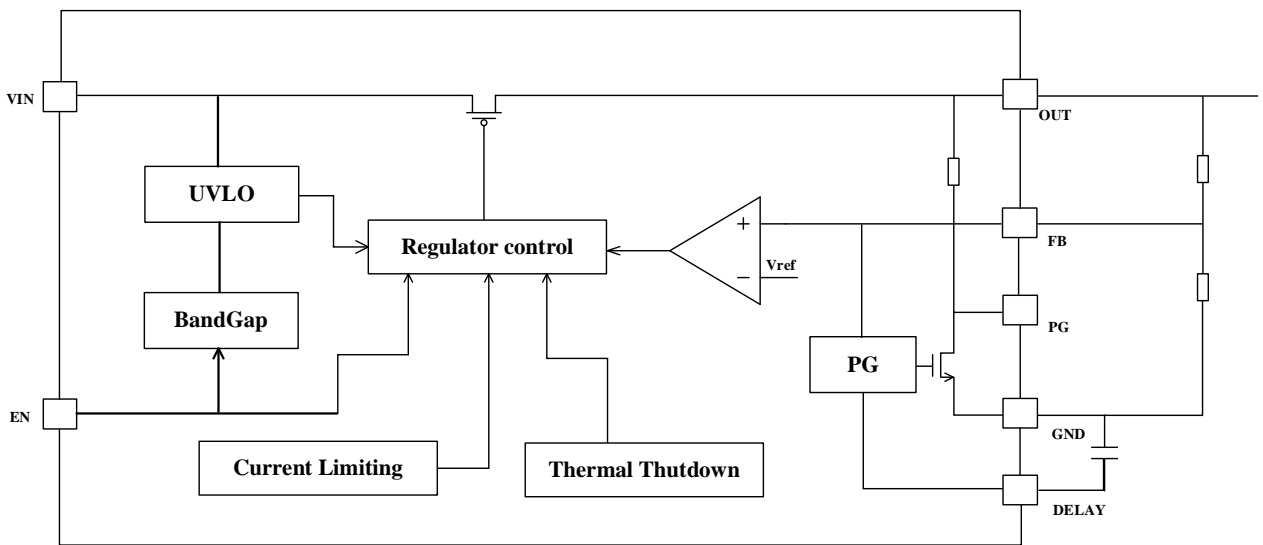


Fig 8 Internal block diagram of SIT14503 adjustable output series

FEATURE DESCRIPTION

1 Overview

The SIT14503 series is a low dropout linear regulator (LDO) with ultra-low quiescent current and a wide input voltage range of 3V to 40V. The quiescent current of the SIT14503 series is less than 1 μ A when disabled and less than 6 μ A at light loads.

The SIT14503 provides fixed output of 5V. In addition, the product family is available with fixed 2.5V, 3.3V and 15V outputs, or adjustable outputs from 0.65V to 24V ⁽¹⁾. The adjustable output voltage version uses an external resistance feedback, with a typical FB pin feedback voltage of 0.65V. The SIT14503 can provide a load current of up to 300mA.

The power-good delay can be adjusted by external components, allowing the delay time to be configured to fit application-specific systems. When OUT reaches the PG threshold $V_{(PG-rise)}$, the Delay pin starts to output current $I_{(Charge)}$. When the Delay pin voltage reaches $V_{(RISE)}$, PG is allowed to pull up. The user can select the appropriate Delay capacitor according to the MCU delay requirements.

The SIT14503 series features built-in protection against overcurrent, thermal shutdown and automatic restart.

NOTE ⁽¹⁾: If you need any other versions of the SIT14503 series except for the fixed 5V output, please contact the sales.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Input voltage	VIN	-0.3	42	V
Enable voltage	EN	-0.3	VIN	V
Feedback voltage	FB	-0.3	6	V
Power good	PG	-0.3	VIN	V
Output voltage	OUT	-0.3	VIN	V
Delay	DELAY	-0.3	6	V
Ambient temperature	T _{amb}	-40	125	°C
Virtual junction temperature	T _j	-40	150	°C
Storage temperature	T _{stg}	-55	150	°C

Note: The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

DC CHARACTERISTICS

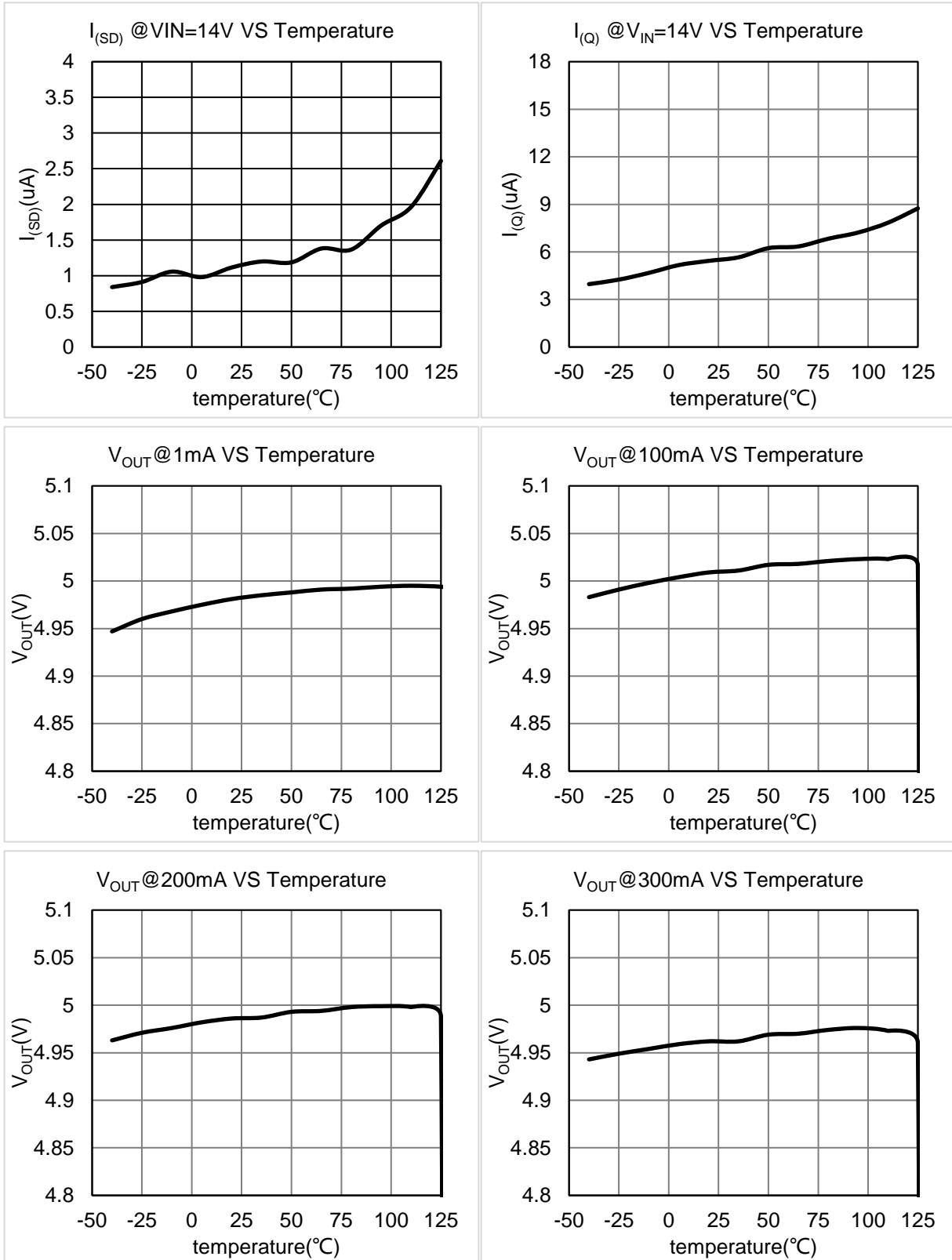
Unless otherwise stated, specified at $-40^{\circ}\text{C} \leq T_{\text{amb}} \leq 125^{\circ}\text{C}$. Typical values are all at $V_{\text{IN}}=14\text{V}$, $C_{\text{out}} = 10\mu\text{F}$, $T_{\text{amb}}=25^{\circ}\text{C}$.

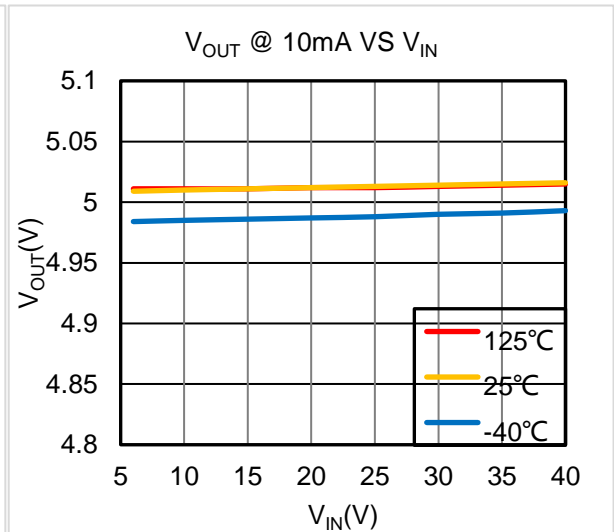
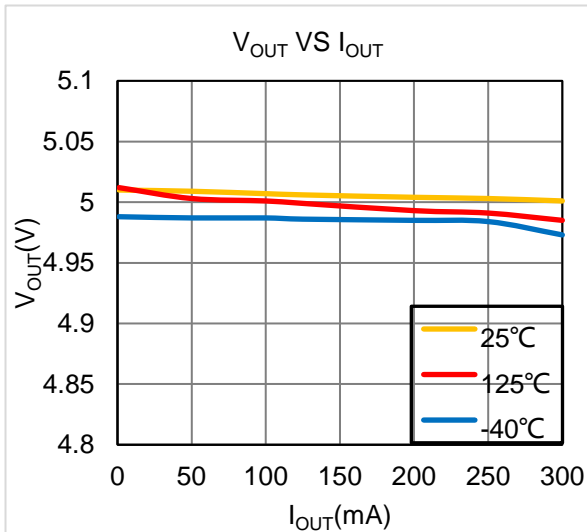
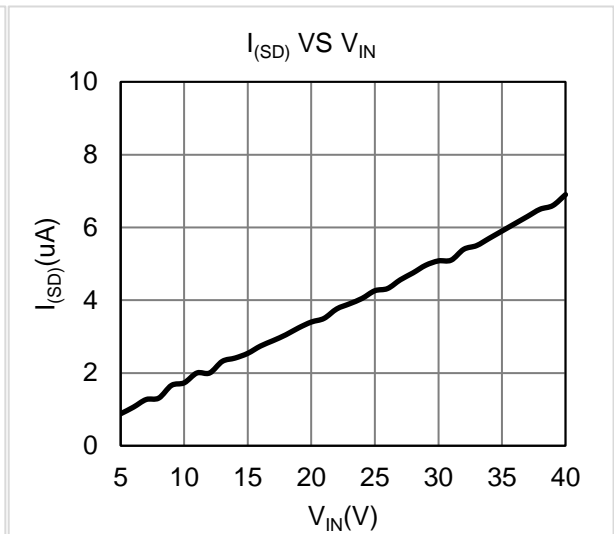
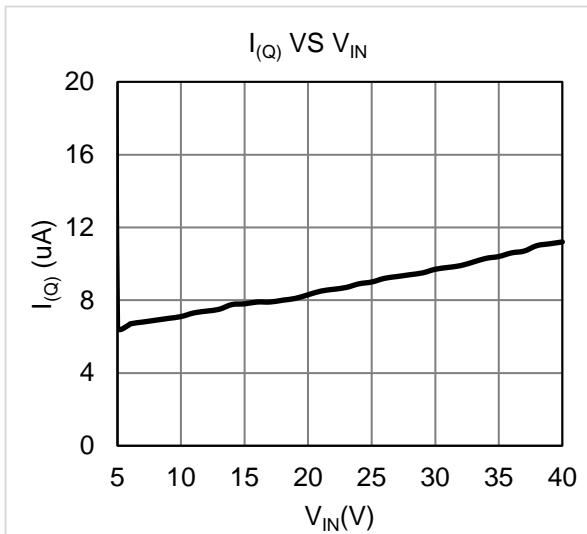
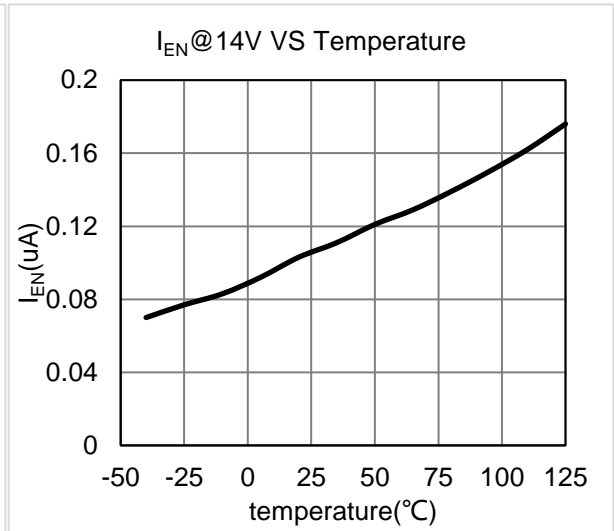
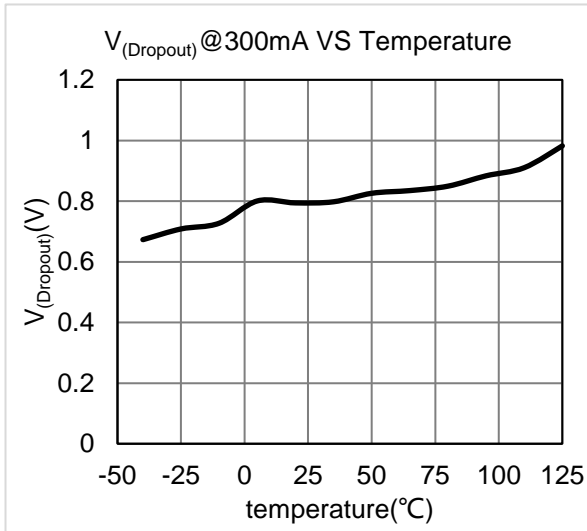
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE AND CURRENT						
V_{IN}	Input voltage		3		40	V
$I_{(\text{SD})}$	Shutdown current	EN=0, $V_{\text{IN}}=14\text{V}$		1	3	μA
$I_{(\text{Q})}$	Quiescent current	EN=5, $V_{\text{IN}}=14\text{V}$ $I_{\text{OUT}}=0\text{A}$		6	15	μA
ENABLE INPUT (EN)						
V_{IL}	Logic input low level				0.7	V
V_{IH}	Logic input high level		2			V
I_{EN}	EN pin input current	EN=5V		0.1	0.5	μA
REGULATED OUTPUT						
V_{OUT}	Output voltage (fixed output version)	$V_{\text{IN}} = \text{OUT} + V_{(\text{Dropout})}$ to 40 V, $I_{\text{OUT}} = 1\text{mA}$ to I_{MAX}	-2		2	%
$V_{(\text{Line-Reg})}$	Line regulation	$V_{\text{IN}} = 6\text{V}$ to 40 V, $I_{\text{OUT}} = 10\text{mA}$			20	mV
$V_{(\text{Load-Reg})}$	Load regulation	$V_{\text{IN}} = 14\text{V}$, $I_{\text{OUT}} = 1\text{mA}$ to I_{MAX}			40	mV
DROP OUT						
$V_{(\text{Dropout})100\text{mA}}$	Dropout voltage	OUT=5V, $I_{\text{OUT}}=100\text{mA}$		210	390	mV
$V_{(\text{Dropout})200\text{mA}}$	Dropout voltage	OUT=5V, $I_{\text{OUT}}=200\text{mA}$		420	780	mV
$V_{(\text{Dropout})300\text{mA}}$	Dropout voltage	OUT=5V, $I_{\text{OUT}}=300\text{mA}$		630	1170	mV
OVER CURRENT PROTECTION						
$I_{(\text{CL})-300\text{mA}}$	Output overcurrent limit			600		mA
PSRR						
PSRR	Power supply rejection ratio	$I_{\text{OUT}} = 10\text{mA}$, frequency=100 Hz, $C_{\text{OUT}}=2.2\mu\text{F}$		60 ⁽¹⁾		dB
THERMAL SHUTDOWN						
$T_{(\text{SD})}$	Junction shutdown temperature			175 ⁽¹⁾		$^{\circ}\text{C}$
$T_{(\text{REC})}$	Overtemperature recovery			155 ⁽¹⁾		$^{\circ}\text{C}$

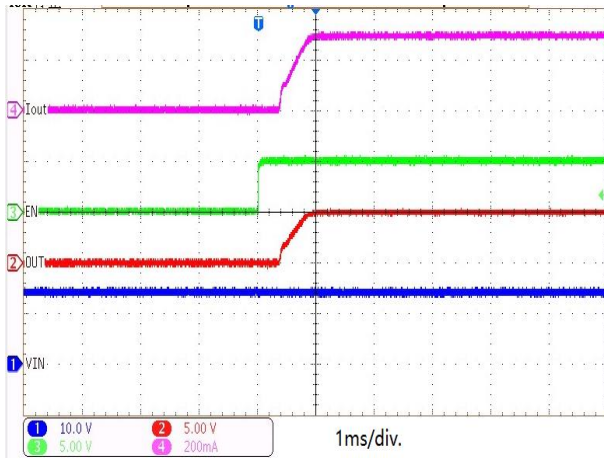
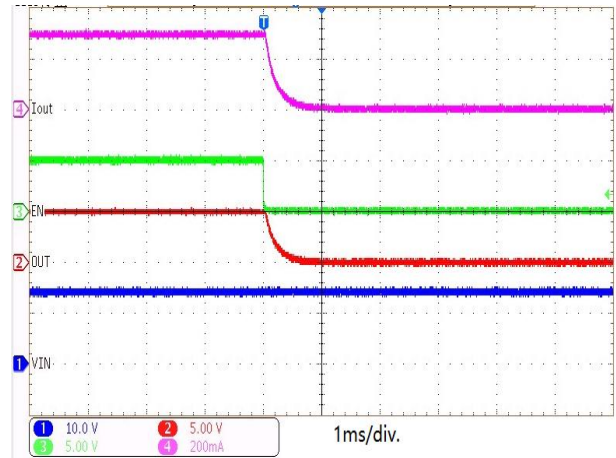
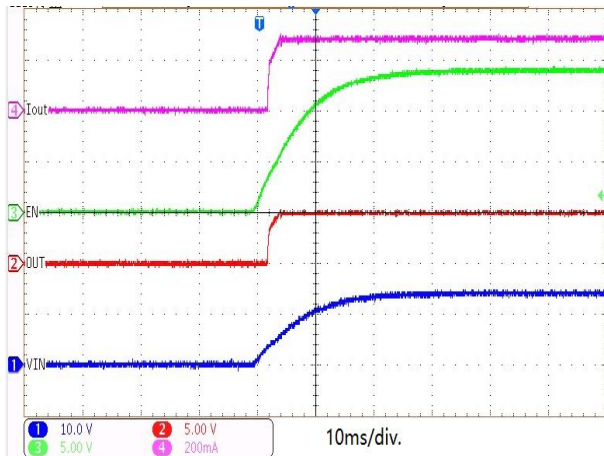
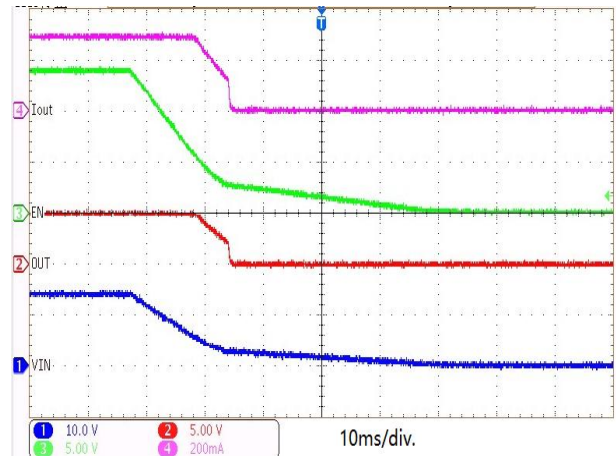
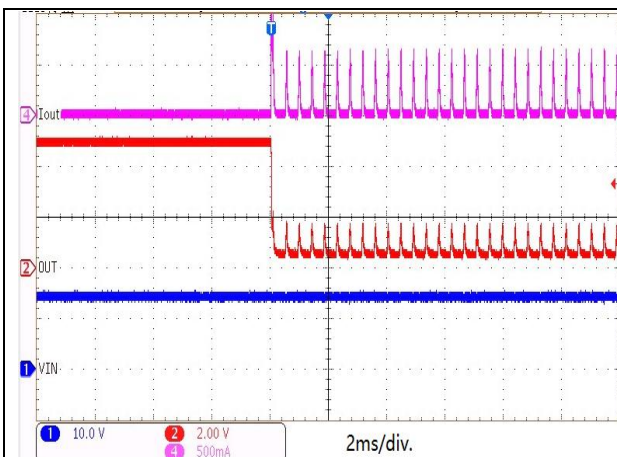
Note ⁽¹⁾: guaranteed by designed, not tested in production.

ESD PERFORMANCE

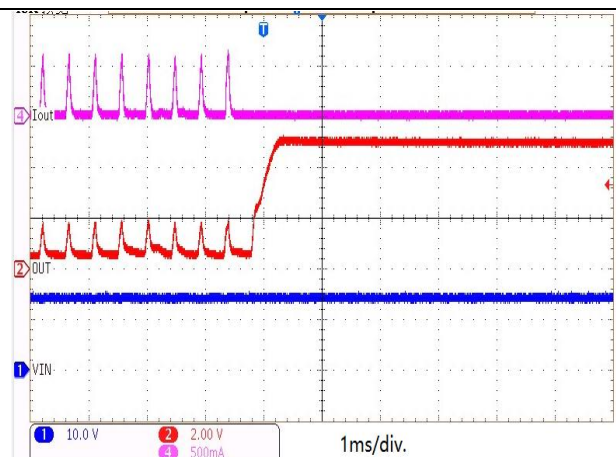
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{ESD}	HBM				±3	kV
	CDM				±750	V

TYPICAL CHARACTERISTIC


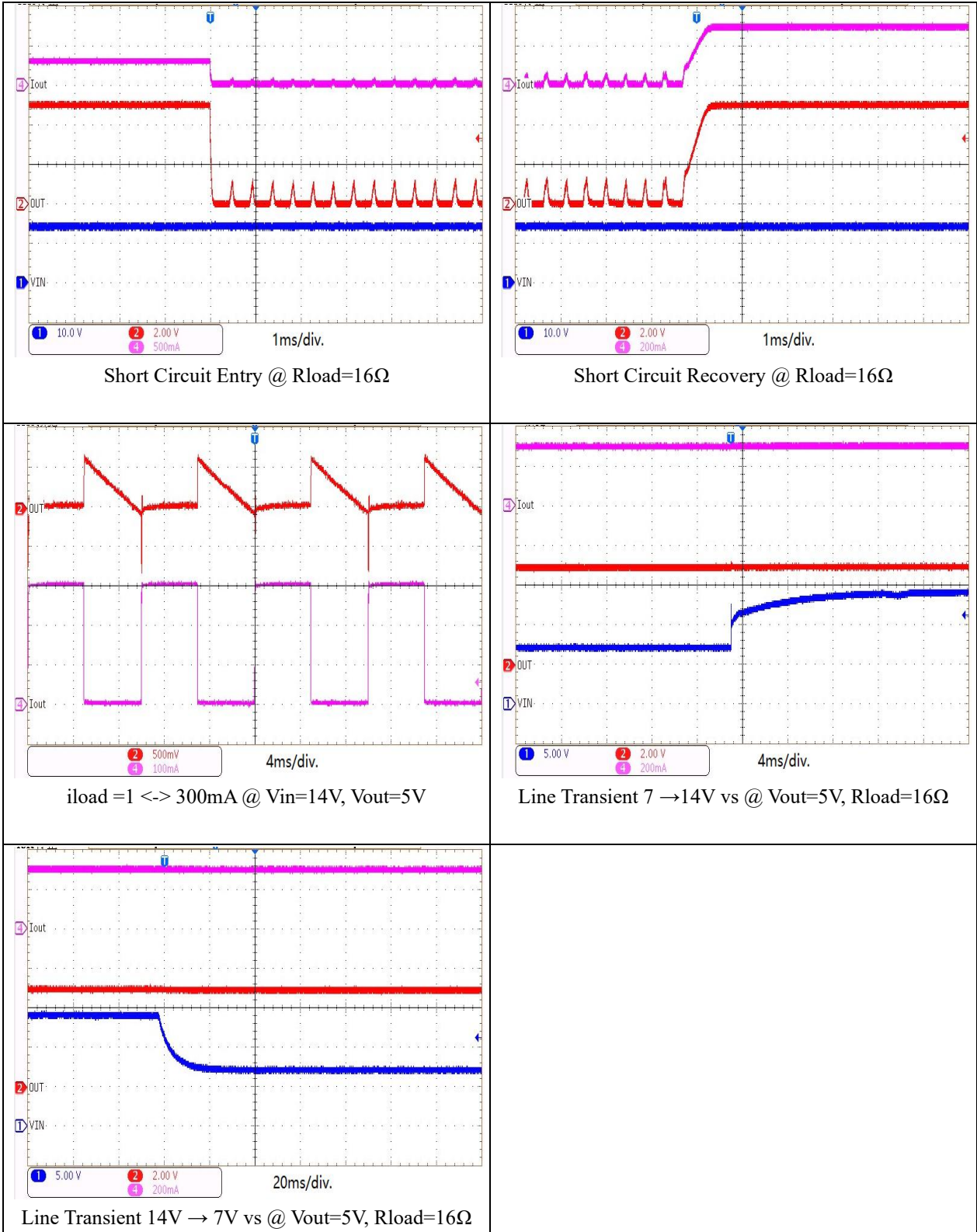


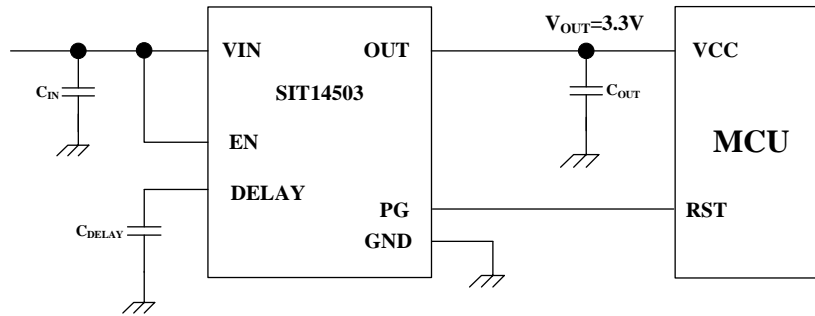
TYPICAL WAVEFORM

 EN=L→H @ $V_{in}=14V$, $V_{out}=5V$, $R_{load}=16\Omega$

 EN=H→L @ $V_{in}=14V$, $V_{out}=5V$, $R_{load}=16\Omega$

 Power-Up @ $V_{in}=V_{EN}=14V$, $V_{out}=5V$, $R_{load}=16\Omega$

 Power-OFF @ $V_{in}=14V$, $V_{out}=5V$, $R_{load}=16\Omega$


Short Circuit Entry @ no load

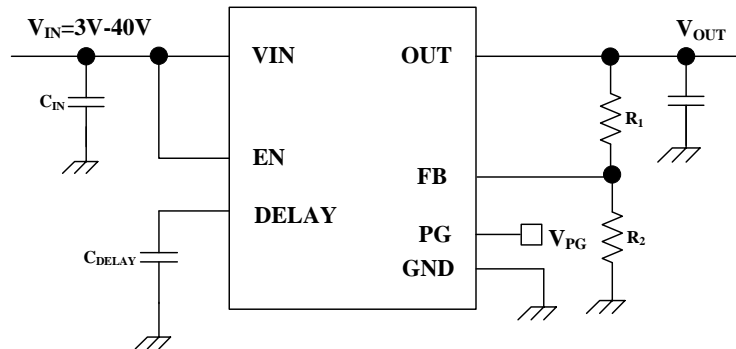


Short Circuit Recovery @ no load

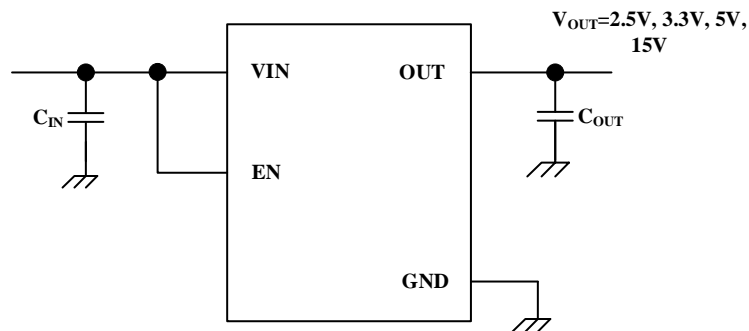


TYPICAL APPLICATION


Note: To select a capacitor for DELAY, use below equation: $C_{DELAY} = \frac{I_{(Charge)} \times t_{Delay}}{V_{(Rise)}}$

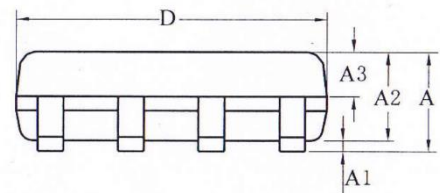
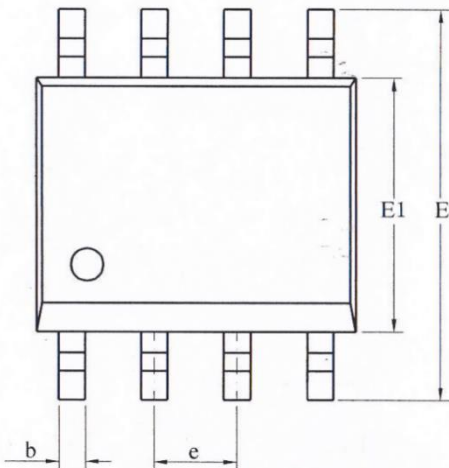
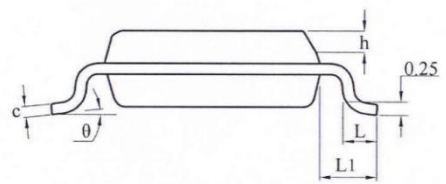
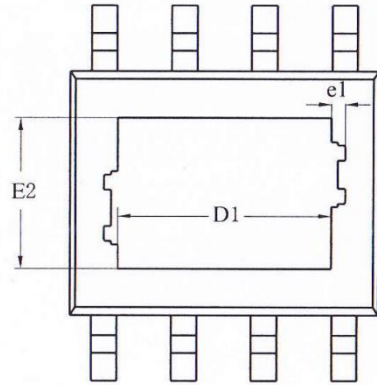
Fig 9 Typical application diagram


Note: calculate the value for V_{out} using the following equation: $V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \times V_{FB}$, it is recommended the $R_2=650k\Omega \pm 1\%$, and the temperature coefficient is less than 100 ppm.

Fig 10 SIT14503/P full function application diagram

Fig 11 SIT14503/P simplest application diagram

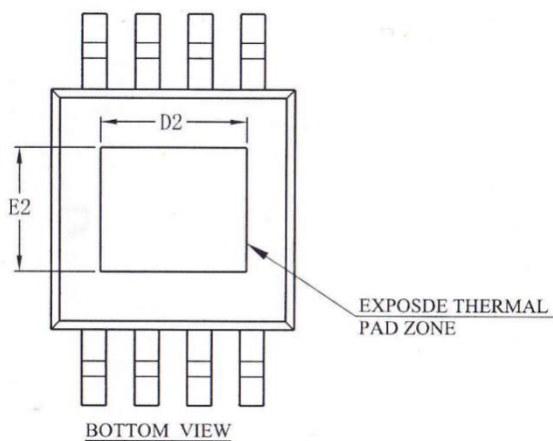
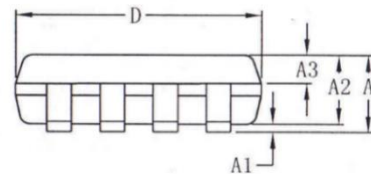
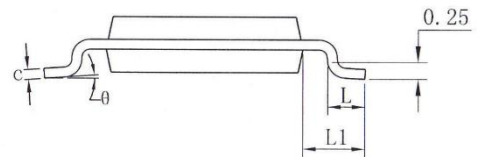
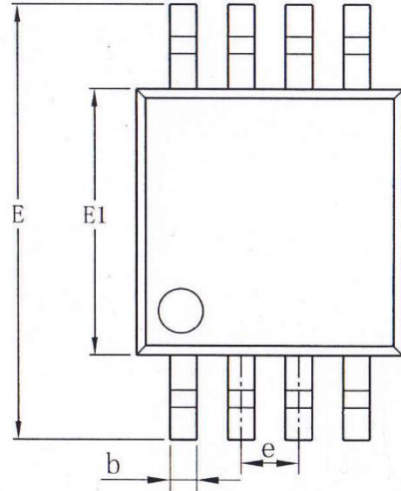
ESOP8 DIMENSION
PACKAGE SIZE

Symbol	Min./mm	Typ./mm	Max./mm
A	-	-	1.65
A1	0.05	-	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
c	0.20	-	0.24
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	-	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0°	-	8°



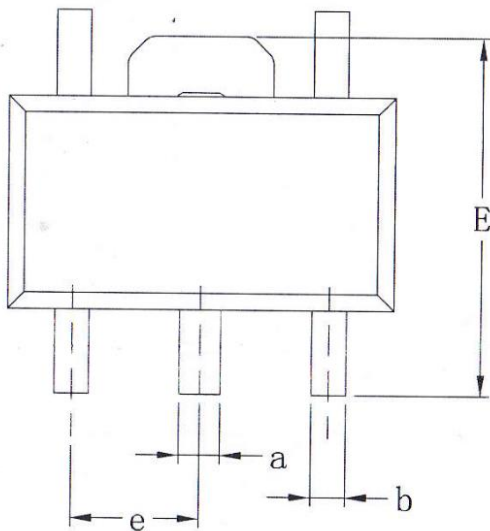
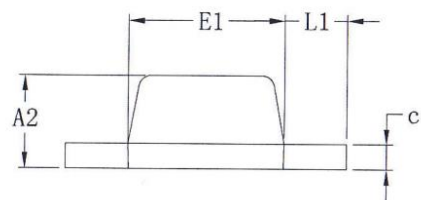
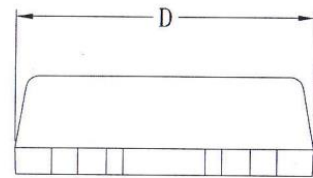
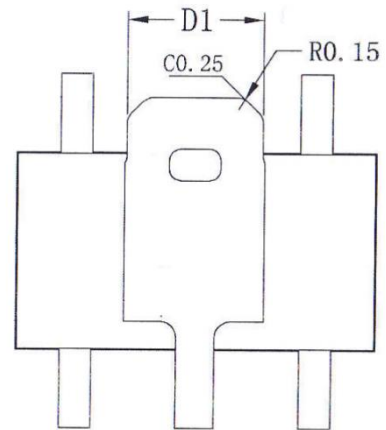
EMSOP8 DIMENSION
PACKAGE SIZE

Symbol	Min./mm	Typ./mm	Max./mm
A	-	-	1.10
A1	0.05	-	0.15
A2	0.75	0.85	0.95
A3	0.30	0.35	0.40
b	0.28	-	0.36
c	0.15	-	0.19
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	-	0.70
L1	0.95REF		
θ	0°	-	8°



SOT89-5 DIMENSION
PACKAGE SIZE

Symbol	Min./mm	Typ./mm	Max./mm
A2	1.40	1.50	1.60
b	0.38	-	0.46
c	0.38	-	0.42
a	0.46	-	0.56
D	4.40	4.50	4.60
D1	1.62	-	1.83
E	3.95	3.90	4.25
E1	2.40	2.50	2.60
e	1.50BSC		
L	0.89	-	1.20
L1	1.05REF		



THERMAL INFORMATION

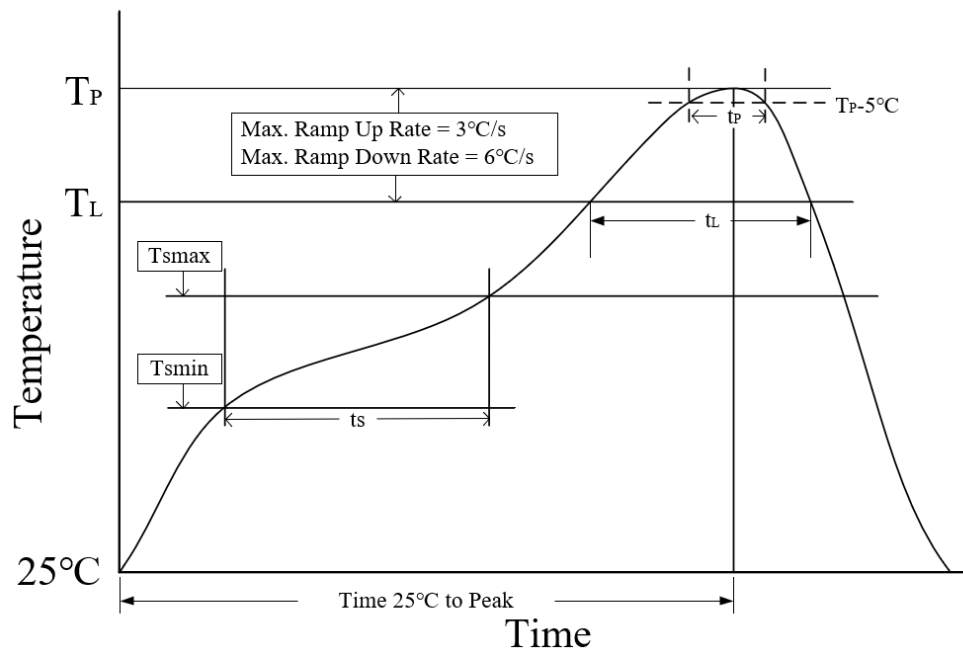
Symbol	Parameter	Package	Value	Unit
R _{θJA}	Junction-to-Ambient Thermal Resistance	ESOP8	42	°C/W
		EMSOP8	67	°C/W
		SOT89-5	50	°C/W
R _{θJC}	Junction-to-Case Thermal Resistance	ESOP8	8	°C/W
		EMSOP8	40	°C/W
		SOT89-5	44	°C/W

Note: According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board.

ORDERING INFORMATION

Type number	Output voltage	Output current	PG function	Package	Packing
SIT14503QT/P	5V	300mA	√	ESOP8	盘装编带
SIT14503QU	5V	300mA	×	EMSOP8	盘装编带
SIT14503QS	5V	300mA	×	SOT89-5	盘装编带

2500 pieces/disc in taped packages.

REFLOW SOLDERING


Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	$3^\circ\text{C/second max}$
Preheat time t_s ($T_{smin}=150^\circ\text{C}$ to $T_{smax}=200^\circ\text{C}$)	60-120 seconds
Melting time t_L ($T_L=217^\circ\text{C}$)	60-150 seconds
Peak temp T_P	$260-265^\circ\text{C}$
5°C below peak temperature t_p	30 seconds
Ave cooling rate (T_P to T_L)	$6^\circ\text{C/second max}$
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	September 2023