FEATURES

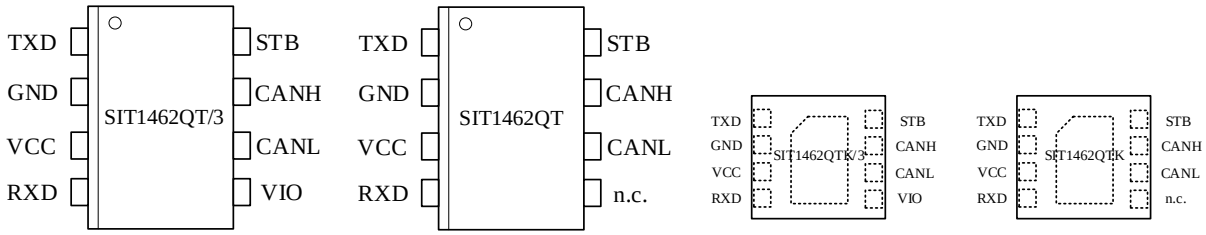
- ISO 11898-2:2024, SAE J2284-1~ SAE J2284-5 and SAE J1939-14 compliant;
- Implements CAN Signal Improvement Capability as defined in CiA 601-4:2019;
- Thermally protected;
- ±40V BUS protection;
- Driver (TXD) dominant time-out function;
- Low power Standby mode with remote and local wake-up capability;
- SIT1462Q/3 I/O pins supports 1.8V, 3.3V and 5V MCU;
- Undervoltage protection on pins VCC and VIO;
- High-speed CAN, support 5Mbps CAN with Flexible Data-Rate and 8Mbps CAN with Flexible Data-Rate in point-to point networks;
- High ElectroMagnetic Immunity;
- Unpowered state disengages from the bus;
- Available in SOP8 and DFN3*3-8 packages.

DESCRIPTION

SIT1462Q is an interface chip applied between the CAN protocol controller and the physical two-wire CAN bus. It features a much tighter bit timing symmetry performance to enable CAN FD communication up to 8Mbit/s, and has the capability of differential signal transmission between bus and CAN protocol controller.

Parameter	Symbol	Min	Max	Unit
VCC supply voltage	VCC	4.5	5.5	V
VIO supply voltage	VIO	1.7	5.5	V
CANH, CANL input / output voltage	V_{can}	-40	+40	V
Bus differential voltage	V_{diff}	1.5	3.0	V
Ambient temperature	T_{amb}	-40	125	℃
Storage temperature	T_{stg}	-55	150	℃

PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Description
1	TXD	Transmit data input.
2	GND	Ground.
3	VCC	5V supply voltage input.
4	RXD	Receive data output.
5	VIO	Supply voltage input for I/O level adapter in SIT1462Q/3.
	n.c.	Not connected in SIT1462Q.
6	CANL	LOW-level CAN bus line.
7	CANH	HIGH-level CAN bus line.
8	STB	Standby mode control input; active-HIGH.

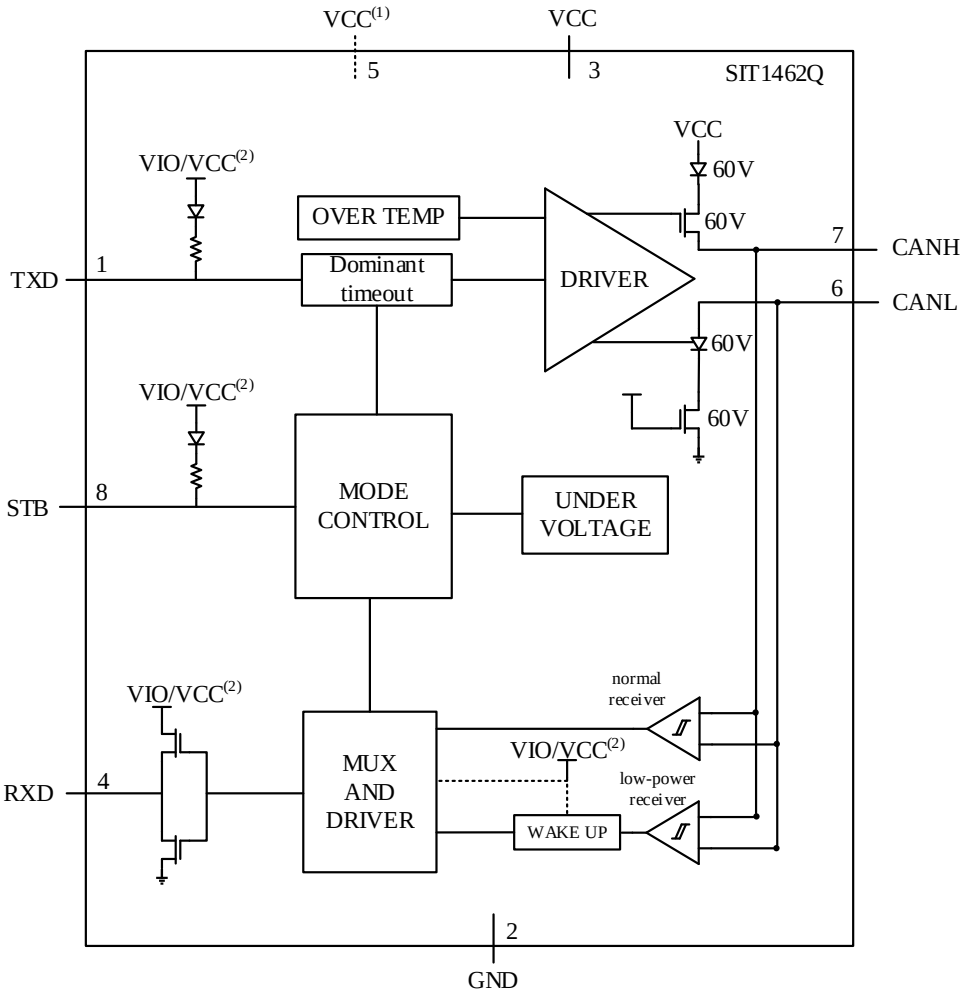
Note: The metal pad on the back of the DFN3*3-8 package is recommended to be grounded.

LIMITING VALUES

Parameter	Symbol	Conditions	Value	Unit
Supply voltage	V_{CC}, V_{VIO}	pins VCC, VIO	-0.3~+7	V
MCU side ports voltage	V_{TXD}, V_{RXD}, V_{STB}	pins TXD, RXD, STB	-0.3~+7	V
Voltage between pin CANH and pin CANL	V_{CANL}, V_{CANH}	pins CANH, CANL	-40~+40	V
Bus differential voltage withstand	$V_{CANH-CANL}$		-40~+40	V
electrostatic discharge voltage	V_{ESD}	IEC 61000-4-2: on pins CANH, CANL	-10~+10	kV
		Human-body model (HBM), per AEC Q100-002		
		all pins	-4~+4	kV
		pins CANH and CANL with respect to GND	-8~+8	kV
		Charged Device Model (CDM)		
		on corner pins	-750~+750	V
		on corner pins	-500~+500	V
transient voltage	Vtrt	Transient Immunity ISO 7637-2 on Bus Pins		
		pulse 1	-100	V
		pulse 2a	75	V
		pulse 3a	-150	V
		pulse 3b	100	V
Storage temperature	T_{stg}		-55~150	℃
Virtual junction temperature	T_j		-40~150	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

BLOCK DIAGRAM



(1) VIO is only available in the SIT1462Q/3, pin 5 is not connected in the SIT1462Q;

(2) VIO in SIT1462Q/3; VCC in SIT1462Q.

STATIC CHARACTERISTICS

Unless specified otherwise; all values are tested in recommended operating conditions: T_j=-40℃~150℃, V_{CC}=4.5V~5.5V, V_{IO}=1.7V~5.5V (SIT1462Q/3), R_L=60Ω.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply characteristics: pin VCC						
Supply voltage	V_{CC}		4.5	-	5.5	V
Standby undervoltage detection voltage	$V_{uvd(stb)}$		3.4	-	4.5	V
Standby undervoltage hysteresis voltage	$V_{uvhys(stb)}$		50	-	-	mV
Switch-off undervoltage detection voltage	$V_{uvd(swoff)}$	SIT1462Q	0.95	-	1.65	V
VCC supply current	I_{CC}	Normal mode; dominant; $t<t_{to(dom)TXD}$; V_{TXD}=0V	-	40	70	mA
		Normal mode; dominant; short circuit on bus lines; V_{TXD}=0V; -3V< (V_{CANH}=V_{CANL}) <+40V	-	-	125	mA
		Normal mode; recessive; V_{TXD}=V_{IO} (1)	-	4.2	10	mA
		Standby mode; SIT1462Q/3	-	-	2	μA
		Standby mode; SIT1462Q	-	-	21	μA
I/O level adapter supply; pin VIO (SIT1462Q/3)						
Supply voltage	V_{IO}		1.7		5.5	V
Switch-off undervoltage detection voltage	$V_{uvd(swoff)}$		0.95		1.65	V
VIO supply current	I_{IO}	Normal mode; dominant; V_{TXD}=0V		240	760	μA
		Normal mode; recessive; V_{TXD}=V_{IO} (1)		120	460	μA
		Standby mode			21	μA
Pin TXD characteristics						
HIGH-level input voltage	V_{IH}		0.7 V_{IO} (1)	-	-	V
LOW-level input voltage	V_{IL}		-	-	0.3 V_{IO} (1)	V
Hysteresis voltage	$V_{hys(TXD)}$		50	-	-	mV
Pull-up resistance	R_{pu}		20	-	80	kΩ
Input capacitance	C_i		-	-	10	pF
Pin RXD characteristics						
HIGH-level output current	$I_{OH(RXD)}$	V_{RXD}=V_{IO}-0.4V (1)	-10	-	-1	mA
LOW-level output current	$I_{OL(RXD)}$	Bus dominant; V_{RXD}=0.4V	1	-	10	mA
Pin STB characteristics						
HIGH-level input voltage	V_{IH}		0.7V_{IO} (1)	-	-	V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LOW-level input voltage	V_{IL}		-	-	$0.3V_{IO}$ (1)	V
Hysteresis voltage	$V_{hys(STB)}$		50	-	-	mV
Pull-up resistance	R_{pu}		20	-	80	kΩ
Input capacitance	C_i		-	-	10	pF
Overtemperature protection						
Shutdown junction temperature	$T_{j(sd)}$		165	-	185	℃
Release shutdown junction temperature	$T_{j(sd)rel}$		155	-	175	℃
Bus lines; pins CANH and CANL						
Dominant output voltage on pin CANH	$V_{O(dom)}$	$t<t_{to(dom)TXD}$; V_{TXD}=0V; R_L=50Ω to 65Ω	2.89	3.55	4.26	V
Dominant output voltage on pin CANL			0.77	1.45	2.13	V
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym}=V_{CANH}+V_{CANL}$; C_{SPLIT}=4.7nF; f_{TXD}=250kHz, 1MHz or 2.5MHz	0.9V_{CC}	-	1.1V_{CC}	V
Common mode voltage step	$V_{cm(step)}$		-150	-	150	mV
Peak-to-peak common mode voltage	$V_{cm(p-p)}$		-300	-	300	mV
Differential output voltage	$V_{O(diff)}$	Normal mode; $t<t_{to(dom)TXD}$; V_{TXD}=0V; V_{CC}=4.5V to 5.5V; R_L=50Ω to 65Ω	1.5	-	3	V
		Normal mode; $t<t_{to(dom)TXD}$; V_{TXD}=0V; V_{CC}=4.5V to 5.5V; R_L=45Ω to 70Ω	1.4	-	3.3	V
		Normal mode; dominant; $t<t_{to(dom)TXD}$; V_{TXD}=0V; V_{CC}=4.5V to 5.5V; R_L=2240Ω	1.5	-	5	V
		Normal mode; $V_{TXD}=V_{IO}$; 错误!未找到引用源。 No load	-500	-	+50	mV
		Standby mode; No load	-0.2	-	+0.2	V
Output voltage	$V_{O(rec)}$	Normal mode; $V_{TXD}=V_{IO}$; 错误!未找到引用源。 No load	2	2.5	3	V
		Standby mode; No load	-0.1	-	+0.1	V
Differential receiver threshold voltage	$V_{th(RX)diff}$	Normal mode; -12V≤V_{CANH}≤12V; -12V≤V_{CANL}≤12V	0.5	-	0.9	V
		Standby mode; -12V≤V_{CANH}≤12V; -12V≤V_{CANL}≤12V	0.4	-	1.1	V
receiver recessive voltage	$V_{rec(RX)}$	Normal mode; -12V≤V_{CANH}≤12V; -12V≤V_{CANL}≤12V	-4	-	0.5	V
		Standby mode; -12V≤V_{CANH}≤12V; -12V≤V_{CANL}≤12V	-4	-	0.4	V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
receiver dominant voltage	$V_{dom(RX)}$	Normal mode; -12V≤V_{CANH}≤12V; -12V≤V_{CANL}≤12V	0.9	-	9	V
		Standby mode; -12V≤V_{CANH}≤12V; -12V≤V_{CANL}≤12V	1.1	-	9	V
differential receiver hysteresis voltage	$V_{hys(RX)dif}$	Normal mode; -12V≤V_{CANH}≤12V; -12V≤V_{CANL}≤12V	80	-	-	mV
short-circuit output current	$I_{O(SC)}$	V_{CANH}=-15V to 40V; V_{CANL}=-15V to 40V		-	115	mA
recessive short-circuit output current	$I_{O(SC)rec}$	V_{CANH}=-27V to 32V; V_{CANL}=-27V to 32V; V_{TXD}=V_{IO} for t>$t_{d(TXD-busrec)end}$	-5		5	mA
leakage current	I_L	V_{CC}=V_{IO}= 0V or pins shorted to GND via 47kΩ; V_{CANH}=V_{CANL}=5V	-10		10	μA
input resistance	R_i	-2V≤V_{CANH}≤7V; -2V≤V_{CANL}≤7V	25	40	50	kΩ
input resistance deviation	$\triangle R_i$	0V≤V_{CANH}≤5V; 0V≤V_{CANL}≤5V	-3		3	%
differential input resistance	R_{ID}	-2V≤V_{CANH}≤7V; -2V≤V_{CANL}≤7V	50	80	100	kΩ
common-mode input capacitance	$C_{i(cm)}$ (2)		-	-	40	pF
differential input capacitance	$C_{i(diff)}$ (2)		-	-	20	pF

DYNAMIC CHARACTERISTICS

Unless specified otherwise; all values are tested in recommended operating conditions: T_j=-40℃~150℃, V_{CC}=4.5V~5.5V, V_{IO}=1.7V~5.5V (SIT1462Q/3), R_L=60Ω.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CAN timing characteristics; $t_{bit(TXD)}$≥125ns; Figure 1 and Figure 3.						
Delay time from TXD to bus dominant	$t_{d(TXD-busdom)}$	Normal mode	-	-	80	ns
Delay time from TXD to bus recessive	$t_{d(TXD-busrec)}$	Normal mode	-	-	80	ns
Delay time from bus dominant to RXD	$t_{d(busdom-RXD)}$	Normal mode	-	-	110	ns
Delay time from bus recessive to RXD	$t_{d(busrec-RXD)}$	Normal mode	-	-	110	ns
Delay time from TXD LOW to RXD LOW	$t_{d(TXDL-RXDL)}$	Normal mode	-	-	190	ns
Delay time from TXD HIGH to RXD HIGH	$t_{d(TXDH-RXDH)}$	Normal mode			190	ns
CAN FD timing characteristics according to (CiA 601-4:2019); $t_{bit(TXD)}$≥125ns; Figure 1 and Figure 4.						
Signal improvement time	$t_{SIC\_TXD\_base}$			-	530	ns
Transmitted recessive bit width deviation	$\Delta t_{bit(bus)}$ (2)	$\Delta t_{bit(bus)}$=$t_{bit(bus)}$-$t_{bit(TXD)}$	-10	-	10	ns
Receiver timing symmetry	Δt_{rec} (2)	Δt_{rec}=$t_{bit(RXD)}$- $t_{bit(bus)}$	-20	-	15	ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Received recessive bit width deviation	$\Delta t_{bit(RXD)}$ (2)	$\Delta t_{bit(RXD)}=t_{bit(RXD)}-t_{bit(TXD)}$	-30	-	20	ns
CAN FD timing characteristics according to ISO 11898-2:2016; Figure 1 and Figure 4.						
Transmitted recessive bit width	$t_{bit(bus)}$	2Mbit/s; ($t_{bit(TXD)}$=500ns)	480	-	520	ns
		5Mbit/s; ($t_{bit(TXD)}$=200ns)	180	-	210	ns
		8Mbit/s; ($t_{bit(TXD)}$=125ns)	115		135	ns
Receiver timing symmetry	Δt_{rec}	2Mbit/s	-65	-	40	ns
		5Mbit/s	-45	-	15	ns
		8Mbit/s	-20		15	ns
Bit time on pin RXD	$t_{bit(RXD)}$	2Mbit/s; ($t_{bit(TXD)}$=500ns)	470	-	520	ns
		5Mbit/s; ($t_{bit(TXD)}$=200ns)	170	-	220	ns
		8Mbit/s; ($t_{bit(TXD)}$=125ns)	95		145	ns
TXD dominant time-out time						
TXD dominant time-out time	$t_{to(dom)TXD}$	V_{TXD}=0V; Normal mode	0.8	-	9	ms
Bus wake-up times; pins CANH and CANL; Figure 12.						
Bus dominant wake-up filter time	$t_{fitr\_wake(busdom)}$	Standby mode	0.5	-	1.8	µs
Bus recessive wake-up filter time	$t_{fitr\_wake(busrec)}$	Standby mode	0.5	-	1.8	µs
Bus wake-up time-out time	$t_{to(wake)bus}$	Standby mode	0.8	-	9	ms
Mode transitions						
Mode change transition time	$t_{t(moch)}$		-	-	50	µs
Start-up time	$t_{startup}$		-	-	1.5	ms
RXD start-up time	$t_{startup(RXD)}$	to Standby mode after wake-up	4	-	50	µs
Pin STB; IO filter						
IO filter time	$t_{filter(IO)}$		1		8	µs
Undervoltage detection						
Undervoltage detection time	$t_{det(uv)}$	On pin VCC	-	-	50	µs
Switch-off undervoltage detection time	$t_{uvdt(swoff)}$	On pin VCC; SIT1462Q	-	-	50	µs
		On pin VIO; SIT1462Q/3	-	-	50	µs
Undervoltage recovery time	$t_{rec(uv)}$	On pin VCC	-	-	50	µs

(1) V_{IO} only in SIT1462Q/3 version.

(2) Guaranteed by design; not tested in production.

TEST CIRCUIT

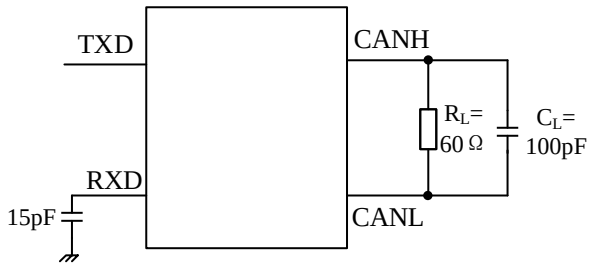


Figure 1 CAN transceiver timing test circuit

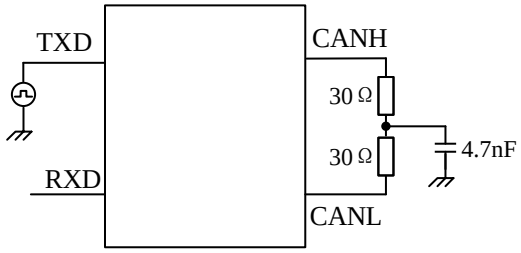


Figure 2 Test circuit for measuring transceiver driver symmetry

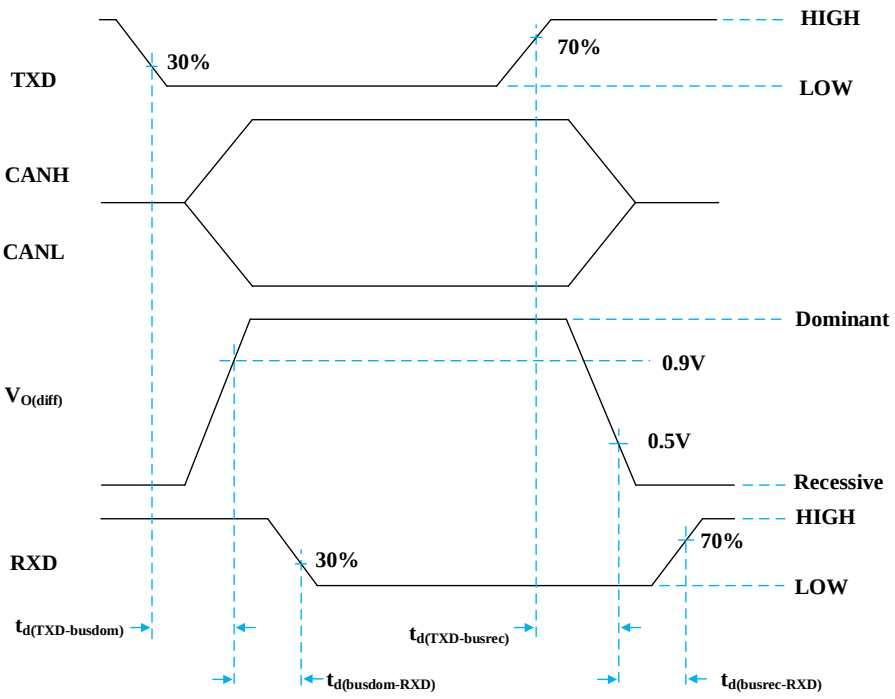


Figure 3 CAN transceiver timing diagram

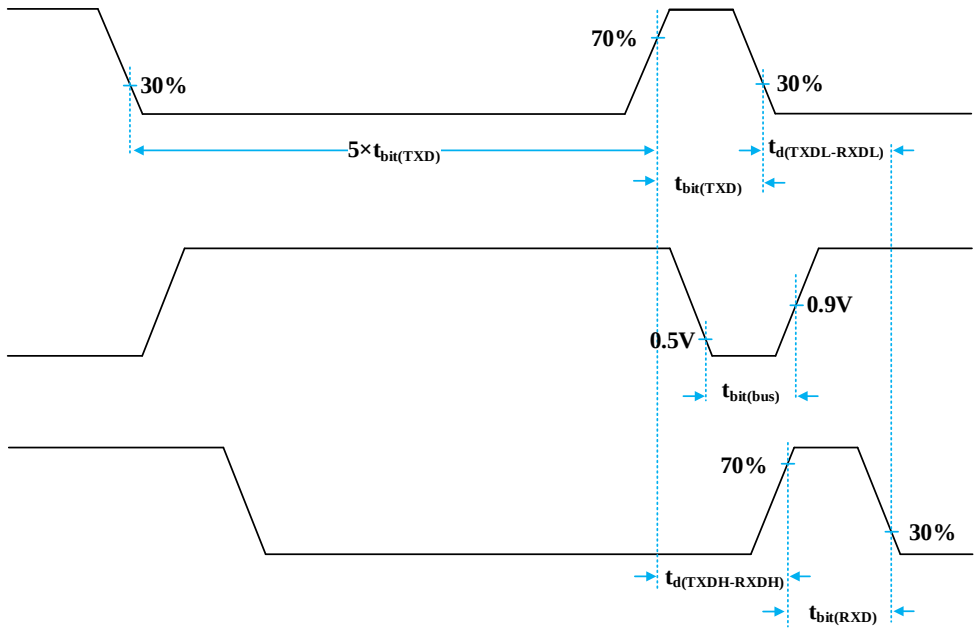


Figure 4 CAN FD timing definitions according to ISO 11898-2:2016

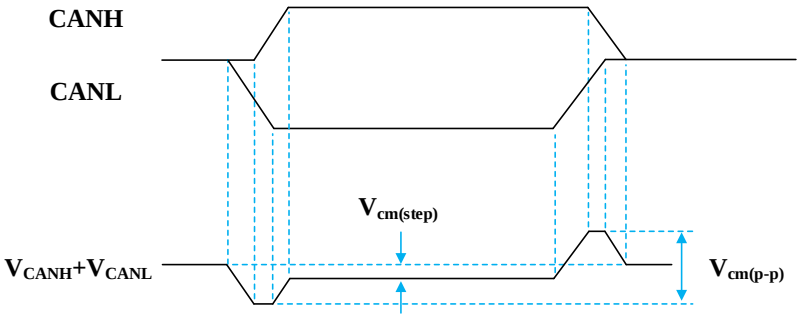


Figure 5 CAN bus common-mode voltage according to SAE 1939-14

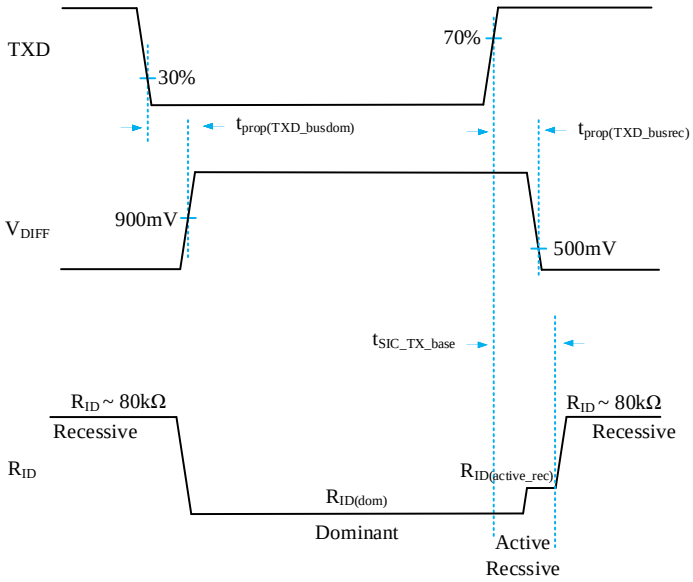
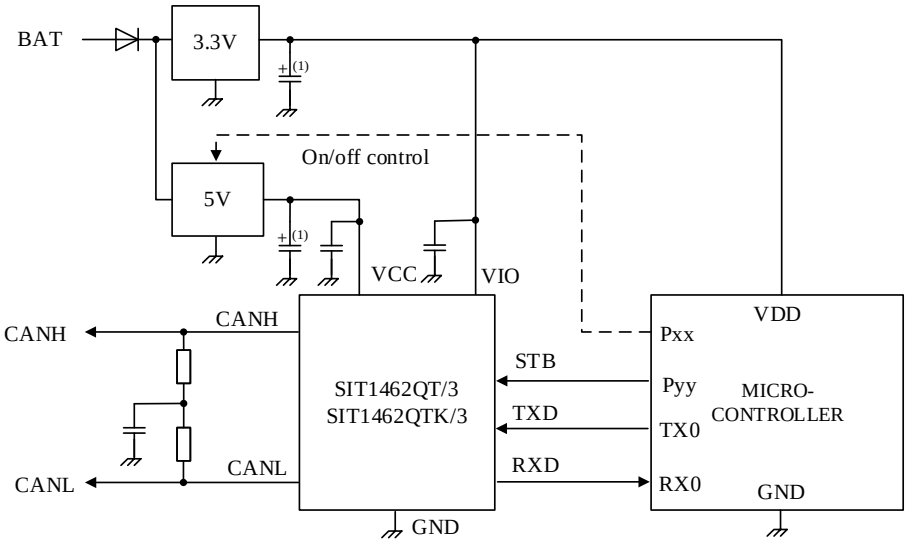


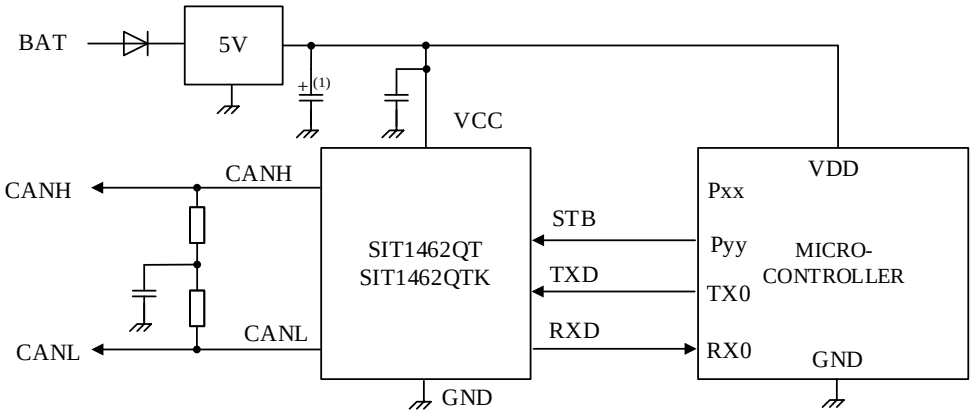
Figure 6 transmitter impedance and timing diagram for dominant-to-passive recessive transition

APPLICATION INFORMATION



(1) Optional, depends on regulator.

Figure 7 Typical SIT1462Q/3 application with a 3.3V microcontroller



(1) Optional, depends on regulator.

Figure 8 Typical SIT1462Q application with a 5V microcontroller

ADDITIONAL DESCRIPTION

1 Sketch

SIT1462Q is an interface chip applied between CAN protocol controller and physical bus, features a much tighter bit timing symmetry performance to enable CAN FD communication up to 8 Mbit/s, and has the capability of differential signal transmission between bus and CAN protocol controller. SIT1462Q includes CAN Signal Improvement Capability (SIC), as defined in CiA 601-4. CAN signal improvement significantly reduces signal ringing in a network, allowing reliable CAN FD communication to function in larger topologies. In addition, SIT1462Q features a much tighter number of nodes and stub topologies.

2 Overtemperature protection

The device is protected against overtemperature conditions. If the junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the CAN bus drivers are disabled. When the junction temperature drops below $T_{j(sd)rel}$, the CAN bus drivers recover once TXD has been reset to HIGH and Normal mode is selected (waiting for TXD to go HIGH prevents output driver oscillation due to small variations in temperature).

3 Undervoltage protection

If VCC drops below the standby undervoltage detection threshold ($V_{uvd(stb)(VCC)}$) for $t_{det(uv)}$, the transceiver switches to Standby mode. The logic state of pin STB is ignored until VCC has recovered.
In the SIT1462Q/3, if VIO drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)(VIO)}$) for $t_{uvd(swoff)}$, the transceiver switches to Off mode and disengages from the bus (high-ohmic) until VIO has recovered.
In the SIT1462Q, if VCC drops below the switch-off undervoltage detection threshold ($V_{uvd(swoff)(VCC)}$) for $t_{uvd(swoff)}$, the transceiver switches to Off mode and disengages from the bus (high-ohmic) until VCC has recovered.

4 Operating modes

SIT1462Q supports three operating modes, Normal, Standby and Off. The operating mode is selected via pin STB. The following table shows the corresponding mode status.

Mode	Inputs		Outputs	
	STB	TXD	CAN driver	RXD
Normal	LOW	LOW	Dominant	LOW
		HIGH	Recessive	LOW when bus dominant
				HIGH when bus recessive
Standby	HIGH	X	Biased to ground	Follows BUS when wake-up detected
				HIGH when no wake-up detected
Off (1)	X	X	High-ohmic state	High-ohmic state

(1) Off mode is entered when the voltage on pin VIO or pin VCC is below the switch-off undervoltage detection threshold.

4.1 Off mode

The SIT1462Q switches to Off mode from any mode when the supply voltage falls below the switch-off undervoltage threshold $V_{uvd(swoff)}$.
In Off mode, the pins CAN and RXD are in a high-ohmic state.

4.2 Standby mode

When the supply voltage rises above the switch-off undervoltage detection threshold, the SIT1462Q starts to boot up, triggering an initialization procedure. The SIT1462Q switches to the selected mode after t_{starup}.
Standby mode is selected when pin STB goes HIGH. In this mode, the transceiver is unable to transmit or receive data and a low-power receiver is activated to monitor the bus for a wake-up pattern. The transmitter and Normal-mode receiver blocks are switched off and the bus pins are biased to ground to minimize system supply current. Pin RXD follows the bus after a wake-up request has been detected.
A transition to Normal mode is triggered when STB is forced LOW.
If the supply voltage is below the Standby undervoltage hysteresis voltage $V_{uvd(stb)}$ when STB goes LOW, the SIT1462Q will remain in Standby mode.
Pending wake-up events will be cleared and differential data on the bus pins converted to digital data via the low-power receiver and output on pin RXD.
In the SIT1462Q/3, the low-power receiver is supplied from V_{IO} and can detect CAN bus activity when V_{IO} is above switch-off undervoltage detection voltage $V_{uvd(swoff)}$ (even if V_{IO} is the only available supply voltage).

4.3 Normal mode

A LOW level on pin STB selects Normal mode, provided the supply voltage on pin VCC is above the standby undervoltage detection threshold, $V_{uvd(std)}$.
In this mode, the transceiver can transmit and receive data via bus lines CANH and CANL. Pin TXD must be HIGH at least once in Normal Mode before transmission can begin. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines into digital data on pin RXD. The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

4.4 Operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in Figure 11 and in the state diagrams (Figure 9 and Figure 10)

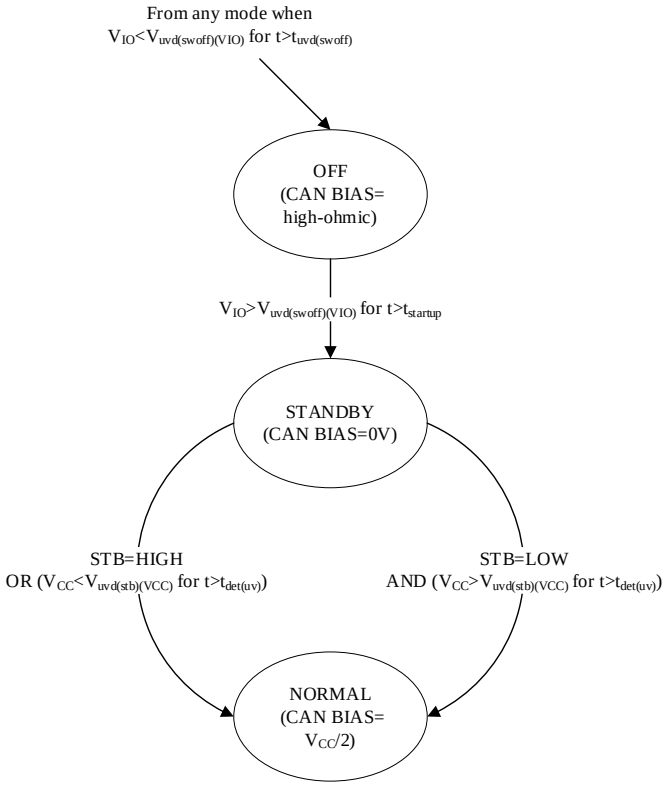


Figure 9 SIT1462Q/3 state diagram

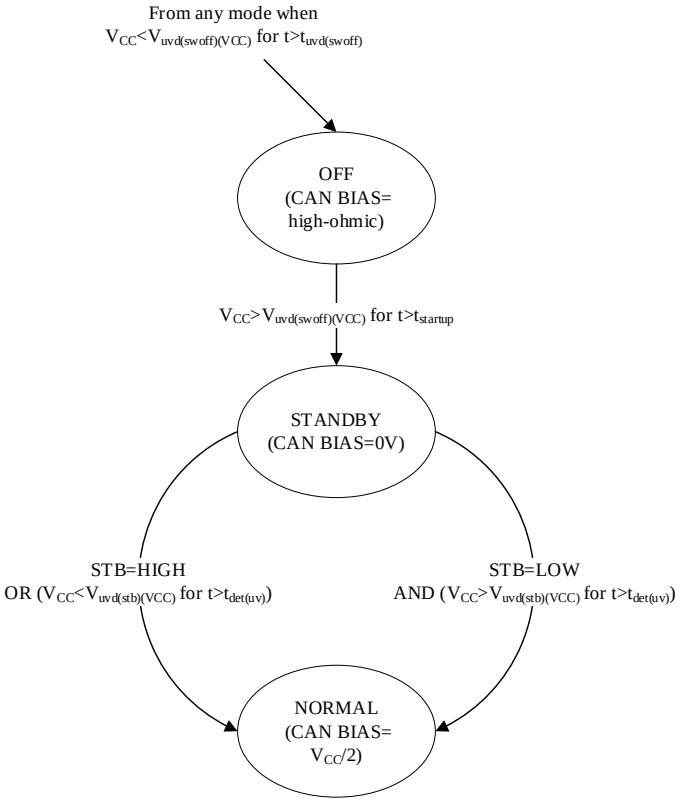


Figure 10 SIT1462Q state diagram

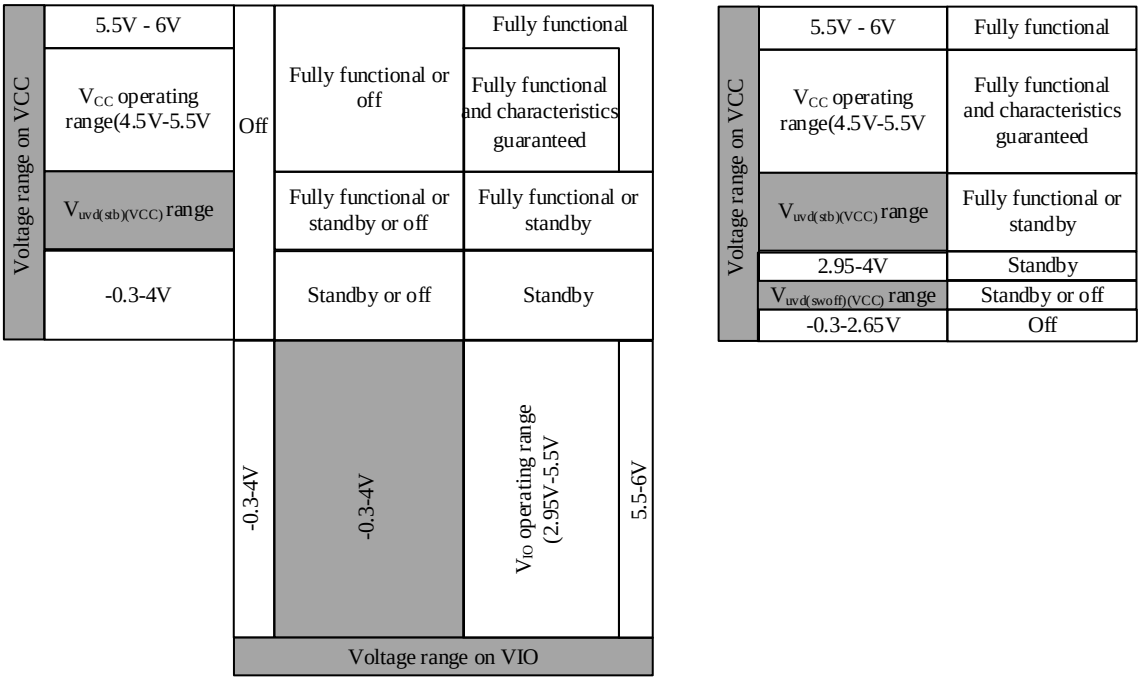


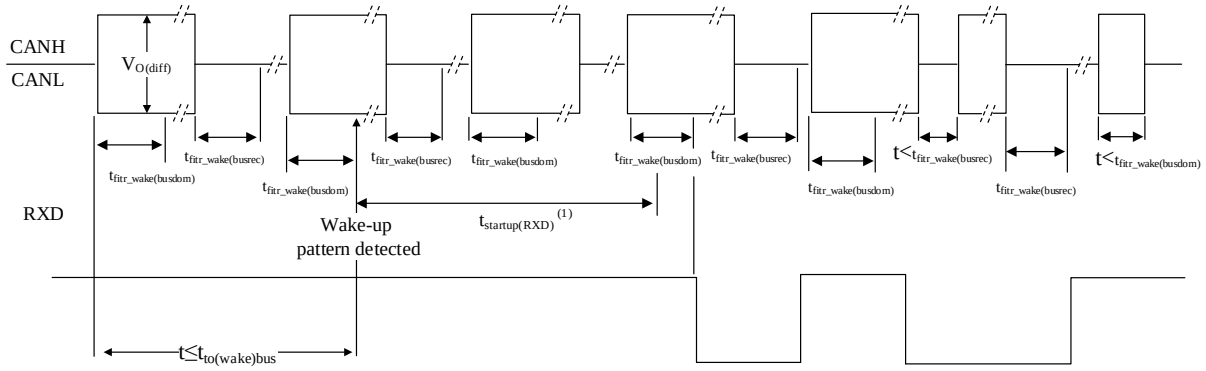
Figure 11 Supply voltage ranges and gap-free operation

5 Dominant timeout function

A "TXD dominant time-out" timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD goes HIGH.

6 Remote wake-up

SIT1462Q wakes up from Standby mode when dedicated wake-up pattern is detected on the bus. Wake-up timing is shown in the Figure 12。



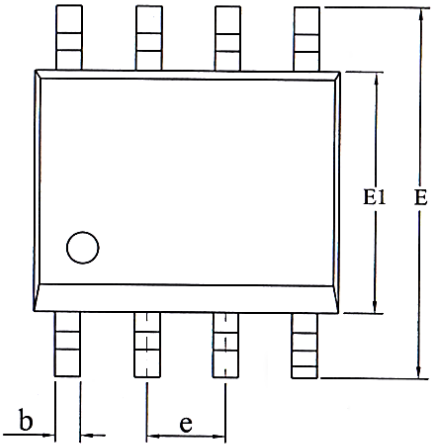
(1) During $t_{startup(RXD)}$, the low-power receiver is on but pin RXD is not active (i.e. HIGH/recessive). The first dominant pulse of width ≥ $t_{filr\_(wake)bus}$ that ends after $t_{startup(RXD)}$ will trigger RXD to go LOW/dominant.

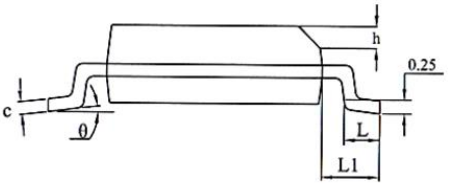
Figure 12 Wake-up timing

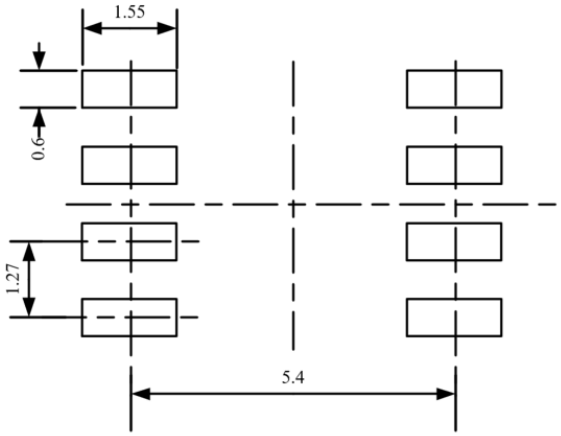
SOP8 DIMENSIONS

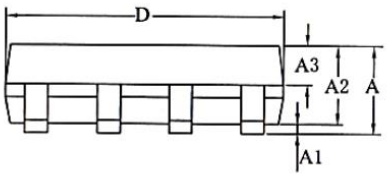
package size

Symbol	Min./mm	Typ./mm	Max./mm
A	-	-	1.75
A1	0.10	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.47
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.50	-	0.80
L1	1.05REF		
c	0.20	-	0.24
θ	0°	-	8°







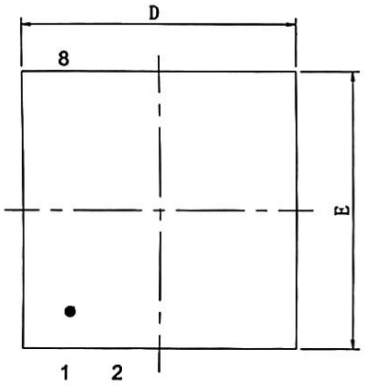


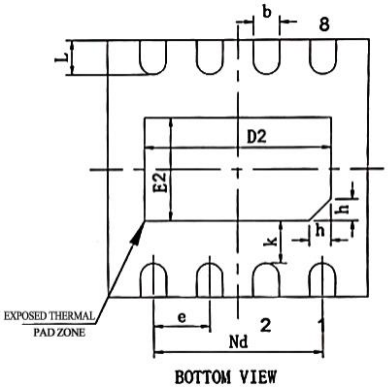
LAND PATTERN EXAMPLE (Unit: mm)

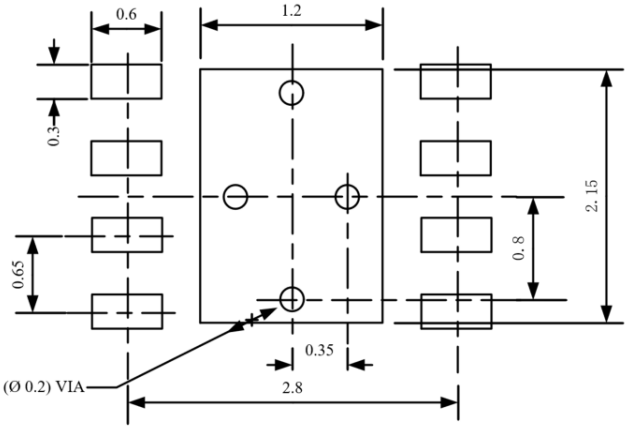
DFN3*3-8 DIMENSIONS

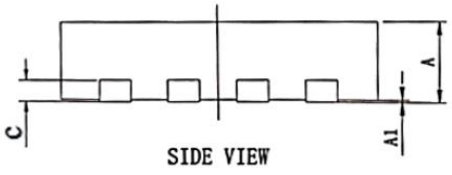
Package size

Symbol	Min./mm	Typ./mm	Max./mm
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	2.05	2.15	2.25
Nd	1.95BSC		
E2	1.10	1.20	1.30
b	0.25	0.30	0.35
e	0.65BSC		
k	0.50REF		
L	0.35	0.40	0.45
h	0.20	0.25	0.30



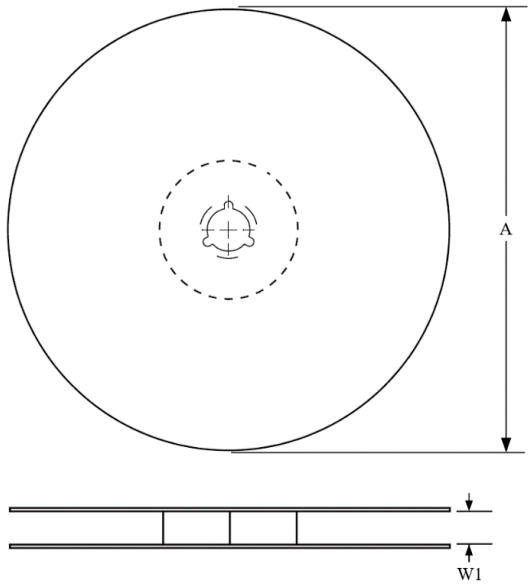




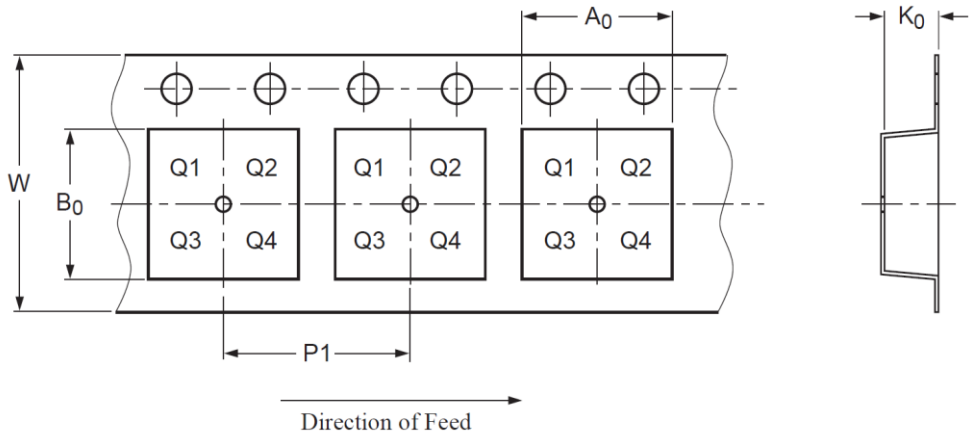


LAND PATTERN EXAMPLE (Unit: mm)

TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



PIN1 is in quadrant 1

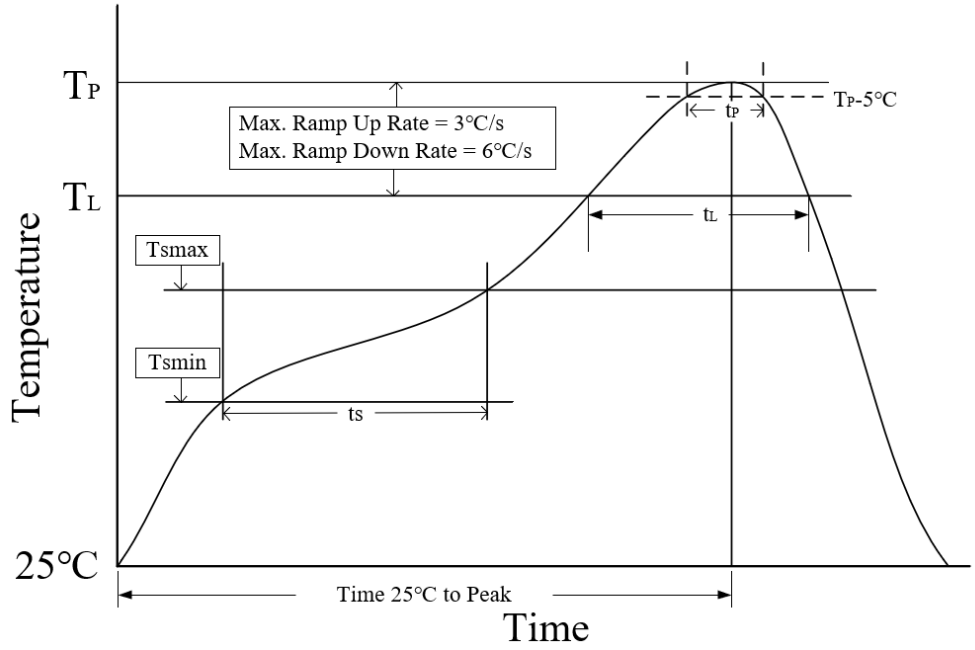
Package Type	Reel Diameter A (mm)	Tape Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
SOP8	330±1	12.4	6.60±0.1	5.30±0.10	1.90±0.1	8.00±0.1	12.00±0.1
DFN3*3-8	329±1	12.4	3.30±0.1	3.30±0.1	1.10±0.1	8.00±0.1	12.00±0.3

ORDERING INFORMATION

Type number	Package	Packing
SIT1462QT/3	SOP8	Tape and reel
SIT1462QT	SOP8	Tape and reel
SIT1462QTK/3	DFN3*3-8	Tape and reel
SIT1462QTK	DFN3*3-8	Tape and reel

SOP8 is packed with 2500 pieces/disc in braided packaging; Leadless DFN3*3-8 is packed with 6000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5 °C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25°C to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	September 2024