SIV121C

1/11-INCH VGA CMOS IMAGE SENSOR

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SETi Co., Ltd.

DATA SHEET

SIV121C : 1/11-inch VGA CMOS Image Sensor

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Contents

1. Overview

1.1. General Description

The SIV121C features 640H x 480V resolution with 1/11-inch optical format, and 4-transistor pixel structure for high image quality and low noise variations. It delivers superior image quality by on-chip design of a 10-bit ADC and embedded image signal processor.

The SIV121C performs a huge range of on-chip image processing functions of auto exposure (AE), auto white balance(AWB), black level compensation (BLC), false color correction, gamma correction, color correction, lens shading correction, and so on.

It incorporates on-chip camera functions of sub-sampling and windowing that generates such various output size formats as VGA, QVGA, QQVGA, CIF, QCIF and QQCIF. Output data formats as YUV/YCbCr422, RGB565, and 8bit RGB Bayer formats. Those advanced features including X/Y image flip and image effects can be easily controlled and programmed through a simple I2C interface.

1.2. Features

- 0.13um CMOS Process Technology
- Micro-lens for High Sensitivity and RGB Mosaic Color Filter Array
- Column Parallel 10bit A/D conversion
- Internal LDO voltage regulator.
- Power Sleep (Idle) and Power Down(Standby) Mode for Power Saving
- VGA / QVGA / QQVGA / CIF / QCIF / QQCIF Sub-sampling Mode, HV Half Binning Mode, and programmable User Window Size.
- YUV/YCbCr422, RGB565, and 8bit RGB Bayer Output Data Formats
- Power Supply Voltage: 2.65V~2.9V for Analog, 1.7V~2.9V for Digital I/O, and internal LDO power for Digital Core
- I2C Serial Programming Interface
- Progressive Scan Mode and Electronic Rolling Shutter
- Integrated On-chip Image Signal Processing
  - Automatic Exposure (AE)
  - Automatic White Balance (AWB)
  - Automatic Gain Control (AGC)
  - Black Level Compensation (BLC)
  - Color Interpolation
  - False Color Correction
  - Lens Shading Correction
  - FPN, and Random Noise Cancellation
  - Gamma Correction
  - Color Matrix and Color Space Conversion
  - Hue, Sharpness, Brightness, Contrast Stretch, and Color Saturation Control
  - Image Effects: Sepia, Mono, Inverted Mono, YCbCr Inversion, embossing, and sketch
  - Image X Flip (mirror) and Y Flip

1.3. Key Specifications

Table 1. Key specifications

Parameter		Typical Value
Optical Format		1/11-inch
Pixel Size		2.2um x 2.2um
Image Area		1443.2 um (H) x 1091.2 um (V), 1809.3 um Diagonal
Video Format		640H x 480V
Effective Pixel Array		656H x 496V
Total Pixel Array		672H x 534V
Output Data Format		YUV/YCbCr422, RGB565 and 8bit RGB Bayer
Output Display Format		VGA(640x480), QVGA(320x240), QQVGA(160x120) CIF(352x288), QCIF(176x144), QQCIF(88x72) and User Define Window
ADC Resolution		10bit ADC
Sensitivity		0.71 V/Lux *sec
Maximum Frame Rate		30fps @ VGA, 24MHz MCLK
Maximum Master Clock		27MHz
Operating Temperature		-20 ~ 60 ℃
Dynamic Range		60 dB
SNR		37 dB
Dark Signal		5 mV/sec@60℃
Supply Voltage	Core	1.5V
	Analog	2.8 V
	I/O	1.8V / 2.8V
Power Consumption		79 mW @ 24 MHz, 30 fps 60 uA @ Stand-by
Package-Type		Die, NeoPAC

1.4. Block Diagram

Figure 1. Block diagram

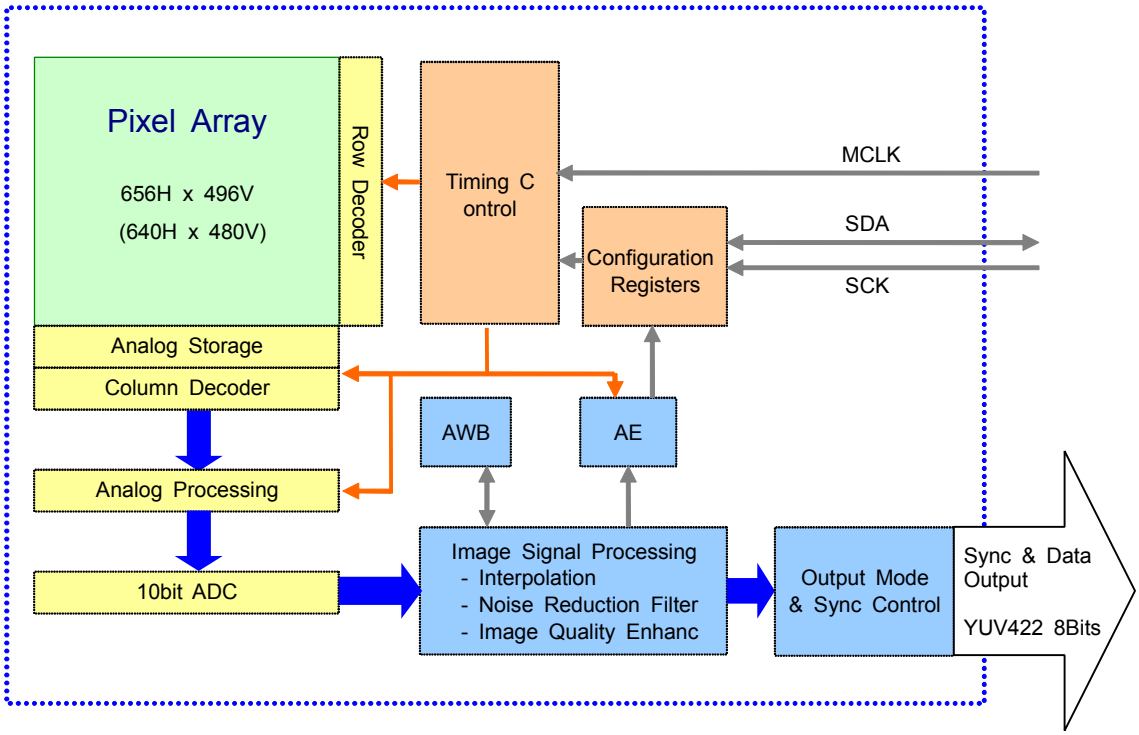
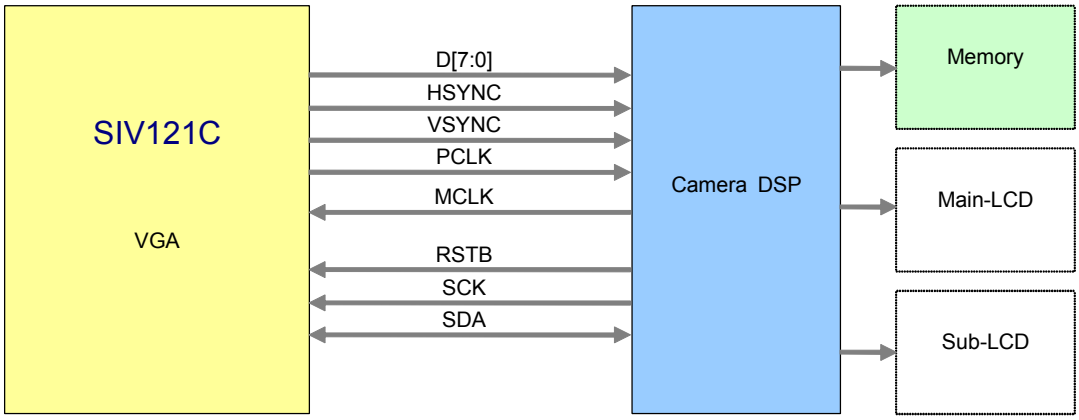


Figure 2. System interface



2. Chip Information

2.1. Pin Descriptions

Table 2. Pin description

Pin No.	Pin Name	Pin Description	Pin Type
1	VSSC/O	Digital Core / IO Ground	GND
2	VDDO	Digital I/O Power (1.8V / 2.8V)	1.8V/2.8V
3	D[1]	Data Out[1]	Tri-Output
4	PCLK	Output Pixel Data Synchronous Clock	Tri-Output
5	D[2]	Data Out[2]	Tri-Output
6	D[3]	Data Out[3]	Tri-Output
7	D[0]	Data Out[0]	Tri-Output
8	RSTB	Sensor Chip Reset. (Active Low)	Input
9	MCLK	System Master Clock	Input
10	VDD	Digital Core Power (1.5V)	1.5V
11	VDDA	Analog Power (2.8V)	2.8V
12	VSSA	Analog Ground	GND
13	SDA	Serial Bus Data	Bi-Directional
14	SCK	Serial Bus Clock	Input
15	VSYNC	Frame Synchronous Signal	Tri-Output
16	HSYNC	Horizontal Synchronization	Tri-Output
17	D[7]	Data Out[7]	Tri-Output
18	D[6]	Data Out[6]	Tri-Output
19	D[5]	Data Out[5]	Tri-Output
20	D[4]	Data Out[4]	Tri-Output

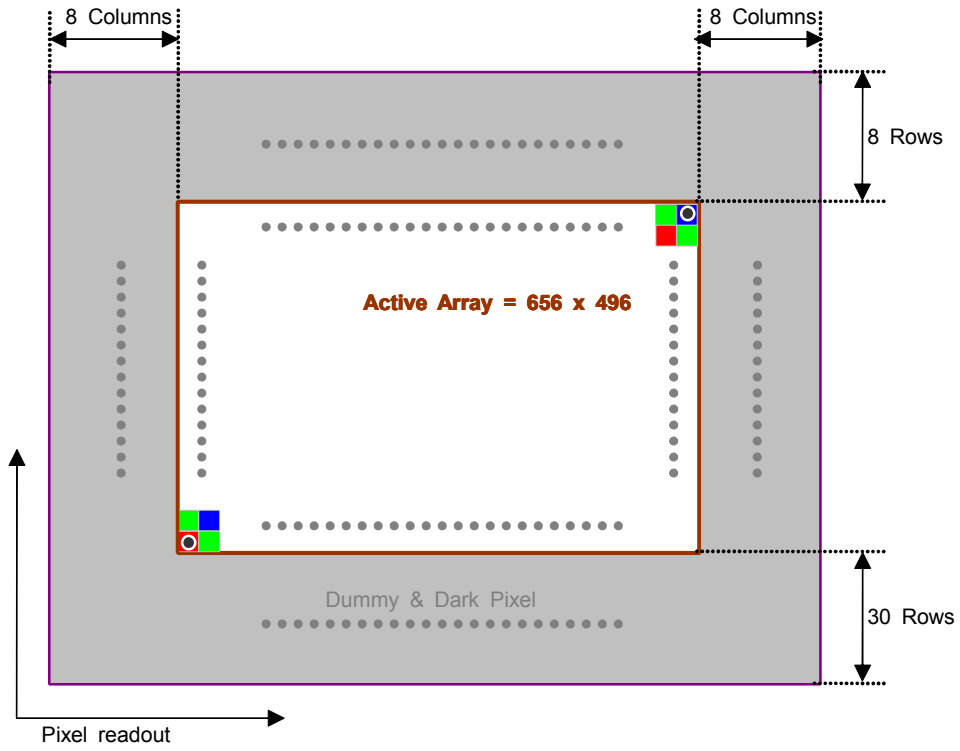
2.2. Pixel Array Information

The sensor core pixel array is configured as 672 columns by 534 rows. And physical active pixel array is configured as 656 columns by 496 rows. In default mode, a VGA full image is generated, starting at red pixel of column 8, row 30.

Table 3. Pixel coordinates

Video format	Window size	Pixel coordinates	Remark
Total sensor array	672H x 534V	(0,0) ~ (671,533)	Dummy & dark pixels
VGA	656H x 496V	(8,30) ~ (663,525)	Physical array size

Figure 3. Pixel array structure



2.3. I2C Control

The internal registers of the sensor are programmable through I2C serial bus interface that has SDA (Serial Bus Data, Bi-directional) and SCK (Serial Bus Clock, Input) pins and can be used to write and read the required data into.

The I2C 7-bit slave device address of the sensor is 0x33 (0110011b). Therefore it can be actually programmed by R/W operations into the 0x67 / 0x66 addresses. In SIV121C, 1-byte I2C serial interface is used. (I.e. 1-byte address & data transmission)

2.4. Pixel Clock Information

The PCLK (pixel clock) that is the pixel operation clock for internal circuit is mostly used for the internal operation, and timing controls like a frame timing control, integration timing control, and so on. The CLK_DIV function of the CNTR_B register (BANK[0x01], REG[0x04]) can define the PCLK frequency as follows.

The PCLK that is the pixel output clock for external circuit to synchronize data lines differs accordingly to the display modes and video output formats.

Table 4. PCLK by CLK_DIV (BANK[0x01],REG[0x04])

CLK_DIV[1:0]		PCLK
B3	B2	
0	0	1/2 MCLK Frequency
0	1	1/4 MCLK Frequency
1	0	1/8 MCLK Frequency
1	1	1/16 MCLK Frequency

Table 5. PCLK change for different display mode and format

Video Display Mode	PCLK	
	Bayer	YCbCr
VGA	PCLK	2 PCLK
QVGA	1/2 PCLK	PCLK
QQVGA	1/4 PCLK	1/2 PCLK
CIF	PCLK	2 PCLK
QCIF	1/2 PCLK	PCLK
QQCIF	1/4 PCLK	1/2 PCLK

2.5. Electrical Specifications

2.5.1. Absolute maximum ratings

Table 6. Absolute maximum ratings.

Symbol	Parameter	Rating	Unit
V_{DDO}	DC supply voltage for I/O	-0.3 ~ 2.9	V
V_{DDA}	AC supply voltage for analog	-0.3 ~ 2.9	V
V_{IN}	DC input voltage	-0.3 ~ VDD + 0.3	V
V_{OUT}	DC output voltage	-0.3 ~ VDD + 0.3	V
T_{OPP}	Operating temperature(Performance guaranteed)	-20 ~ 50	ºC
T_{OPF}	Operating temperature(Chip function guaranteed)	-20 ~ 60	ºC
T_{STG}	Storage temperature	-30 ~ 85	ºC

*Note that the image quality even within the operation temperature can be getting worse under the brightness conditi on lower than 100Lux.

2.5.2. DC Electrical Specification

Table 7. DC Electrical Characteristics & operating conditio ns

Conditions: TA = 25 ºC unless otherwise specifie d.

Symbol	Parameter	Condition	Min.	Typical	Max.	Unit
V_{DDO}	DC supply voltage for I/O		1.7	-	2.9	V
V_{DDA}	AC supply voltage for analog		2.65	2.8	2.9	V
V_{IH}	Input high voltage	CMOS	0.7VDD			V
V_{IL}	Input low voltage				0.3VDD	V
V_{OH}	Output high voltage	I_{OH}=4mA	0.8VDD			V
V_{OL}	Output low voltage	I_{OL}=4mA			0.2VDD	V
I_{IH}	Input leakage current	V_{IN}=VDD			1	uA
I_{IL}	Input leakage current	V_{IN} = GND			1	uA
I_{OZ}	3-state output leakage current				1	uA
P_{AVG}	Power dissipation	VDDA=2.8V VDDO=2.8V		79		mW
P_{STBY}	Standby current			60		uA

*Note that the V_{DDO}, V_{DDC}, V_{DDA} beyond the limits of here above spec can make the image quality deteriorated.

2.5.3. AC Electrical Specification

Figure 4. Data output timing (default setting)

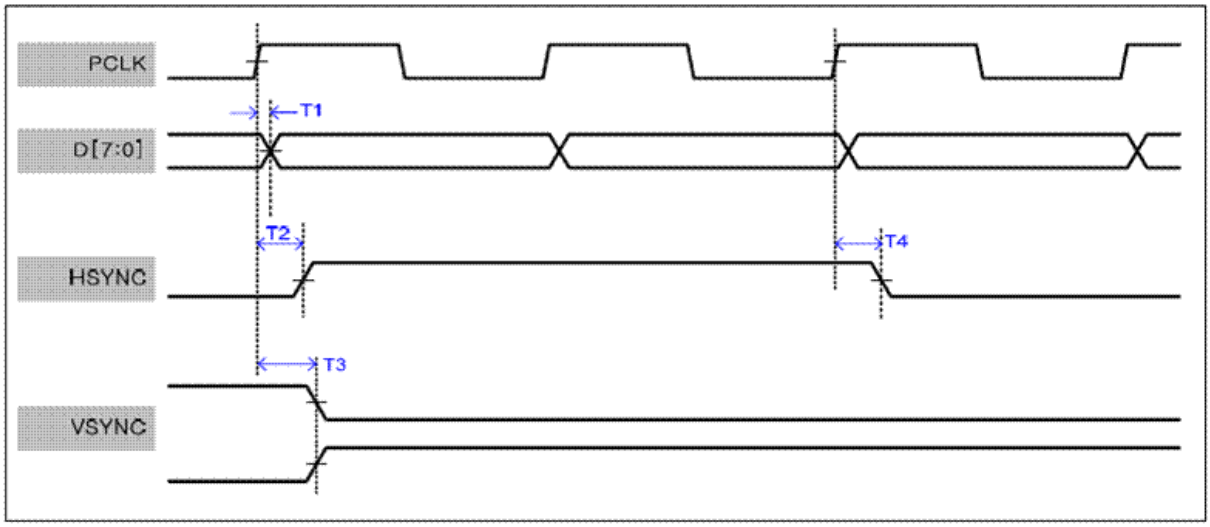


Table 8. AC Characteristics

Parameter	Symbol	Condition	Min	Typical	Max	Unit
System Master clock frequency	f_{MCLK}	Duty = 50 %	12	24	48	MHz
Pixel clock frequency	f_{PCLK}	Duty = 40 ~ 60% @30fps	-	24	-	MHz
Propagation delay time from pixel clock	T3	VSYNC output	-	-	10	ns
	T2	HSYNC output	-	-	10	ns
	T1	D[7:0] output	-	-	10	ns
HSYNC hold time from pixel clock	T4	HSYNC output	-	-	10	ns

(Output loading = 30pF)

2.6. Power Sequence

2.6.1. Power-On Sequence

1) RSTB to Low-level. (default)
2) After Supplying Supply VDDO & VDDA
3) Supply the MCLK.
4) RSTB to High-level (Minimum 10 MCLKs)
5) Set the register through the serial bus SCK/SDA activa ted by host.
   (I2C Device Address: Write (0x66) / Read (0x67))

2.6.2. Power-Off Sequence

1) RSTB to Low-level.
2) MCLK off
3) Power off (VDDO, & VDDA)

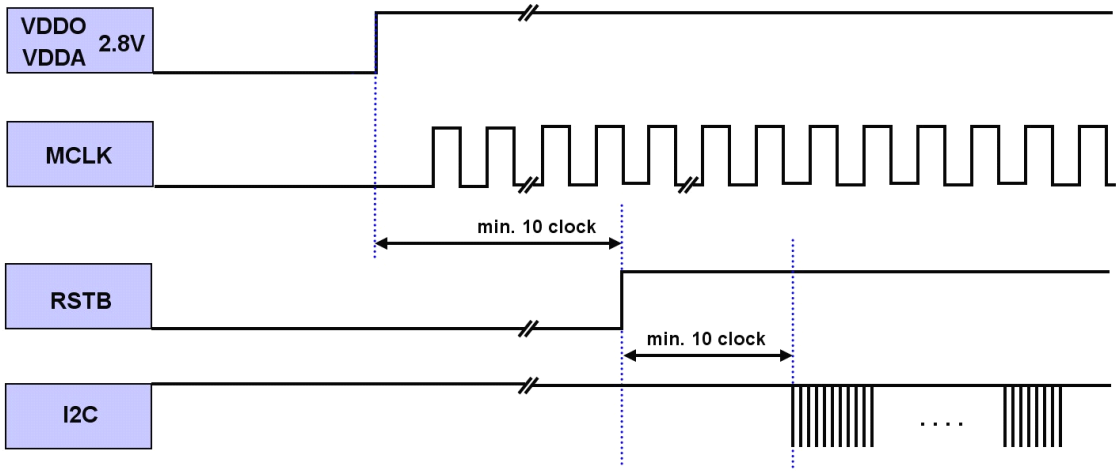


Figure 5. Power-On sequence.

2.7. Standby Sequence

The input MCLK, VDDO and VDDA don't have specific effects on the standby mode (power down mode) operation. When the standby mode, all internal digital and analog blocks go into an inactive mode except I2C. Along with this, the power consumption is reduced considerably. SIV121C has only 1-type standby mode. That is software standby (I2C controlled standby) mode as below.

2.7.1. Software Standby (I2C Controlled Standby)

When the CHIP_CNTR register bit "1" is enabled (BANK[0x00], REG[0x03]=0x02), I2C standby mode can be activated.

In this software standby state,

1) I2C operation is available.
2) Output pads are in HI-Z state.
3) Chip goes into power-down mode.
4) Internal registers hold current value

2.8. Reference Circuit

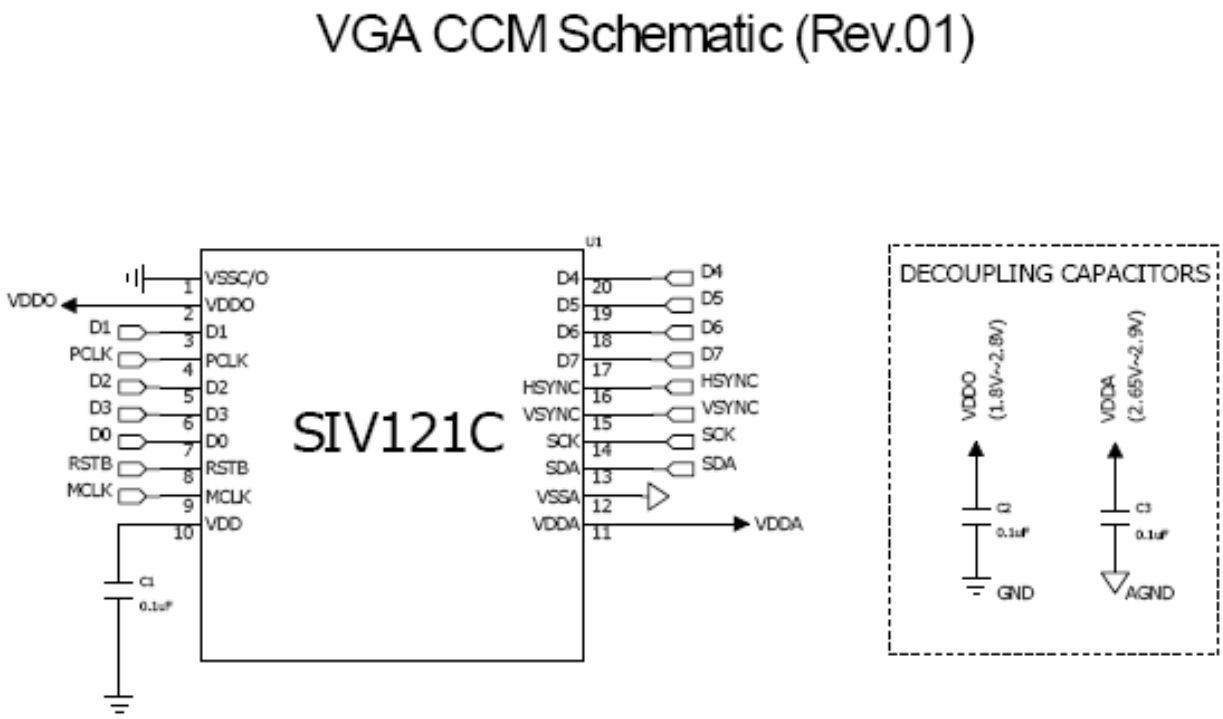


Figure 6. SIV121C reference circuit

! NOTE: This schematic is the reference circuit for campact camera image sensor module.

- VDD(Core Voltage) is supplied from the internal LDO of SIV121C.
- VDD must be connected to the chip with decoupling capacitors as close as possible.
- If VSSA, VSSO and VSSC should be merged, the common line pattern should have enough wide as can as possible.
- SCK and SDA must be connected with pull-up resistors to the system.
  Resistor values depend on the applied system.
- RSTB must not be shared with other devices.
- RSTB (Sensor Reset) : High - Normal operation / Low - Reset

3. Functional Description

3.1. Frame Timing Information

A frame size including horizontal and vertical blanking, valid image data is synchronized with the PCLK. The amount of horizontal and vertical blanking is achieved by programming the bits in corresponding registers as described here below.

Table 9. Frame timing related registers (BANK[0x01])

Register Name	Addr	Description
BNKT	0x20	Frame timing register
HBNKT	0x21	Frame timing register
VBNKT	0x22	Frame timing register
SCAN	0x23	Frame timing register
ROWFILL	0x24	Frame timing register

Timing @ VGA mode

Horizontal Blank Time:

HBNKT[11:0]

={BNKT[7:4],HBNKT[7:0] }

1 Row Time

= (Display Width (HDT) + [Scan Time (Optional) +1]+ [Horizontal Blank Time(HBT)+1]+[ROWFIL(HFT)+1]) * PCLKs

Vertical Blank Time:

= VBNKT[11:0] + 1 Rows

VBNKT [11:0]

= { BNKT[3:0], VBNKT[7:0] }

1	1	1	1	1	1	1	1	7.97

3.2. Gain

The gain can either be programmed by the user or controlled by the internal AGC (automatic gain control circuit). Raw R, G, B Bayer data are amplified to compensate the output levels by the GAIN factor.

The GAIN value automatically varies with the pixel integration time when AE (auto exposure) function works upon the luminance level of the light source. The GAIN register controls a coarse gain level and fine gain level. Each CGAIN (Coarse Gain) and FGAIN (Fine Gain) functions make analog gain levels and digital gain variously controllable.

The manual changes of the gain values may possibly cause to lose image quality, so vendor-recommended register values are highly preferable.

GAIN = $2^{CGAIN[1:0]}$ x (FGAIN[7:0] / 32)

Max Value = 64x

(Max Gain by the internal AGC = 32x)

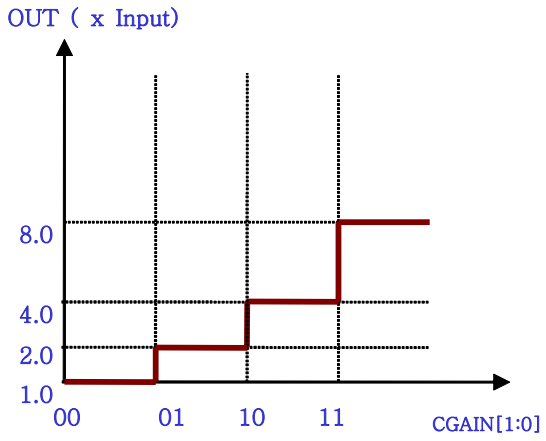


Figure 7. CGAIN OUT

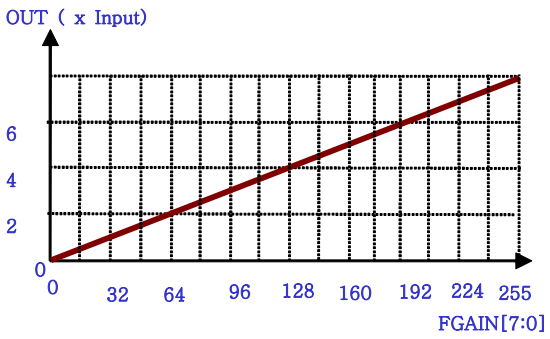


Figure 8. FGAIN OUT

Table 10. Coarse GAIN output (BANK [0x02], REG[0x32])

CGAIN[1:0]		Coarse GAIN output
D1	D0	
0	0	x1
0	1	x2
1	0	x4
1	1	x8

Table 11. Fine GAIN output (BANK [0x02], REG[0x33])

FGAIN[7:0]								Fine GAIN output
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0.5
0	0	1	0	0	0	0	0	1
0	0	1	1	0	0	0	0	1.5
0	1	0	0	0	0	0	0	2
0	1	0	1	0	0	0	0	2.5
1	0	0	0	0	0	0	0	4

3.3. Video Output Format

Pixel array has Bayer mosaic color filters, and each pixel has only one type of color filter on it. As it is necessary to get all of RGB color components to assert a full color for a pixel, missed data must be inferred from color data of other pixels by color interpolation. Since human eyes are less sensitive to color variations than luminance, each color component can be sub-sampled to reduce the amount of data to be transmitted, but almost preserve the same image quality.

Each pixel consists of two data of Y, Cr or Y, Cb and its data output order can be programmed by setting OUTFMT[5:4] register, in the 8-bit YCbCr422 output format as shown below.

Table 12. YCbCr422 output (BANK [0x04], REG[0x12])

OUTFMT[5:4]	Output order	Remark
00	Cr Y Cb Y	C First & Cr First
01	Cb Y Cr Y	C First & Cb First
10	Y Cr Y Cb	Y First & Cr First
11	Y Cb Y Cr	Y First & Cb First

3.4. Video Output Size

The VMODE registers are accessible to set a variety of the display image sizes as below. These display video sizes are deeply related to their data output format.

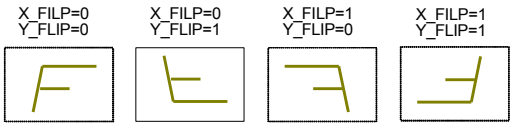
Table 13. Video output size (BANK[0x01], REG[0x06]).

VMODE[2:0]			Video format	Video Output Size
D2	D1	D0		
0	1	1	QQCIF	88 x 72
0	1	0	QCIF	176 x 144
0	0	0	CIF	352 x 288
1	0	0	QQVGA	160 x 120
1	0	1	QVGA	320 x 240
1	1	0	VGA	640 x 480

3.5. X/Y Flip Control

The pixel data are read out from left to right in horizontal direction and from bottom to top in vertical direction normally. By changing the mirror mode, the read-out sequence can be reversed and the resulting image can be top in vertical mirror mode. The horizontal and vertical mirror mode can be programmed by X/Y-flip control register, CNTR_B[1:0] (BANK[0x01], REG[0x04]). During mirrored readout, the region of active pixels used to generate the Y-flip mirrored image is offset by 1 upper row in horizontal direction so that the readout always starts on the same color pixel.

Figure 9. X/Y flip setting



3.6. Color Matrix

In general, the color specifications of the image sensor differ from the fabrication process like color filter, design or something. The color matrix adjusts these unsuitable color specifications unlike the actual color of the subject.

The color matrix of the chip is designed to work deeply interconnected to the color space conversion. Thereby, the user surely takes its mutual relation into consideration to tune the color matrix.

The color matrix uses 3x3 color correction matrix shown below.

$$\begin{pmatrix} R_{out} \\ G_{out} \\ B_{out} \end{pmatrix} = \begin{pmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & C_{22} & C_{23} \\ C_{31} & C_{32} & C_{33} \end{pmatrix} \times \begin{pmatrix} R_{in} \\ G_{in} \\ B_{in} \end{pmatrix}$$

3.7. Color Space Conversion

The chip outputs RGB Bayer and YCbCr data by asserting the function which converts RGB color space to YCbCr. The equation from CCIR-601 is normally used for color space conversion and reverse conversion.

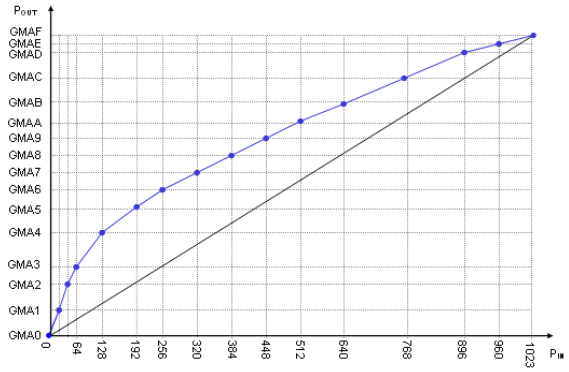
3.8. Color Interpolation

Each color bayer pixel from the image sensor is converted into R, G, and B pixels and the missing color information of a bayer pixel can be derived from average value of adjacent pixels. 5x5 interpolation window will be shifted by one pixel horizontally and vertically.

3.9. Gamma Correction

Gamma correction operates on R, G, and B pixels respectively to improve non-linear relation between the video signal and the display device output. Piecewise linear method is implemented. 16 piece linear seg-ments are supported and user-programmable.

Figure 10. Gamma graph.



3.10. Shading Correction

The circumstance area of pixel array does not have enough quantity of light due to optical character-istics of lens. It causes reduction of signal near peripheral of pixel array. The reduction of signal depends on both of pixel location and color.

Figure 11. Lens shading X&Y axis.

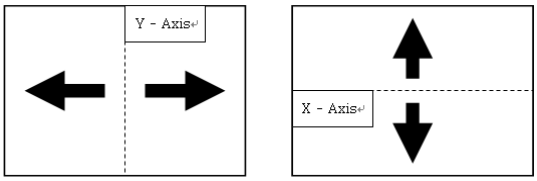
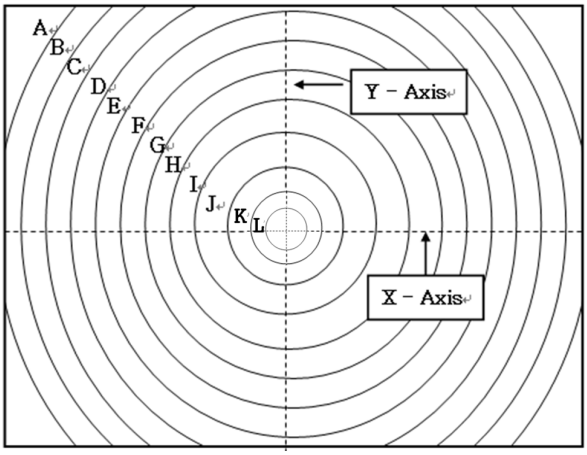


Figure 12. Lens shading area map.



3.11. Automatic Exposure (AE)

AE control algorithm tracks the change of the luminance of a frame image compared frame to frame and compares calculated luminous to the AE target value. The image brightness is adjusted by controlling analog gain , digital gain and shutter time of the pixel array. Luminous integrator filter makes stable image from fast luminous change environment. Also, AE algorithm of SIV121C has fast speed control that abnormal luminous change

3.12. Automatic White Balance (AWB)

In general, light source have unique color tempera- ture, which may distort the original color of the subject image input into the sensor. The AWB algorithm tracks the white color using the white pixel detection algorithm. This algorithm controls the AWB color gain (RGAIN, BGAIN), automatically.

4. Register Description

4.1. Register List

Table 14. Accessible register list

BANK [0x00]: PMU Block

Address	Name	Default	Mode	Address	Name	Default	Mode
0x00	BLK_SEL	0x00	R/W	0x03	CHIP_CNTR	0x02	R/W
0x01	ChipID	0x95	R	0x10	LDO_CNTR	0x02	R/W
0x02	INFO	0x10	R				

BANK [0x01]: Control Block

Address	Name	Default	Mode	Address	Name	Default	Mode
0x03	CNTR_A	0x02	R/W	0x20	BNKT	0x00	R/W
0x04	CNTR_B	0x00	R/W	0x21	HBNKT	0x65	R/W
0x06	VMODE	0x04	R/W	0x22	VBNKT	0x03	R/W
0x07	Reserved	-	-	0x23	SCAN	0x63	R/W
0x08	UPDATE_FLAG	0x00	W	0x24	ROWFILL	0x31	R/W
0x09~0x1F	Reserved	-	-	0x51	TEST51	0x00	R/W

BANK [0x02]: AE Block

Address	Name	Default	Mode	Address	Name	Default	Mode
0x10	AE_CNTR	0x80	R/W	0x40	G_MAX	0x45	R/W
0x11	MAX_SHUTSTEP	0x0F	R/W	0x42	G_TOP0	0x28	R/W
0x12	Y_TARGET_N	0x80	R/W	0x44	G_MIN0	0x08	R/W
0x13	Y_TARGET_CWF	0x80	R/W	0x45	G50_DEC	0x09	R/W
0x14	Y_TARGET_A	0x78	R/W	0x46	G33_DEC	0x17	R/W
0x16	LOCK_LEVEL	0x40	R/W	0x47	G25_DEC	0x1D	R/W
0x18	AEADCT	0x00	R/W	0x48	G20_DEC	0x21	R/W
0x19	DA2BR	0x8E	R/W	0x49	G12_DEC	0x23	R/W
0x1A	D2B_RET_TIME	0x06	R/W	0x4A	G09_DEC	0x24	R/W
0x1B	BR2DA	0x00	R/W	0x4B	G06_DEC	0x26	R/W
0x1C	Control register	-	-	0x4C	G03_DEC	0x27	R/W
0x1D	INI_SHUTTIME	0x01	R/W	0x4D	G100_INC	0x27	R/W
0x1E	INI_CGAIN	0x00	R/W	0x4E	G50_INC	0x1A	R/W
0x1F~0x22	Control register	-	-	0x4F	G33_INC	0x14	R/W
0x23~0x2e	Reserved	-	-	0x50	G25_INC	0x11	R/W
0x2F	Control register	-	-	0x51	G20_INC	0x0F	R/W
0x30	SHTH	0x00	R/W	0x52	G12_INC	0x0D	R/W
0x31	SHTL	0x7D	R/W	0x53	G09_INC	0x0C	R/W
0x32	CGAIN	0x00	R/W	0x54	G06_INC	0x0A	R/W
0x33	FGAIN	0x28	R/W	0x55	G03_INC	0x09	R/W
0x34	STST_P	0x7D	R/W	0x5F	WIN_CNT	0x00	R/W
0x35~0x3F	Reserved	-	-	0x56~0x86	Control register		

BANK [0x03]: AWB Block

Address	Name	Default	Mode	Address	Name	Default	Mode
0x10	AWBCNTR1	0xC3	R/W	0x43	AWBMRNG3	0x10	R/W
0x11	AWBCNTR2	0xC0	R/W	0x44	AWBSTEP1	0x12	R/W
0x12	AWBCNTR3	0x80	R/W	0x45	AWBSTEP2	0x35	R/W
0x13	CRTARGET	0x80	R/W	0x46	WINLRNG	0xF8	R/W
0x14	CBTARGET	0x80	R/W	0x47~0x5E	Reserved	-	-
0x15	RGNTOP	0xDF	R/W	0x5F	AWBSTST	0x00	R/W
0x16	RGNBOT	0x70	R/W	0x60	RGAIN	0xB0	R/W
0x17	BGNTOP	0xDF	R/W	0x61	BGAIN	0xB5	R/W
0x18	BGNBOT	0x78	R/W	0x62	GGAIN	0x80	R/W
0x19	WHTCRTOP	0x90	R/W	0x63	D20RGNI	0x90	R/W
0x1A	WHTCRBOT	0x70	R/W	0x64	D20BGNI	0xB0	R/W
0x1B	WHTCBTOP	0x90	R/W	0x65	D20RGNO	0x90	R/W
0x1C	WHTCBBOT	0x70	R/W	0x66	D20BGNO	0xB0	R/W
0x1D	WHTCXTOP	0x90	R/W	0x67	D30RGNI	0xA0	R/W
0x1E	WHTCXBOT	0x70	R/W	0x68	D30BGNI	0xA8	R/W
0x1F	Reserved	-	-	0x69	D30RGNO	0xA0	R/W
0x20	AWBLTOP	0xD8	R/W	0x6A	D30BGNO	0xA8	R/W
0x21	AWBLBOT	0x70	R/W	0x6B	CRAVG	0x80	R/W
0x22	RBLINE	0xA4	R/W	0x6C	CBAVG	0x80	R/W
0x23	RBOVER	0x20	R/W	0x6D	CRWHT	0x80	R/W
0x24	AWBGRNG	0xFF	R/W	0x6E	CBWHT	0x80	R/W
0x25	WHTCNTL	0x05	R/W	0x6F~0x70	Reserved	-	-
0x26	WHTCNTN	0x30	R/W	0x71	AWBTST	0x00	R/W
0x27	BRTSRT	0x04	R/W	0x72	FRGAIN	0x80	R/W
0x28	BRTRGNTOP	0xB8	R/W	0x73	FBGAIN	0x80	R/W
0x29	BRTRGNBOT	0xB0	R/W				
0x2A	BRTBGNTOP	0xB5	R/W				
0x2B	BRTBGNBOT	0xAF	R/W				
0x2C	GAINCONT	0x00	R/W				
0x2D~0x2F	Reserved	-	-				
0x30	AWBWINHSH	0x00	R/W				
0x31	AWBWINHSL	0x10	R/W				
0x32	AWBWINVSH	0x00	R/W				
0x33	AWBWINVSL	0x10	R/W				
0x34	AWBWINHEH	0x02	R/W				
0x35	AWBWINHEL	0x76	R/W				
0x36	AWBWINVEH	0x01	R/W				
0x37	AWBWINVEL	0xd6	R/W				
0x38~0x3F	Reserved	-	-				
0x40	AWBLRNG	0x01	R/W				
0x41	AWBMRNG1	0x04	R/W				
0x42	AWBNRNG2	0x08	R/W				

BANK [0x04]: IDP Block

Address	Name	Default	Mode	Address	Name	Default	Mode
0x10	IPFUN	0x40	R/W	0x3F	GMAF	0xFF	R/W
0x11	SIGCNT	0x1D	R/W	0x40	SPOSIA	0x0A	R/W
0x12	OUTFMT	0xD1	R/W	0x41	SPOSIB	0xDC	R/W
0x13	IPFUN2	0xFF	R/W	0x42	SPOSIC	0xBA	R/W
0x14	IPFUN3	0x00	R/W	0x43	SPOSID	0x98	R/W
0x15	VBTC	0x00	R/W	0x44	SPOSIE	0x75	R/W
0x16	Reserved	-	-	0x45	SPOSIF	0x31	R/W
0x17	Reserved	-	-	0x46	SHDHORR	0x00	R/W
0x18	DPCCTRL	0x8E	R/W	0x47	SHDVERR	0x00	R/W
0x19	BNRCTRL	0x0F	R/W	0x48	SHDHORGR	0x00	R/W
0x1A	DPCTHV	0x00	R/W	0x49	SHDVERGR	0x00	R/W
0x1B	DPCTHVSLP	0x24	R/W	0x4A	SHDHORGB	0x00	R/W
0x1C	DPCTHVDIFSRT	0x08	R/W	0x4B	SHDVERGB	0x00	R/W
0x1D	DPCTHVDIFSLP	0x08	R/W	0x4C	SHDHORB	0x00	R/W
0x1E	DPCTHVMAX	0xFF	R/W	0x4D	SHDVERB	0x00	R/W
0x1F	DPCNUMGX	0x55	R/W	0x4E	SHDCNTH	0x04	R/W
0x20	DPCNUMCX	0x55	R/W	0x4F	SHDCNTX	0x46	R/W
0x21	BNRTHV	0x04	R/W	0x50	SHDCNTY	0xF6	R/W
0x22	BNRTHVSLP	0x24	R/W	0x51	SSRT	0x80	R/W
0x23	BNRNEICNT	0x00	R/W	0x52	SHDOFSRR	0x00	R/W
0x24	STRTNOR	0x04	R/W	0x53	SHDOFSGR	0x00	R/W
0x25	STRTDRK	0x0F	R/W	0x54	SHDOFSGB	0x00	R/W
0x26	Reserved	-	-	0x55	SHDOFSBB	0x00	R/W
0x27	Reserved	-	-	0x56	Reserved	-	-
0x28	HxBLCL	-	R/O	0x57	SHDDRKCTRL2	0x00	R/W
0x29	RxBLCL	-	R/O	0x58	SHDDRKCTRL3	0x00	R/W
0x2A	GrBLCL	-	R/O	0x59 ~0x60	Reserved	-	-
0x2B	GbBLCL	-	R/O	0x61	INTCTRL1	0xF7	R/W
0x2C	BxBLCL	-	R/O	0x62	Reserved	-	-
0x2D	Reserved	-	-	0x63	Reserved	-	-
0x2E	Reserved	-	-	0x64	INTCTRL4	0x0C	R/W
0x2F	BLCCTRL	0x00	R/W	0x65	INTCTRL5	0xFF	R/W
0x30	GMA0	0x00	R/W	0x66	INTCTRL6	0x08	R/W
0x31	GMA1	0x08	R/W	0x67	INTCTRL7	0xFF	R/W
0x32	GMA2	0x10	R/W	0x68	INTCTRL8	0x00	R/W
0x33	GMA3	0x1B	R/W	0x69	INTCTRL9	0x00	R/W
0x34	GMA4	0x37	R/W	0x6A	INTCTRLA	0x00	R/W
0x35	GMA5	0x4D	R/W	0x6B	INTCTRLB	0x00	R/W
0x36	GMA6	0x60	R/W	0x6C	INTCTRLC	0xA0	R/W
0x37	GMA7	0x72	R/W	0x6D	INTCTRLD	0x10	R/W
0x38	GMA8	0x82	R/W	0x6E	INTCTRLE	0x08	R/W
0x39	GMA9	0x91	R/W	0x6F	INTCTRLF	0x18	R/W
0x3A	GMAA	0xA0	R/W	0x70	Reserved	-	-
0x3B	GMAB	0xBA	R/W	0x71	CMA11	0x3B	R/W
0x3C	GMAC	0xD3	R/W	0x72	CMA12	0xCE	R/W
0x3D	GMAD	0xEA	R/W	0x73	CMA13	0xF7	R/W
0x3E	GMAE	0xF5	R/W	0x74	CMA21	0x13	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Mode	Address	Name	Default	Mode
0x75	CMA22	0x25	R/W	0xAB	BRTCNT	0x00	R/W
0x76	CMA23	0x07	R/W	0xAC	CONTGAIN	0x10	R/W
0x77	CMA31	0xF2	R/W	0xAD	IMGYOFST	0x00	R/W
0x78	CMA32	0xC7	R/W	0xAE	HUECOS	0x40	R/W
0x79	CMA33	0x47	R/W	0xAF	HUESIN	0x00	R/W
0x7A	CMB11	0x3B	R/W	0xB0	YTOP	0xFF	R/W
0x7B	CMB12	0xCE	R/W	0xB1	YBOT	0x00	R/W
0x7C	CMB13	0xF7	R/W	0xB2	CRTOP	0xFF	R/W
0x7D	CMB21	0x13	R/W	0xB3	CRBOT	0x00	R/W
0x7E	CMB22	0x25	R/W	0xB4	CBTOP	0xFF	R/W
0x7F	CMB23	0x07	R/W	0xB5	CBBOT	0x00	R/W
0x80	CMB31	0xF2	R/W	0xB6	IEFCT	0x00	R/W
0x81	CMB32	0xC7	R/W	0xB7	CBEFCT	0x60	R/W
0x82	CMB33	0x47	R/W	0xB8	CREFCT	0xA0	R/W
0x83	CMC11	0x3B	R/W	0xB9	GSTRT	0x13	R/W
0x84	CMC12	0xCE	R/W	0xBA	GSLOP	0x10	R/W
0x85	CMC13	0xF7	R/W	0xBB	Reserved	-	-
0x86	CMC21	0x13	R/W	0xBC	Reserved	-	-
0x87	CMC22	0x25	R/W	0xBD	Reserved	-	-
0x88	CMC23	0x07	R/W	0xBE	DGCTRL	0x0C	R/W
0x89	CMC31	0xF2	R/W	0xBF	DGAIN	0x20	R/W
0x8A	CMC32	0xC7	R/W	0xC0	WDATH	0x34	R/W
0x8B	CMC33	0x47	R/W	0xC1	WHSRTL	0x00	R/W
0x8C	CMASEL	0x00	R/W	0xC2	WHWIDL	0xFF	R/W
0x8D	Reserved	-	-	0xC3	WVSRTL	0x00	R/W
0x8E	Reserved	-	-	0xC4	WVWIDL	0xFF	R/W
0x8F	Reserved	-	-	0xC5~0xCA	Reserved	-	-
0x90	EUGAIN	0x15	R/W	0xCB	EXTHXSYNK	0x00	R/W
0x91	EDGAIN	0x15	R/W	0xCC~0xD8	Reserved	-	-
0x92	ECORE	0x44	R/W	0xD9	ENHCTRL1	0x09	R/W
0x93	EUCORESTRT	0x12	R/W	0xDA	ENHCTRL2	0x10	R/W
0x94	EUCOREEND	0xFF	R/W	0xDB	ENHCTRL3	0x10	R/W
0x95	EUCORESLOP	0x20	R/W	0xDC	ENHCTRL4	0x20	R/W
0x96	Reserved	-	-	0xDD	Reserved	-	-
0x97	EDCORESTRT	0x12	R/W	0xDE	NOIZCTRL	0x24	R/W
0x98	EDCOREEND	0xFF	R/W	0xDF~0xE4	Reserved	-	-
0x99	EDCORESLOP	0x20	R/W	0xE5	MEMSPDA	0x15	R/W
0x9A	EUCLIP	0x20	R/W	0xE6	MEMSPDB	0x02	R/W
0x9B	EDCLIP	0x20	R/W	0xE7	MEMSPDC	0x04	R/W
0x9C	ESTART	0x13	R/W	0xE8	TSTFUN	0x00	R/W
0x9D	ESLOP	0x20	R/W	0xE9	TSTDATH	0x00	R/W
0x9E	EDGLEVEL	0x00	R/W	0xEA	TSTDATL	0x00	R/W
0x9F~0xa7	Reserved	-	-	0xEB	HxFNT	0x00	R/W
0xA8	YGAIN	0x10	R/W	0xEC	HxBCK	0x00	R/W
0xA9	CRGAIN	0x10	R/W				
0xAA	CBGAIN	0x10	R/W				

4.2. Accessible Register Feature

BANK [0x00]: PMU Block

<table>
<tr><th>Address</th><th>Name</th><th>Default</th><th>Description</th><th>Mode</th></tr>
<tr><td>0x00</td><td>BLK_SEL</td><td>0x00</td><td>[2:0] Block address (BANK) selector
000 PMU Control Block
001 Timing Control Block
010 AE control Block
011 AWB Control Block
100 IDP Control Block</td><td>R/W</td></tr>
<tr><td>0x01</td><td>ChipID</td><td>0x95</td><td>Chip device ID</td><td>R</td></tr>
<tr><td>0x02</td><td>INFO</td><td>0x10</td><td>Device version information</td><td>R</td></tr>
<tr><td>0x03</td><td>CHIP_CNTR</td><td>0x02</td><td>[7:6] PCLK output drivability control – PCLK output drive capability select
00: 3mA 01: 5.6mA 10: 5.6mA 11: 8.2mA
[5:4] Other output drivability control – other output drive capability select
00: 3mA 01: 5.6mA 10: 5.6mA 11: 8.2mA
[2] SDA output drivability control – SDA output drive capability select
0: 2.6mA 1: 5.2mA
[2] Output pad enable - It activates an output pin operation.
0 All output pads are in HI_Z state (except SDA)
1 Normal operation mode
[1] Control a S/W stand-by (power-down) mode
0 Normal operation mode
1 Stand-by mode
In S/W stand-by mode
- Digital block's and Analog block's power is off.
- I2C Operation is available</td><td>R/W</td></tr>
<tr><td>0x10</td><td>LDO_CNTR</td><td>0x02</td><td>[7] Control Main LDO's Operation.
0 Off Main LDO at Power Down Mode.
1 On Main LDO at Power Down Mode.
[5] SKEW_EN : PAD SKEW Enable
[4] SKEW_LV : PAD SKEW Level
<table>
<tr><th>SKEW_EN</th><th>SKEW_LV</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>Bypass</td></tr>
<tr><td>0</td><td>1</td><td>Don't use</td></tr>
<tr><td>1</td><td>0</td><td>Default 대비 0.6ns 증가</td></tr>
<tr><td>1</td><td>1</td><td>Default 대비 1.2ns 증가</td></tr>
</table>
[1:0] Sensor control registers (Must set up recommended value)</td><td>R/W</td></tr>
</table>

BANK [0x01]: Control Block

<table>
<tr><th>Address</th><th>Name</th><th>Default</th><th>Description</th><th>Mode</th></tr>
<tr><td>0x03</td><td>CNTR_A</td><td>0x02</td><td>[0] Control device enable - Assert the device into an idle or dynamic mode
0 Idle mode – Internal clock is disable
1 Dynamic mode – Normal operation mode</td><td>R/W</td></tr>
<tr><td>0x04</td><td>CNTR_B</td><td>0x00</td><td>[7:6] Control fixed frame mode
00 Normal operation mode
01 Fixed frame mode @ exposure time <= frame size
Normal operation mode @ exposure time > frame size
10/11 Fixed frame mode
[3:2] Clock (PCLK) divider – max 1/8 PCLK
00: PCLK 01: 1/2PCLK 10: 1/4PCLK 11: 1/8PCLK
[1] Control vertical flip image
0 Normal image
1 Vertical flip image
[0] Control horizontal flip (mirror) image
0 Normal image
1 Horizontal flip (mirror) image</td><td>R/W</td></tr>
<tr><td>0x06</td><td>VMODE</td><td>0x04</td><td>[7:6] @ sub-sampling mode
[7] vertical binning
[6] horizontal binning
[2:0] Control Display Mode
<table>
<tr><th colspan="3">VMODE
[2:0]</th><th>Video Format</th><th>Window Size</th><th>Sensor
Output</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>QQCIF(88 x 72)</td><td>368x304</td><td>184x152</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>QCIF(176 x 144)</td><td>368x304</td><td>184x152</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>CIF_(352 x 288)</td><td>360x296</td><td>360x296</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>QQVGA(160 x 120)</td><td>656 x 496</td><td>328 x248</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>QVGA(320 x 240)</td><td>656 x 496</td><td>328 x248</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>VGA(640 x 480)</td><td>648 x488</td><td>648 x488</td></tr>
</table></td><td></td></tr>
<tr><td>0x08</td><td>UPDATE
_FLAG</td><td>0x00</td><td>[0] Shadow update flag @ register writing
0 : No operation
1 : Shadow update enable @ EN_UP_SHW register '1', auto cleared</td><td></td></tr>
<tr><td>0x09~0x1F</td><td></td><td></td><td>Sensor control register (Must set up recommended value)</td><td></td></tr>
</table>

BANK [0x01]: Control Block

Address	Name	Default	Description	Mode
0x20	BNKT	0x00	[7:4] HBNKT[11:8] [3:0] VBNKT[11:8]	R/W
0x21	HBNKT	0x65	HBNKT[7:0]	R/W
0x22	VBNKT	0x03	VBNKT[7:0]	R/W
0x23	SCAN	0x63	If Reg0x04[5] =1 (HST_EN), Use Horizontal Scan Time. SCAN[7:0] : Define HST Time , Unit is CLK Real HST Time = (SCAN[7:0]) + 1	R/W
0x24	ROWFILL	0x31	ROWFILL[7:0] : Define Row Fill Time , Unit is PCLK Real Row Fill Time = (ROWFILL[7:0]) +1	R/W
0x25-0x50			Reserved registers & sensor test registers (Must set up recommended values)	
0x51	TEST51	0x00	[1] EN_UP_SHW : Shadow update enable @ last update register writing **0 : Shadow update disable** **1 : Shadow update enable (UPDATE_SHW register)**	
0x52~0x5F			Reserved registers & sensor test registers (Must set up recommended values)	

BANK [0x02]: AE Block

Address	Name	Default	Description	Mode
0x10	AE_CNTR	0x80	[7] Control AE function **0 Disable AE function** **1 Enable AE function** [6] AE_STOP : Control AutoExposure Function **0 : Run AutoExposure Function** **1 : Stop AutoExposure Function** [2] Adjust BLC Value @ Very dark condition (shutter time & GAIN max) **0 Disable adjust BLC value** **1 Enable adjust BLC value**	R/W
0x11	MAX_SHUTSTEP	0x0F	[5:0] This register defines the maximum exposure time of the AE function by writing the integer proportion of the STST_P. **Max. Shutter Time = (Max_Shut_Step[5:0] x Shutter_Step) Rows**	R/W
0x12	Y_TARGET_N	0x80	The luminance target value of AE function for D65 Light Source	R/W
0x13	Y_TARGET_CWF	0x80	The luminance target value of AE function for CWF Light Source	R/W
0x14	Y_TARGET_A	0x78	The luminance target value of AE function for A Light Source	R/W
0x16	LOCK_LEVEL	0x40	[7:6] AE Speed Control **00 : Fast -> 11 : Slow** [2:0] Stop difference level of AE function - Lock level of shutter time & gain Difference Level = ((|Y_TARGET – Y_AVG|)/YTGT_LEVEL)*100% **000: Level0 (<3%) 001: Level1 (<6.125%)** **010: Level2 (<12.5%) 011: Level3 (<25%)** **100: Level4 (<50%) 101: Level5 (<75%)** **110: Level6 (>75%) 111: Level7 (AE Stop)**	R/W
0x18	AEADCT	0x00	Sensor control register (Must set up recommended value)	R/W
0x19	DA2BR	0x8E	[7] Dark to bright function enable – AE speed-up at dark to very bright condition. **0 Disable DA2BR function** **1 Enable Shutter Step Control** [6] Level Option for Function Enable **0 Y_AVG >= 208** **1 Y_AVG = Level6** Minimum shutter time for function enable (unit: Sutter step)	R/W
0x1A	D2B_RET_TIME	0x06	[5:0] This register sets new shutter time at DA2BR function enable condition. (unit: Sutter step)	R/W
0x1B	BR2DA	0x00	[7] Bright to dark function control – AE speed-up at bright to very dark condition. **0 Disable BR2DA function** **1 Enable BR2DA function** BR2DA function Enable condition 1) Shutter Time <= BR_SHUT 2) Y_TARGET > Y_AVG 3) Y_AVG <= 31 [6] Level Option for Function Enable **0 Y_AVG >= 208** **1 Y_AVG = Level6** [5:0] Maximum shutter time for BR2DA function enable (unit: Line)	R/W

BANK [0x02]: AE Block

Address	Name	Default	Description	Mode
0x1C			Sensor control register (Must set up recommended value)	
0x1D	INI_SHUTTIME	0x01	[7] Initial Shutter Time Control Register **0 INI_SHUTTIME[5:0], Unit is Shutter Step** **1 INI_SHUTTIME[6:0], Unit is Row** [6:0] Initial Shut Time @ AE Function Start	R/W
0x1E	INI_CGAIN	0x00	Initial Coarse Gain @ AE Function Start	R/W
0x1F~0x2F			Sensor control register (Must set up recommended value)	
0x30	SHTH	0x00	Upper 8 bits of shutter time [15:8] (unit: Line)	R/W
0x31	SHTL	0x7D	Lower 8 bits of shutter time [7:0] (unit: Line) The AE function automatically controls the shutter time (exposure time).	R/W
0x32	CGAIN	0x08	Coarse Gain Register .	R/W
0x33	FGAIN	0x28	Fine Gain Register	
0x34	STST_P	0x7D	Anti-flicker shutter step	R/W
0x35-0x3F			Reserved	
0x40	G_MAX	0x45	Max Gain Value @ Shutter step = Max Shutter step (Max : x32) Gain Value = 2 *G_XX[7:5] x (1 +G_XX [4:0]/32])	R/W
0x42	G_TOP0	0x28	Gain Top @ Shutter step < Max. Shutter step	R/W
0x44	G_MIN0	0x08	Min Gain Value	R/W
0x45	G50_DEG	0x09	GAIN adjust value @ shutter step1 ->shutter step2	R/W
0x46	G33_DEC	0x17	GAIN adjust value @ shutter step2 ->shutter step3	R/W
0x47	G25_DEC	0x1D	GAIN adjust value @ shutter step3 ->shutter step4	R/W
0x48	G20_DEC	0x21	GAIN adjust value @ shutter step4 ->shutter step5	R/W
0x49	G12_DEC	0x23	GAIN adjust value @ shutter step5-6 ->shutter step6-7	R/W
0x4A	G09_DEC	0x24	GAIN adjust value @ shutter step7-9 ->shutter step8-10	R/W
0x4B	G06_DEC	0x26	GAIN adjust value @ shutter step10-14 ->shutter step11-15	R/W
0x4C	G03_DEC	0x27	GAIN adjust value @ shutter step15-22->shutter step16-23	R/W
0x4D	G100_INC	0x27	GAIN adjust value @ shutter step2 ->shutter step1	R/W
0x4E	G50_INC	0x1A	GAIN adjust value @ shutter step3 ->shutter step2	R/W
0x4F	G33_INC	0x14	GAIN adjust value @ shutter step4 ->shutter step3	R/W
0x50	G25_INC	0x11	GAIN adjust value @ shutter step5 ->shutter step4	R/W
0x51	G20_INC	0x0F	GAIN adjust value @ shutter step6 ->shutter step5	R/W
0x52	G12_INC	0x0D	GAIN adjust value @ shutter step7-8 ->shutter step6-7	R/W
0x53	G09_INC	0x0C	GAIN adjust value @ shutter step9-11 ->shutter step8-10	R/W
0x54	G06_INC	0x0A	GAIN adjust value @ shutter step12-16 ->shutter step11-15	R/W
0x55	G03_INC	0x09	GAIN adjust value @ shutter step17-24->shutter step16-23	R/W
0x56-0x5E			Sensor control register (Must set up recommended value)	
0x5F	WIN_CNT	0x00	Window Average Control Register 0 : Center Weight Average 1. Flat Average 2. Spot Mode Average	R/W
0x60~0x86			Control and reserved registers	

BANK [0x03]: AWB Block

Address	Name	Default	Description	Mode
0x10	AWBCNTR1	0xC3	[7:6] Control AWB function & mode selector **00 Disable AWB function** **01 Enable Average mode AWB function** **11 Enable Advanced mode AWB function** [5] AWB gain fix [4] AWB speed control **1 Normal 0 Fast** [2:0] AWB options **000/001/110/111 No option** **010 AWB gain move fix @ Integration Time < BRTSRT** **011 AWB gain move between BRTRGNBOT(BRTBGNBOT) and BRTRGNTOP(BRTBGNTOP) @ Integration Time < BRTSRT** **100 AWB gain fix to BRTRGN & BRTBGN** **101 Manual Gain (FRGAIN,FBGAIN) Enable** **=> BRTRGN = (BRTRGNTOP + BRTRGNBOT) / 2** **BRTBGN = (BRTBGNTOP + BRTBGNBOT) / 2**	R/W
0x11	AWBCNTR2	0xC0	[7:5] AWB UNLOCK Check Selection @ Advanced Mode **000 Unlock condition @ White Pixel Count < WHTCNTL** **001 Unlock condition @ CRAVG > WINLRNG or CBAVG > WINLRNG** **010 Unlock condition @ "case 000" or "case 001"** **011 Unlock condition @ "case 000" and "case 001"** **100 Unlock condition @ WCRAVG > WINLRNG or WCBAVG > WINLRNG** **101 Unlock condition @ "case 000" or "case 100"** **110 Unlock condition @ "case 000" and "case 100"** [2] AWB operation start at AE stable condition **0 Always AWB Working (default)** **1 AWB Working after AE Stable** [1] AWB Gain Boundary Control Selection @ Outdoor<->Indoor **0 Off** **1 On**	R/W
0x12	AWBCNTR3	0x80	[7] AWB gain move select in AWB lock condition This function is enabled that AWB gain moves all the time. **0 AWB gain not moving in lock range** **1 AWB gain moving in lock range** [6:5] AWB frame update speed control **00 2-frame based AWB calculation** **01 4-frame based AWB calculation** **10/11 8-frame based AWB calculation**	R/W
0x13	CRTARGET	0x80	AWB Cr target value	R/W
0x14	CBTARGET	0x80	AWB Cb target value	R/W
0x15	RGNTOP	0xDF	AWB R gain top value	R/W

BANK [0x03]: AWB Block

Address	Name	Default	Description	Mode
0x16	RGNBOT	0x70	AWB R gain bottom value	R/W
0x17	BGNTOP	0xDF	AWB B gain top value	R/W
0x18	BGNBOT	0x78	AWB B gain bottom value	R/W
0x19	WHTCRTOP	0x90	CR Top Value for AWB White Pixel Detection	R/W
0x1A	WHTCRBOT	0x70	CR Bottom Value for AWB White Pixel Detection	R/W
0x1B	WHTCBTOP	0x90	CB Top Value for AWB White Pixel Detection	R/W
0x1C	WHTCBBOT	0x70	CB Bottom Value for AWB White Pixel Detection	R/W
0x1D	WHTCXTOP	0x90	CR+CB Average Top Value for AWB White Pixel Detection	R/W
0x1E	WHTCXBOT	0x70	CR+CB Average Bottom Value for AWB White Pixel Detection	R/W
0x20	AWBLTOP	0xD8	Luminance top value for AWB White Pixel Detection	R/W
0x21	AWBLBOP	0x70	Luminance bottom value for AWB White Pixel Detection	R/W
0x22	RBLINE	0xA4	R + B gain average line value	R/W
0x23	RBOVER	0x20	Lock range of R + B gain average line value	R/W
0x24	AWBGRNG	0xFF	R, B gain range related to G gain	R/W
0x25	WHTCNTL	0x05	White Pixel Count for Unlock Condition(X32)	R/W
0x26	WHTCNTN	0x30	White Pixel Minimum Count(X32) for White Mode	R/W
0x27	BRTSRT	0x04	Integration time start value for decision of very bright condition R & B gain fix to BRTRGN, BRTBGN @ integration time < BRTSRT	R/W
0x28	BRTRGNTOP	0xB8	RGain Top @ Outdoor <-> Indoor Gain Boundary Control	R/W
0x29	BRTRGNBOT	0xB0	RGain Bottom @ Outdoor <-> Indoor Gain Boundary Control	R/W
0x2A	BRTBGNTOP	0xB5	BGain Top @ Outdoor <-> Indoor Gain Boundary Control	R/W
0x2B	BRTBGNBOT	0xAF	BGain Bottom @ Outdoor <-> Indoor Gain Boundary Control	R/W
0x2C	GAINCONT	0x00	Outdoor <-> Indoor R(B)GAIN Step Control @ Integration Time > BRTSRT SCALE : 0.5 -> [2] On 1 -> [1:0] == 00 2 -> [1:0] == 01 4 -> [1:0] == 10 8 -> [1:0] == 11 **calRGNTOP = BRTRGNTOP + |IntTime – BRTSRT| / SCALE** **calRGNBOT = BRTRGNBOT - |IntTime – BRTSRT| / SCALE** **calBGNTOP = BRTBGNTOP + |IntTime – BRTSRT| / SCALE** **calBGNBOT = BRTBGNBOT - |IntTime – BRTSRT| / SCALE**	R/W

BANK [0x03]: AWB Block

Address	Name	Default	Description	Mode
0x2D~0x2F	-	-	Reserved	
0x30	AWBWINHSH	0x00	AWB Horizontal Window Start Byte	R/W
0x31	AWBWINHSL	0x10	= { AWBWINHSH[1:0], AWBWINHSL[7:0] }	
0x32	AWBWINVSH	0x00	AWB Vertical Window Byte	R/W
0x33	AWBWINVSL	0x10	= { AWBWINVSH[0], AWBWINVSL[7:0]}	
0x34	AWBWINHEH	0x02	AWB Horizontal Window End High Byte	R/W
0x35	AWBWINHEL	0x76	= { AWBWINHEH[1:0], AWBWINHEL[7:0]}	
0x36	AWBWINVEH	0x01	AWB Vertical Window End High Byte	R/W
0x37	AWBWINVEL	0xD6	= { AWBWINVEH[0], AWBWINVEL[7:0]}	
0x38-0x3F	-	-	Reserved	
0x40	AWBLRNG	0x01	AWB Lock Range	R/W
0x41	AWBMRNG1	0x04	AWB Un-Lock Range Level 1 (AWBLRNG < AWBMRNG1)	R/W
0x42	AWBMRNG2	0x08	AWB Un-Lock Range Level 2 (AWBLRNG1 < AWBMRNG2)	R/W
0x43	AWBMRNG3	0x10	AWB Un-Lock Range Level 3 (AWBLRNG2 < AWBMRNG3)	R/W
0x44	AWBSTEP1	0x12	[7:4] Move step value 1 **Move Step @ AWBLRNG <= |Average –Target| < AWBMRNG1** [3:0] Move step value 2 **Move Step @ AWBLRNG1 <= |Average –Target| < AWBMRNG2**	R/W
0x45	AWBSTEP2	0x35	[7:4] Move step value 3 **Move Step @ AWBLRNG2 <= |Average –Target| < AWBMRNG3** [3:0] Move step value 4 **Move Step @ AWBLRNG3 <= |Average –Target|**	R/W
0x46	WINLRNG	0xF8	[7:4] AWBURNG : Average mode enable condition **Average Mode Start @ |Average – Target| >= AWBURNG** [3:0] AWBLRNG : White mode enable condition **White Mode Start @ |Average – Target| < AWBLRNG**	R/W
0x47-0x5E	-	-	Reserved	-
0x5F	AWBSTST	0x00	[7] : **D20 Light Source Detection** [6] : **D30 Light Source Detection**	R
0x60	RGAIN	0xB0	AWB R gain (x1/128) The AWB function automatically controls the R gain level. (VSync Synchronous)	R/W
0x61	BGAIN	0xB5	AWB B gain (x1/128) The AWB function automatically controls the B gain level. (VSync Synchronous)	R/W

BANK [0x03]: AWB Block

Address	Name	Default	Description	Mode
0x62	GGAIN	0x80	AWB G gain (x1/128) The AWB function automatically controls the G gain level.	R/W
0x63	D20RGNI	0x90	AWB R Gain for D30 to D20	R/W
0x64	D20BGNI	0xB0	AWB B Gain for D30 to D20	R/W
0x65	D20RGNO	0x90	AWB R Gain for D20 to D30	R/W
0x66	D20BGNO	0xB0	AWB B Gain for D20 to D30	R/W
0x67	D30RGNI	0xA0	AWB R Gain for D65 to D30	R/W
0x68	D30BGNI	0xA8	AWB B Gain for D65 to D30	R/W
0x69	D30RGNO	0xA0	AWB R Gain for D30 to D65	R/W
0x6A	D30BGNO	0xA8	AWB B Gain for D30 to D65	R/W
0x6B	CRAVG	0x80	Cr frame average value (VSync Synchronous)	R/W
0x6C	CBAVG	0x80	Cb frame average value (VSync Synchronous)	R/W
0x6D	WCRAVG	0x80	White pixel Cr frame average value (VSync Synchronous)	R/W
0x6E	WCBAVG	0x80	White pixel Cb frame average value (VSync Synchronous)	R/W
0x6F~70	-	-	Reserved	R/W
0x71	AWBTST	0x00	[7] TYPE1: **AWB Window Test** [6] TYPE2: **AWB Data Control Signal Test** [5] TYPE3: **Average Mode CR Average Value Test** [4] TYPE4: **Average Mode CB Average Value Test** [3] TYPE5: **White Mode CR Average Value Test** [2] TYPE6: **White Mode CB Average Value Test** [1] TYPE7: **AWB Finite State Machine Test**	R/W
0x72	FRGAIN	0x80	Manual R Gain Value (VSync Synchronous)	R/W
0x73	FBGAIN	0x80	Manual B Gain Value (VSync Synchronous)	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0x10	IPFUN	0x40	[7] Reserved [6] Pixel Data Change Function Enable [5] AWB Gain Adaption Function Enable [4] Reserved [3] BLC Function Enable [2] Gamma Function Enable [1] Color Matrix & Color Space Conversion Enable [0] Shading Function Enable	R/W
0x11	SIGCNT	0x1D	[7] Vertical Blank Time Control Enable [6] VSYNC Data Selection (1: Short VSYNC, 0: Long VSYNC) [5] Dummy HSYNC Output Enable at Short VSYNC [4] PCLK Clock Polarity Control(1: Positive Data Sync, 0: Negative Data Sync) [3] HSYNC Polarity Control (1: Data Active at HIGH, 0: Data Active at LOW) [2] VSYNC Polarity Control (1: Data Active at LOW, 0: Data Active at HIGH) [1] HSYNC Valid at VSYNC (1: Valid, 0: Not Valid) [0] PCLK Valid at VSYNC, HSYNC	R/W
0x12	OUTFMT	0xD1	[7] UV Mean Value Output at YUV422 Mode [6] Reserved [5:4] Color Mode Selection @ YUV Mode – [5] Y First Selection, [4] U First Selection @ RGB Mode – [5] Byte Swap Selection, [4] B First Selection [3] Window Mode Enable [2:0] Output Mode Selection 000: 8-Bit Bayer Mode (Original Data) 001: 8-Bit Bayer Mode (DPCed Data) 010: 8-Bit B/W Mode 011: RGB565 Mode 101 : YUV422 Mode	R/W
0x13	IPFUN2	0xFF	[7] YUV2RGB Conversion Function Enable [6] Dead Pixel Concealment Function Enable [5] Interpolation Function Enable [4] Sharpness Function Enable [3] Reserved [2] Color Improvement Function Enable [1] HUE Control Function Enable [0] Adaptive Shading Enable @ Dark Condition	R/W
0x14	IPFUN3	0x00	[7] IDP Function Enable 1: Full Working 0: HSYNC Only Working [6] Reserved [5] Memory Working Time Control 0: HSYNC Only 1: Full Case [4] Memory Kill Function Enable [3] Extended HSYNC Selection [2:1] Reserved [0] AEBLC Value Adaptation Block Selection 0: BLC Block 1: AWB Block	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0x15	VBTC	0x00	[7:3] VSYNC Deleting HSYNC Line Count from VSYNC Start [2:0] VSYNC Deleting HSYNC Line Count from the end of VSYNC.	0x15
0x16	-	-	Reserved	-
0x17	-	-	Reserved	-
0x18	DPCCTRL	0x8E	[7] DPC Enable [6:4] Reserved [3] G1/G2 Mixed DPC for Full Mode [2] G1/G2 Mixed DPC for Sub Mode [1] DPC Method for Gx channel 0 : Median in 8-neighbors 1 : Maximum/Minimum in8-Neighbors [0] DPC Method for Rx/Bx channel 0 : Median in 8-neighbors 1 : Maximum/Minimum in 8-Neighbors	R/W
0x19	BNRCTRL	0x0F	[7:5] Half Edge Value Selection [7] Highly Illumination and Flat Pixel [6] Highly Illumination Pixel [5] Flat Pixel [4] Reserved [3] BNR Enable [2] G1/G2 Mixed NR for Full Mode [1] G1/G2 Mixed NR for Sub Mode [0] Twice Weight Selection of x direction Pixel of NR	R/W
0x1A	DPCTHV	0x00	[7:0] DPC Threshold Value @ Outdoor Condition (IllumiInfo < STRTNOR)	R/W
0x1B	DPCTHVSLP	0x24	[7:4] Decreasing DPC Threshold Slope for Normal Condition (STRTNOR < IllumiInfo < STRTDRK) [3:0] Decreasing DPC Threshold Slope for Dark Condition (IllumiInfo > STRTDRK)	R/W
0x1C	DPCTHVDIFSRT	0x08	[5:0] Increasing DPC Threshold Starting Value via SAD Value	R/W
0x1D	DPCTHVDIFSLP	0x08	[5:0] Increasing DPC Threshold Slope via SAD Value (1/8 resolution, 0.000~8.000)	R/W
0x1E	DPCTHVMAX	0xFF	[7:0] Maximum Limit of DPC Threshold Value	R/W
0x1F	DPCNUMGX	0x55	Gx Channel DP Number [7:6] DP Num @ Outdoor/Normal Condition for Full Mode [5:4] DP Num @ Outdoor/Normal Condition for Sub Mode [3:2] DP Num @ Dark Condition for Full Mode [1:0] DP Num @ Dark Condition for Sub Mode	R/W
0x20	DPCNUMCX	0x55	Cx Channel DP Number [7:6] DP Num @ Outdoor/Normal Condition for Full Mode [5:4] DP Num @ Outdoor/Normal Condition for Sub Mode [3:2] DP Num @ Dark Condition for Full Mode [1:0] DP Num @ Dark Condition for Sub Mode	R/W
0x21	BNRTHV	0x04	[7:0] Bayer NR Threshold Value @ Outdoor Condition (IllumiInfo < STRTNOR)	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0x22	BNRTHVSLP	0x24	[7:4] Increasing Bayer NR Threshold Slope for Normal Condition (STRTNOR < IllumiInfo < STRTDRK) [3:0] Increasing Bayer NR Threshold Slope for Dark Condition (IllumiInfo > STRTDRK)	R/W
0x23	BNRNEICNT	0x00	[7] Reserved [6:4] Minimum NR Weight for + direction Pixel [3] Reserved [2:0] Minimum NR Weight for x direction Pixel	R/W
0x24	STRTNOR	0x04	[7:0] IllumiInfo Threshold Point for Outdoor → Indoor	R/W
0x25	STRTDRK	0x0F	[7:0] IllumiInfo Threshold Point for Indoor → Dark	R/W
0x26	-	-	Reserved	-
0x27	-	-	Reserved	-
0x28	HxBLCL	-	[7:6] MSB of Red Pixel Dark Value [5:4] MSB of Green (RG-Line) Pixel Dark Value [3:2] MSB of Green (BG-Line) Pixel Dark Value [1:0] MSB of Blue Pixel Dark Value	R/O
0x29	RxBLCL	-	[7:0] LSB of Red Pixel Dark Value RxBLC Value = {HxBLCL[7:6],RxBLCL}	R/O
0x2A	GrBLCL	-	[7:0] LSB of Green (RG-Line) Pixel Dark Value GrBLC Value = {HxBLCL[5:4],GrBLCL}	R/O
0x2B	GbBLCL	-	[7:0] LSB of Green (BG-Line) Pixel Dark Value GbBLC Value = {HxBLCL[3:2],GbBLCL}	R/O
0x2C	BxBLCL	-	[7:0] LSB of Blue Pixel Dark Value BxBLC Value = {HxBLCL[1:0],BxBLCL}	R/O
0x2D ~ 0x2E	-	-	Reserved	-
0x2F	BLCCTRL	0x00	[7] BLC Update without AE Stop [6] BLC Update When Difference is over BLC Threshold [5:0] BLC Threshold	R/W
0x30	GMA0	0x00	[7:0] Gamma Point at 0 (10-Bit Input)	R/W
0x31	GMA1	0x08	[7:0] Gamma Point at 16 (10-Bit Input)	R/W
0x32	GMA2	0x10	[7:0] Gamma Point at 32 (10-Bit Input)	R/W
0x33	GMA3	0x1B	[7:0] Gamma Point at 64 (10-Bit Input)	R/W
0x34	GMA4	0x37	[7:0] Gamma Point at 128 (10-Bit Input)	R/W
0x35	GMA5	0x4D	[7:0] Gamma Point at 192 (10-Bit Input)	R/W
0x36	GMA6	0x60	[7:0] Gamma Point at 256 (10-Bit Input)	R/W
0x37	GMA7	0x72	[7:0] Gamma Point at 320 (10-Bit Input)	R/W
0x38	GMA8	0x82	[7:0] Gamma Point at 384 (10-Bit Input)	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0x39	GMA9	0x91	[7:0] Gamma Point at 448 (10-Bit Input)	R/W
0x3A	GMAA	0xA0	[7:0] Gamma Point at 512 (10-Bit Input)	R/W
0x3B	GMAB	0xBA	[7:0] Gamma Point at 640 (10-Bit Input)	R/W
0x3C	GMAC	0xD3	[7:0] Gamma Point at 768 (10-Bit Input)	R/W
0x3D	GMAD	0xEA	[7:0] Gamma Point at 896 (10-Bit Input)	R/W
0x3E	GMAE	0xF5	[7:0] Gamma Point at 960 (10-Bit Input)	R/W
0x3F	GMAF	0xFF	[7:0] Gamma Point at 1023 (10-Bit Input)	R/W
0x40	SPOSIA	0x0A	[7:4] Area A Shading Gain [3:0] Area B Shading Gain	R/W
0x41	SPOSIB	0xDC	[7:4] Area C Shading Gain [3:0] Area D Shading Gain	R/W
0x42	SPOSIC	0xBA	[7:4] Area E Shading Gain [3:0] Area F Shading Gain	R/W
0x43	SPOSID	0x98	[7:4] Area G Shading Gain [3:0] Area H Shading Gain	R/W
0x44	SPOSIE	0x75	[7:4] Area I Shading Gain [3:0] Area J Shading Gain	R/W
0x45	SPOSIF	0x31	[7:4] Area K Shading Gain [3:0] Area L Shading Gain	R/W
0x46	SHDHORR	0x00	[7:4] X-axis R Shading Gain for Left Side from Horizontal Center [3:0] X-axis R Shading Gain for Right Side from Horizontal Center	R/W
0x47	SHDVERR	0x00	[7:4] Y-axis R Shading Gain for Top Side from Vertical Center [3:0] Y-axis R Shading Gain for Bottom Side from Vertical Center	R/W
0x48	SHDHORGR	0x00	[7:4] X-axis G(RG-Line) Shading Gain for Left Side from Horizontal Center [3:0] X-axis G(RG-Line) Shading Gain for Right Side from Horizontal Cent er	R/W
0x49	SHDVERGR	0x00	[7:4] Y-axis G(RG-Line) Shading Gain for Top Side from Vertical Center [3:0] Y-axis G(RG-Line) Shading Gain for Bottom Side from Vertical Center	R/W
0x4A	SHDHORGB	0x00	[7:4] X-axis G(BG-Line) Shading Gain for Left Side from Horizontal Center [3:0] X-axis G(BG-Line) Shading Gain for Right Side from Horizontal Cent er	R/W
0x4B	SHDVERGB	0x00	[7:4] Y-axis G(BG-Line) Shading Gain for Top Side from Vertical Center [3:0] Y-axis G(BG-Line) Shading Gain for Bottom Side from Vertical Center	R/W
0x4C	SHDHORB	0x00	[7:4] X-axis B Shading Gain for Left Side from Horizontal Center [3:0] X-axis B Shading Gain for Right Side from Horizontal Center	R/W
0x4D	SHDVERB	0x00	[7:4] Y-axis B Shading Gain for Top Side from Vertical Center [3:0] Y-axis B Shading Gain for Bottom Side from Vertical Center	R/W
0x4E	SHDCNTH	0x04	[7:4] Reserved [3:2] MSB of Shading X-axis Center Position [1:0] MSB of Shading Y-axis Center Position	R/W
0x4F	SHDCNTX	0x46	[7:0] LSB of Shading X-axis Center Position {SHDCNTH[3:2],SHDCNTX}	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0x50	SHDCNTY	0xF6	[7:0] LSB of Shading Y-axis Center Position {SHDCNTH[1:0],SHDCNTY}	R/W
0X51	SSRT	0x80	[7:0] Shading Center Start Gain (X1/128)	R/W
0X52	SHDOFSRR	0x00	[7:0] R Shading Offset Value	R/W
0X53	SHDOFSGR	0x00	[7:0] G(RG-Line) Shading Offset Value	R/W
0x54	SHDOFSGB	0x00	[7:0] G(BG-Line) Shading Offset Value	R/W
0x55	SHDOFSBB	0x00	[7:0] B Shading Offset Value	R/W
0x56	-	-	Reserved	-
0x57	SHDDRKCTRL2	0x00	[7] MSB of Adaptive Shading Slope Gain [6] MSB of Adaptive Shading End Point [5:0] Adaptive Shading Start Point	R/W
0x58	SHDDRKCTRL3	0x00	[7:4] LSB of Adaptive Shading Slope Gain {SHDDRKCTRL2[7],SHDDRKCTRL3[7:4]} [3:0] LSB of Adaptive Shading End Point {SHDDRKCTRL2[6],SHDDRKCTRL[3:0]}	R/W
0x59~0x60	-	-	Reserved	-
0x61	INTCTRL1	0xF7	[7] Filter Selection for G1/G2 Variation Suppression 1: Strong Filter, 0: Weak Filter [6] Filter Selection for Random Noise Reduction 1: Strong Filter, 0: Weak Filter [5] Highly Illuminated Pixel Detection Enable [4] Flat Pattern Detection Enable 1: Interpolation for Noise Suppression @ Flat Pattern, 0: Interpolation for sharpness @ Flat Pattern [3] Highly Illuminated Pixel Interpolation Method 1: Interpolation for gradient suppression @ Highly Illuminated Pixel, 0: general interpolation @ Highly Illuminated Pixel [2] G Pixel Interpolation Method1 1: G Value Interpolated considering R/B Cahnnel Gradient, 0: G Value Interpolated using only G Pixel Values [1] Filter Enable for G1/G2 Variation Suppression [0] Filter Enable for Random Noise Reduction	R/W
0x62~0x63	-	-	Reserved	-
0x64	INTCTRL4	0x0C	[7:0] Edge Sensing Minimum Threshold	R/W
0x65	INTCTRL5	0xFF	[7:0] Edge Sensing Maximum Threshold	R/W
0x66	INTCTRL6	0x08	[7:0] LPF Minimum Threshold	R/W
0x67	INTCTRL7	0xFF	[7:0] LPF Maximum Threshold	R/W
0x68	INTCTRL8	0x00	[7:6] Reserved [5:0] Edge Sensing Threshold Increasing Start Point	R/W
0x69	INTCTRL9	0x00	[7:6] Reserved [5:0] LPF Threshold Increasing Start Point	R/W
0x6A	INTCTRLA	0x00	[7:0] Edge Sensing Threshold Slop	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0x6B	INTCTRLB	0x00	[7:0] LPF Threshold Slop	R/W
0x6C	INTCTRLC	0xA0	[7:0] Highly illuminated Pixel Detect Threshold	R/W
0x6D	INTCTRLD	0x10	[7:0] Hi-Frequency Kernel Detect Threshold	R/W
0x6E	INTCTRLE	0x08	[7:0] G1/G2 Offset Detection Minimum Threshold	R/W
0x6F	INTCTRLF	0x18	[7:0] G1/G2 Offset Detection Maximum Threshold	R/W
0x70	-	-	Reserved	-
0x71	CMA11	0x3B	[7:0] Color Matrix Coefficient 11 for D65 (X1/64, 2's Comp.)	R/W
0x72	CMA12	0xCE	[7:0] Color Matrix Coefficient 12 for D65 (X1/64, 2's Comp.)	R/W
0x73	CMA13	0xF7	[7:0] Color Matrix Coefficient 13 for D65 (X1/64, 2's Comp.)	R/W
0x74	CMA21	0x13	[7:0] Color Matrix Coefficient 21 for D65 (X1/64, 2's Comp.)	R/W
0x75	CMA22	0x25	[7:0] Color Matrix Coefficient 22 for D65 (X1/64, 2's Comp.)	R/W
0x76	CMA23	0x07	[7:0] Color Matrix Coefficient 23 for D65 (X1/64, 2's Comp.)	R/W
0x77	CMA31	0xF2	[7:0] Color Matrix Coefficient 31 for D65 (X1/64, 2's Comp.)	R/W
0x78	CMA32	0xC7	[7:0] Color Matrix Coefficient 32 for D65 (X1/64, 2's Comp.)	R/W
0x79	CMA33	0x47	[7:0] Color Matrix Coefficient 33 for D65 (X1/64, 2's Comp.)	R/W
0x7A	CMB11	0x3B	[7:0] Color Matrix Coefficient 11 for D30 (X1/64, 2's Comp.)	R/W
0x7B	CMB12	0xCE	[7:0] Color Matrix Coefficient 12 for D30 (X1/64, 2's Comp.)	R/W
0x7C	CMB13	0xF7	[7:0] Color Matrix Coefficient 13 for D30 (X1/64, 2's Comp.)	R/W
0x7D	CMB21	0x13	[7:0] Color Matrix Coefficient 21 for D30 (X1/64, 2's Comp.)	R/W
0x7E	CMB22	0x25	[7:0] Color Matrix Coefficient 22 for D30 (X1/64, 2's Comp.)	R/W
0x7F	CMB23	0x07	[7:0] Color Matrix Coefficient 23 for D30 (X1/64, 2's Comp.)	R/W
0x80	CMB31	0xF2	[7:0] Color Matrix Coefficient 31 for D30 (X1/64, 2's Comp.)	R/W
0x81	CMB32	0xC7	[7:0] Color Matrix Coefficient 32 for D30 (X1/64, 2's Comp.)	R/W
0x82	CMB33	0x47	[7:0] Color Matrix Coefficient 33 for D30 (X1/64, 2's Comp.)	R/W
0x83	CMC11	0x3B	[7:0] Color Matrix Coefficient 11 for D20 (X1/64, 2's Comp.)	R/W
0x84	CMC12	0xCE	[7:0] Color Matrix Coefficient 12 for D20 (X1/64, 2's Comp.)	R/W
0x85	CMC13	0xF7	[7:0] Color Matrix Coefficient 13 for D20 (X1/64, 2's Comp.)	R/W
0x86	CMC21	0x13	[7:0] Color Matrix Coefficient 21 for D20 (X1/64, 2's Comp.)	R/W
0x87	CMC22	0x25	[7:0] Color Matrix Coefficient 22 for D20 (X1/64, 2's Comp.)	R/W
0x88	CMC23	0x07	[7:0] Color Matrix Coefficient 23 for D20 (X1/64, 2's Comp.)	R/W
0x89	CMC31	0xF2	[7:0] Color Matrix Coefficient 31 for D20 (X1/64, 2's Comp.)	R/W
0x8A	CMC32	0xC7	[7:0] Color Matrix Coefficient 32 for D20 (X1/64, 2's Comp.)	R/W
0x8B	CMC33	0x47	[7:0] Color Matrix Coefficient 33 for D20 (X1/64, 2's Comp.)	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0x8C	CMASEL	0x00	[7:5] Reserved [4] Selective Color Matrix Enable for D20/D30/D65 [3:2] Color Matrix Selection at Dark Condition 00: D65 Color Matrix Selection at Dark Condition 01: D30 Color Matrix Selection at Dark Condition 10: D20 Color Matrix Selection at Dark Condition [1] D20 Color Matrix Test Enable [0] D30 Color Matrix Test Enable	R/W
0x8D~0x8F	-	-	Reserved	-
0x90	EUGAIN	0x15	[7:0] Green Edge Upper Gain (X1/16)	R/W
0x91	EDGAIN	0x15	[7:0] Green Edge Down Gain (X1/16)	R/W
0x92	ECORE	0x44	[7:4] Green Edge Upper Coring Value [3:0] Green Edge Down Coring Value	R/W
0x93	EUCORESTRT	0x12	[7:6] Reserved [5:0] Green Edge Upper Coring Value Change Start State	R/W
0x94	EUCOREEND	0xFF	[7:0] Green Edge Upper Coring Maximum Value	R/W
0x95	EUCORESLOP	0x20	[7:0] Green Edge Upper Coring Value Change Slope	R/W
0x96	-	-	Reserved	-
0x97	EDCORESTRT	0x12	[7:6] Reserved [5:0] Green Edge Lower Coring Value Change Start State	R/W
0x98	EDCOREEND	0xFF	[7:0] Green Edge Lower Coring Maximum Value	R/W
0x99	EDCORESLOP	0x20	[7:0] Green Edge Lower Coring Value Change Slope	R/W
0x9A	EUCLIP	0x20	[7:0] Green Edge Upper Clip Value	R/W
0x9B	EDCLIP	0x20	[7:0] Green Edge Down Clip Value	R/W
0x9C	ESTART	0x13	[7:6] Reserved [5:0] Green Edge Suppress Start IllumiInfo Point	R/W
0x9D	ESLOP	0x20	[7:4] Green Edge Suppress Slope [3:0] Green Edge Suppress End Gain	R/W
0x9E	EDGLEVEL	0x00	[7:0] Green Edge Disable Value	R/W
0x9F ~ 0xA7	-	-	Reserved	-
0xA8	YGAIN	0x10	[7:6] Reserved [5:0] Luminance Stretch Gain (X1/16)	R/W
0xA9	CRGAIN	0x10	[7:6] Reserved [5:0] CR Color Saturation Gain (X1/16)	R/W
0xAA	CBGAIN	0x10	[7:6] Reserved [5:0] CB Color Saturation Gain (X1/16)	R/W
0xAB	BRTCNT	0x00	[7] Brightness Control Sign Bit (1: minus, 0: plus) [6:0] Brightness Control Value (Absolute Value)	R/W
0xAC	-	-	Reserved	-

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0xAD	IMGYOFST	0x00	[7:0] Y Offset Value @ Contrast Gain Adaptation	R/W
0xAE	HUECOS	0x40	[7] Sign Bit (0: plus, 1: minus) for Cosine [6:0] Absolute Value for Cosine (X1/64)	R/W
0xAF	HUESIN	0x00	[7] Sign Bit (0: plus, 1: minus) for Sine [6:0] Absolute Value for Sine (X1/64)	R/W
0xB0	YTOP	0xFF	[7:0] Luminance output Top Clip Value	R/W
0xB1	YBOT	0x00	[7:0] Luminance output Bottom Clip Value	R/W
0xB2	CRTOP	0xFF	[7:0] CR Output Top Clip Value	R/W
0xB3	CRBOT	0x00	[7:0] CR Output Bottom Clip Value	R/W
0xB4	CBTOP	0xFF	[7:0] CB Output Top Clip Value	R/W
0xB5	CBBOT	0x00	[7:0] CB Output Bottom Clip Value	R/W
0xB6	IEFCT	0x00	[7] Sepia Effect Enable [6] B/W Effect Enable [5] Inverted B/W Effect Enable [4] Inversion Effect Enable [3] Embossing Effect Enable [2] Sketch Effect Enable [1:0] Reserved	R/W
0xB7	CBEFCT	0x60	[7:0] CB Value @ Image Effect	R/W
0xB8	CREFCT	0xA0	[7:0] CR Value @ Image Effect	R/W
0xB9	GSTRT	0x13	[7:6] Reserved [5:0] Color Suppression Change Start IllumiInfo Point	R/W
0xBA	GSLOP	0x10	[7:4] Color Suppression Change Slope [3:0] Color Suppression End Gain	R/W
0xBB~BD	-	-	Reserved	-
0xBE	DGCTRL	0x0C	[7:4] Reserved [3] Digital gain enable [2] AE gain selection 1: Digita gain is set by AE 0: Digital gain is se by DGAIN [BLKSEL: 0x04, ADDR: 0xBF] [1:0] AE gain delay count for AE synchronization	R/W
0xBF	DGAIN	0x20	[7:0] Digital gain (X1/32)	R/W
0xC0	WDATH	0x34	[7:6] MSB of Window Horizontal Start [5:4] MSB of Window Horizontal Width [3] MSB of Window Vertical Start [2] MSB of Window Vertical Width [1:0] Reserved	R/W
0xC1	WHSRTL	0x00	[7:0] LSB of Window Horizontal Start Horizontal Start = {WDATH[7:6],WHSRTL}	R/W
0xC2	WHWIDL	0xFF	[7:0] LSB of Window Horizontal Width Horizontal Width = {WDATH[5:4],WHWIDL}	R/W
0xC3	WVSRTL	0x00	[7:0] LSB of Window Vertical Start Vertical Start = {WDATH[3],WVSRTL}	R/W

BANK [0x04]: IDP Block

Address	Name	Default	Description	Mode
0xC4	WVWIDL	0xFF	[7:0] LSB of Window Vertical Width Vertical Width = {WDATH[2],WVWIDL}	R/W
0xC5 ~ 0xCA	-	-	Reserved	-
0xCB	EXTHXSYNK	0x00	[7:0] Count value to extend Hsync	R/W
0xCC ~ 0xD8	-	-	Reserved	-
0xD9	ENHCTRL1	0x09	[7:0] Minimum Threshold of LPF	R/W
0xDA	ENHCTRL2	0x10	[7:0] Maximum Threshold of LPF	R/W
0xDB	ENHCTRL3	0x10	[7:6] Reserved [5:0] Start Value for IllumiInfo Slope Control of LPF	R/W
0xDC	ENHCTRL4	0x20	[7:6] Reserved [5:0] Increasing Slope Value of LPF	R/W
0xDD	-	-	Reserved	-
0xDE	NOIZCTRL	0x90	[7] Chrominance Filter Enable [6] Cb/Cr Horizontal Filter Selection 0: Cb/Cr Median Filter 1: Cb/Cr Suppression @ Edge Region [5] Window Size Selection of LPF 0: Wide Window 1: Narrow Window [4] Sigma Filter Enable of LPF [3:0] Reserved	R/W
0xDF~ 0xE4	-	-	Reserved	-
0xE5	MEMSPDA	0x15	[7:0] Memory Speed Control A	R/W
0xE6	MEMSPDB	0x02	[3:0] Memory Speed Control B	R/W
0xE7	MEMSPDC	0x04	[7:0] Memory Speed Control C	R/W
0xE8	TSTFUN	0x00	[7] Memory Test Mode [6] Value Clip Test Mode [5] Fix Value Test Mode [4] Ramp Test Mode [3] Vertical Stripe Pattern Test Mode [2] Color Bar Pattern Test Mode [1] Reserved [0] Value Clip Test Mode Selection for LSB 8 bits	R/W
0xE9	TSTDATH	0x00	[7:2] Reserved [1:0] MSB of Test Clip Value	R/W
0xEA	TSTDATL	0x00	[7:0] LSB of Test Clip Value TSTDAT = {TSTDATH[1:0],TSTDATL}	R/W
0xEB	HxFNT	0x00	[7:0]: Subtraction Value for Maximum FNT When HxDMYEN Enable	R/W
0xEC	HxBCK	0x00	[7:0]: Maximum Count Value to Extend Hsync When HxDMYEn Enable	R/W
0xED~0xEF	-	-	Reserved	-

5. Revision History

Table 15. Revision history

Version	Major Revision Items & Remarks	Issued Data
SIV121C-DSPRE(101205)	Initial release of Preliminary document	2010-12-05
SIV121C-DSPRE(101215)	Updated Reference Circuit	2010-12-15
SIV121C-DSPRE(110121)	Updated Register at PMU block	2011-01-21
SIV121C-DSPRE(110126)	Updated Key specifications	2011-01-26
SIV121C-DSPRE(110215)	Updated Key specifications, reference circuit and Registers.	2011-02-15

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