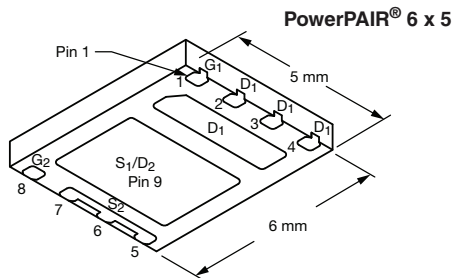


## Dual N-Channel 30 V (D-S) MOSFETs

PRODUCT SUMMARY				
	V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω) (Max.)	I <sub>D</sub> (A) <sup>g</sup>	Q <sub>g</sub> (Typ.)
Channel-1	30	0.00640 at V <sub>GS</sub> = 10 V	16 <sup>a</sup>	7.2 nC
		0.01000 at V <sub>GS</sub> = 4.5 V	16 <sup>a</sup>	
Channel-2	30	0.00137 at V <sub>GS</sub> = 10 V	40 <sup>a</sup>	30.1 nC
		0.00194 at V <sub>GS</sub> = 4.5 V	40 <sup>a</sup>	



**Ordering Information:**  
SiZ914DT-T1-GE3 (Lead (Pb)-free and Halogen-free)

### FEATURES

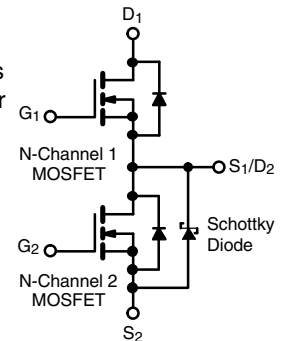
- TrenchFET<sup>®</sup> Gen IV Power MOSFETs
- 100 % R<sub>g</sub> and UIS Tested
- Material categorization:  
For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- CPU Core Power
- Computer/Server Peripherals
- Synchronous Buck Converter
- POL
- Telecom DC/DC



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
Parameter	Symbol	Channel-1	Channel-2	Unit	
Drain-Source Voltage	V <sub>DS</sub>	30		V	
Gate-Source Voltage	V <sub>GS</sub>	+ 20, - 16		V	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	16 <sup>a</sup>	40 <sup>a</sup>	A
		T <sub>C</sub> = 70 °C	16 <sup>a</sup>	40 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	16 <sup>a, b, c</sup>	40 <sup>a, b, c</sup>	
		T <sub>A</sub> = 70 °C	15.5 <sup>b, c</sup>	38.8 <sup>b, c</sup>	
Pulsed Drain Current (t = 100 μs)	I <sub>DM</sub>	80	100	A	
Continuous Source Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	19	28	A
		T <sub>A</sub> = 25 °C	3.25 <sup>b, c</sup>	4.3 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	10	20	A	
Single Pulse Avalanche Energy	E <sub>AS</sub>	5	20	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	22.7	100	W
		T <sub>C</sub> = 70 °C	14.5	64	
		T <sub>A</sub> = 25 °C	3.9 <sup>b, c</sup>	5.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	2.5 <sup>b, c</sup>	3.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C	
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260		°C	

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Channel-1		Channel-2		Unit
		Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient <sup>b, f</sup>	R <sub>thJA</sub>	25	32	19	24	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	4.4	5.5	1	1.25	°C/W

Notes:

- Package limited
- Surface mounted on 1" x 1" FR4 board.
- t = 10 s.
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAIR is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.
- Maximum under steady state conditions is 62 °C/W for channel-1 and 55 °C/W for channel-2.
- T<sub>C</sub> = 25 °C.

SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)								
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit		
<b>Static</b>								
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30			V	
		$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-2	30				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.2		2.4	V	
		$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-2	1		2.4		
Gate Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}, -16\text{ V}$	Ch-1			$\pm 100$	nA	
			Ch-2			$\pm 100$		
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1			1	$\mu\text{A}$	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-2		60	240		
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1				5	mA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-2		0.5		5	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	20			A	
		$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-2	25				
Drain-Source On-State Resistance <sup>b</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 19\text{ A}$	Ch-1		0.00530	0.00640	$\Omega$	
		$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		0.00114	0.00137		
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$	Ch-1		0.00800	0.01000		
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-2		0.00155	0.00194		
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 19\text{ A}$	Ch-1		55		S	
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		68			
<b>Dynamic<sup>a</sup></b>								
Input Capacitance	$C_{iss}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		1208		pF	
			Ch-2		5603			
Output Capacitance	$C_{oss}$	Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		375		pF	
			Ch-2		2202			
Reverse Transfer Capacitance	$C_{rss}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		30		pF	
			Ch-2		168			
$C_{rss}/C_{iss}$ Ratio		Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1		0.025	0.050	pF	
			Ch-2		0.032	0.064		
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1		17	26	nC	
		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2		66	99		
Gate-Source Charge	$Q_{gs}$	Channel-1 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		7.2	11	nC	
			Ch-2		30.1	45.2		
Gate-Drain Charge	$Q_{gd}$	Channel-2 $V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$	Ch-1		3.6		nC	
			Ch-2		10.9			
Output Charge	$Q_{oss}$	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	Ch-1		0.94		nC	
			Ch-2		3.8			
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	Ch-1	0.5	2.5	5	$\Omega$	
			Ch-2	0.2	1	2		

## Notes:

- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .



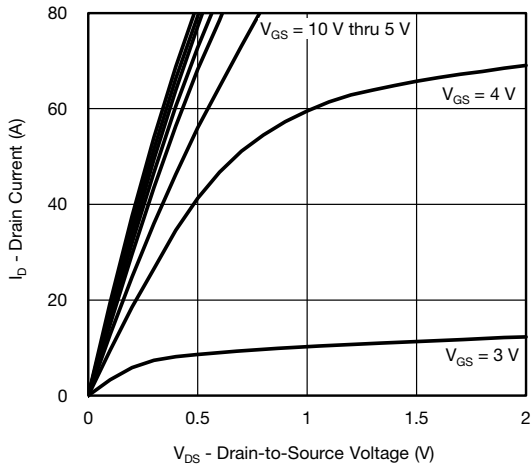
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Dynamic<sup>a</sup></b>							
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		16	24	ns
Rise Time	$t_r$		Ch-2		40	60	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		11	20	
Fall Time	$t_f$		Ch-2		127	190	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		15	23	
Rise Time	$t_r$		Ch-2		40	60	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		5	10	
Fall Time	$t_f$		Ch-2		19	29	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	20	
Rise Time	$t_r$		Ch-2		12	20	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		10	20	
Fall Time	$t_f$		Ch-2		30	45	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		20	30	
Rise Time	$t_r$		Ch-2		35	53	
Turn-Off Delay Time	$t_{d(off)}$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 1.5\ \Omega$ $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\ \Omega$	Ch-1		5	10	
Fall Time	$t_f$		Ch-2		7	14	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	Ch-1			40	A
Pulse Diode Forward Current ( $t = 100\ \mu\text{s}$ )	$I_{SM}$		Ch-2			40	
Body Diode Voltage	$V_{SD}$	$I_S = 10\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-1		0.8	1.2	V
		$I_S = 2\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-2		0.33	0.42	
Body Diode Reverse Recovery Time	$t_{rr}$	Channel-1 $I_F = 10\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		15	23	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$		Ch-2		62	93	
Reverse Recovery Fall Time	$t_a$	Channel-2 $I_F = 10\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	Ch-1		4	8	nC
			Ch-2		96	144	
Reverse Recovery Rise Time	$t_b$		Ch-1		9		ns
			Ch-2		30.5		
			Ch-1		6		
			Ch-2		31.5		

Notes:

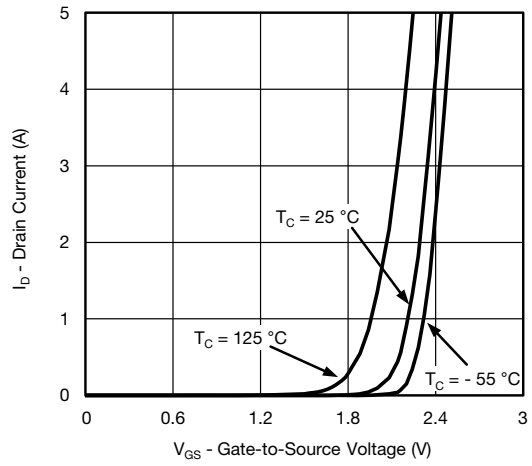
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

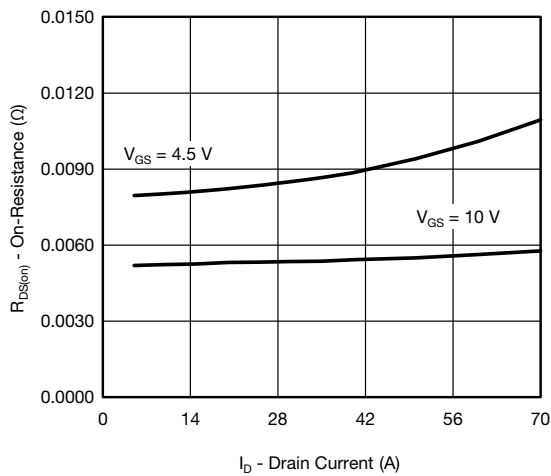
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



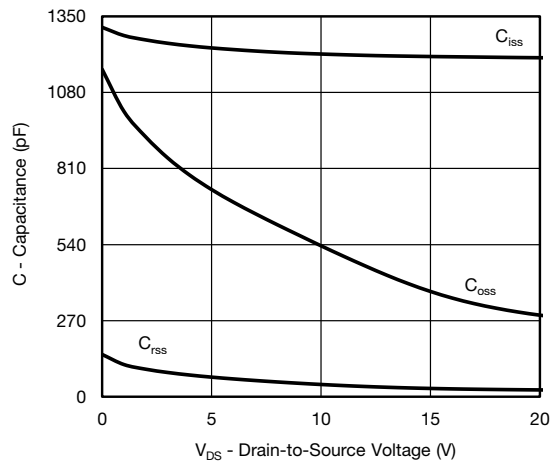
**Output Characteristics**



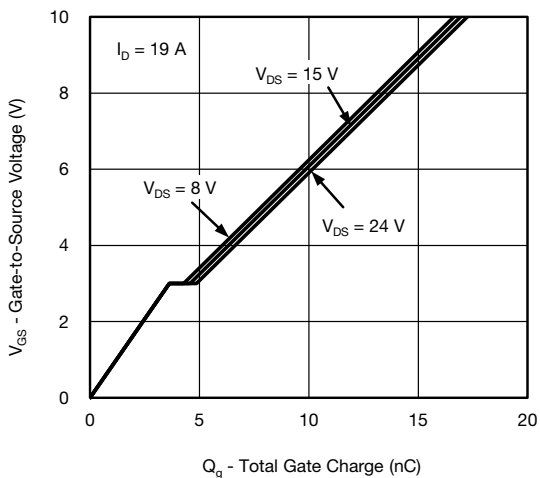
**Transfer Characteristics**



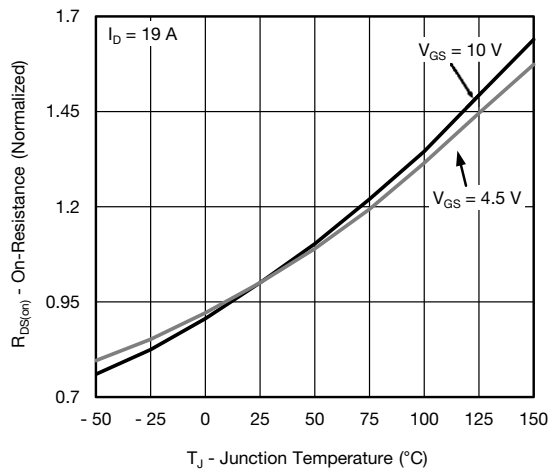
**On-Resistance vs. Drain Current**



**Capacitance**

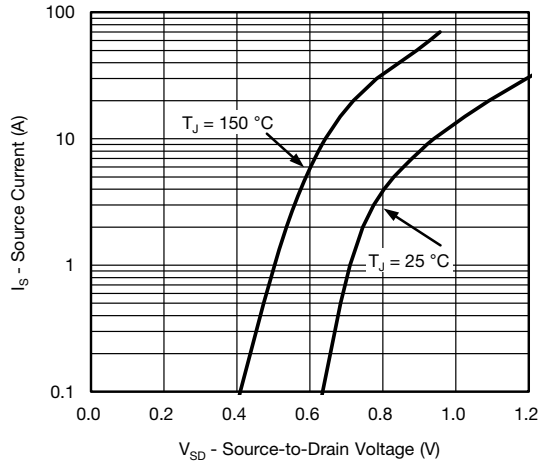


**Gate Charge**

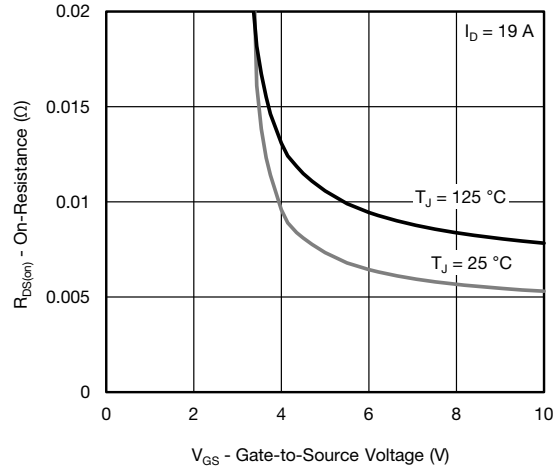


**On-Resistance vs. Junction Temperature**

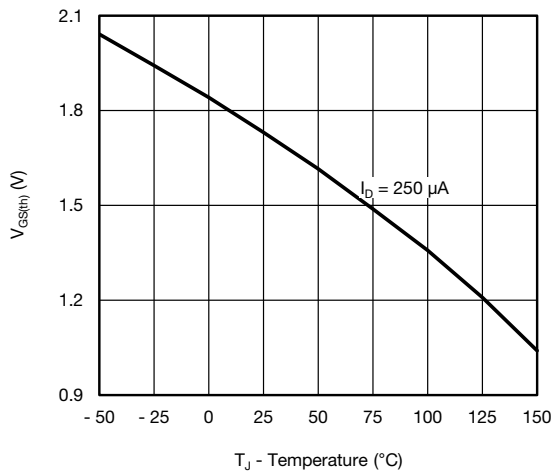
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



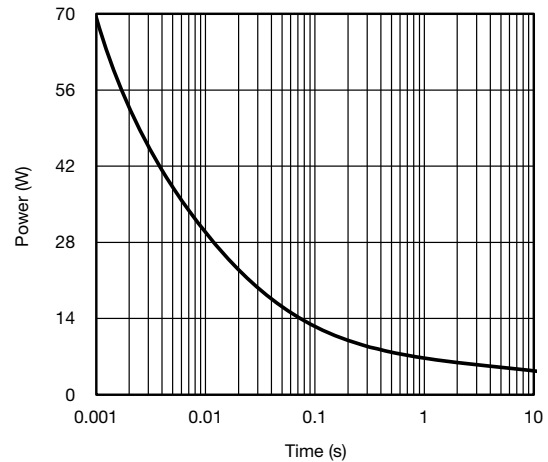
Source-Drain Diode Forward Voltage



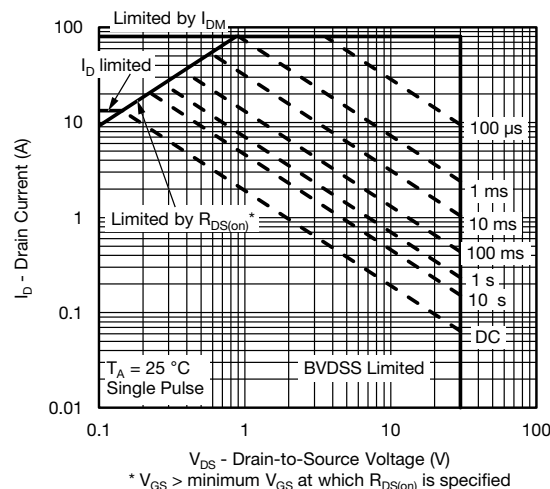
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

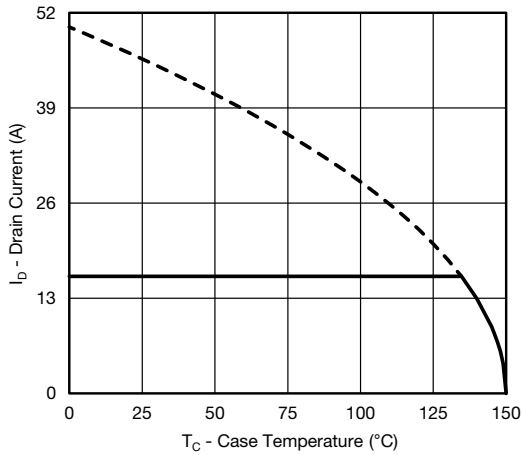


Single Pulse Power, Junction-to-Ambient

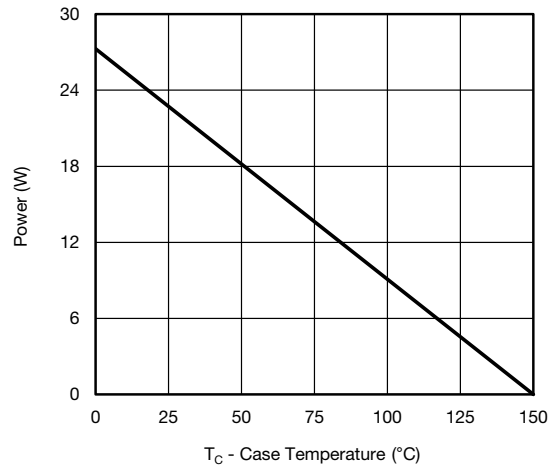


Safe Operating Area, Junction-to-Ambient

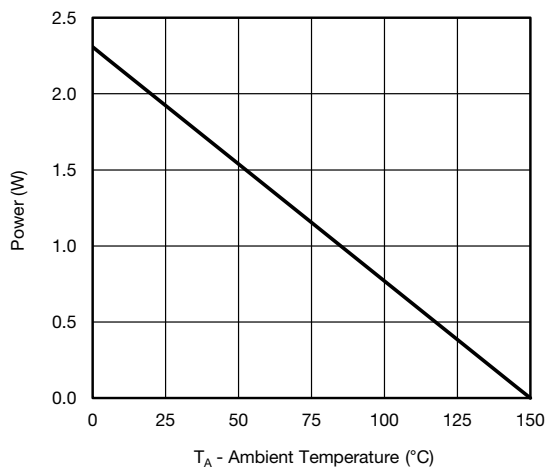
## CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating\***



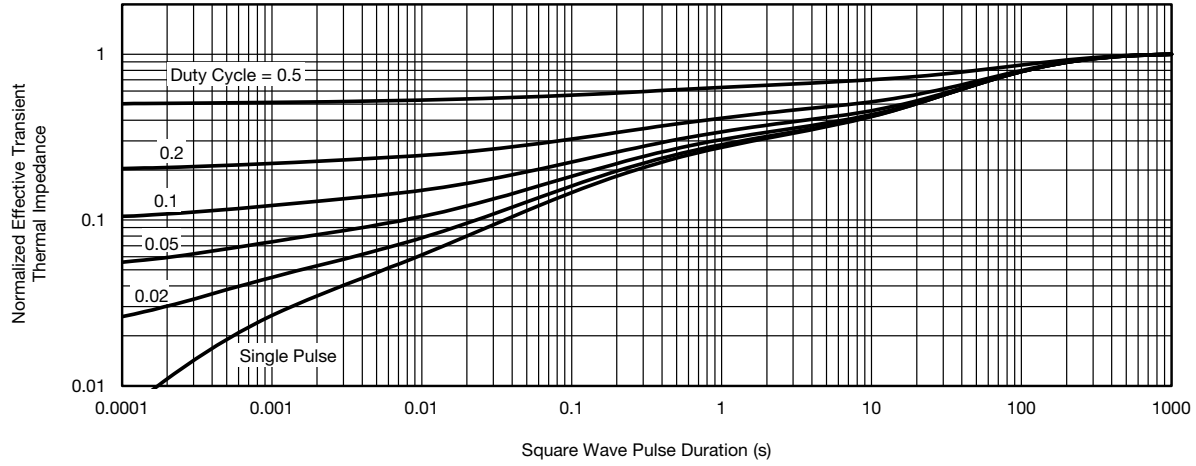
**Power, Junction-to-Case**



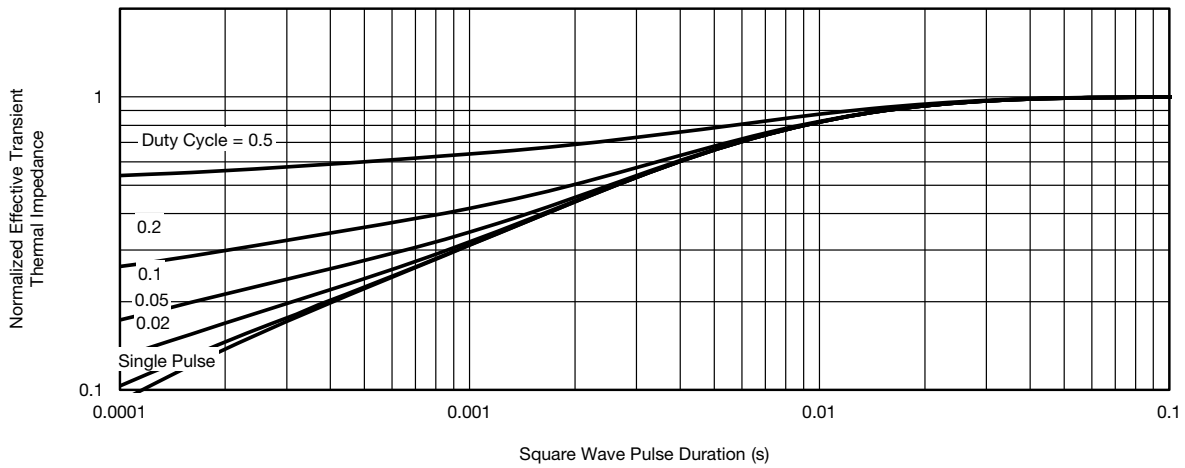
**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max.)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-1 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

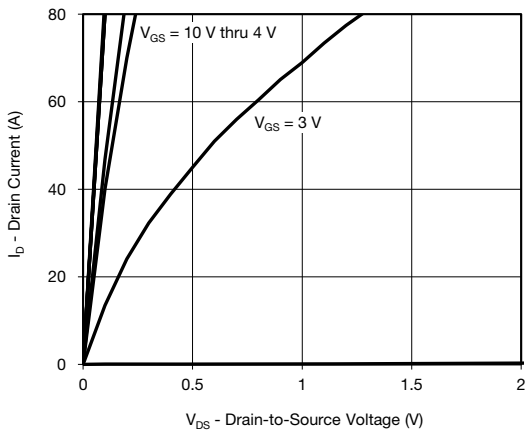


**Normalized Thermal Transient Impedance, Junction-to-Ambient**

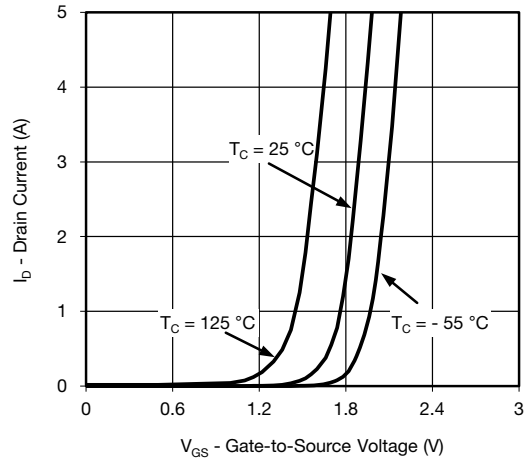


**Normalized Thermal Transient Impedance, Junction-to-Case**

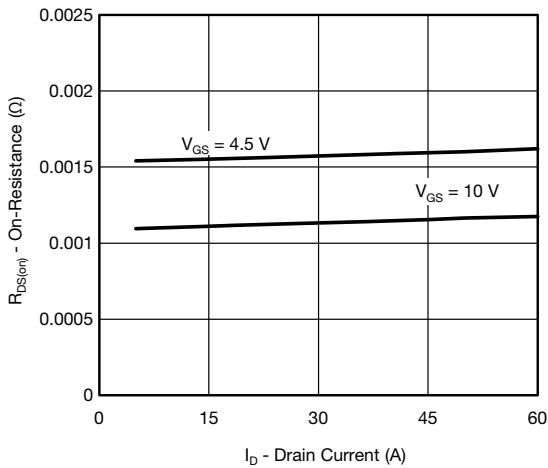
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



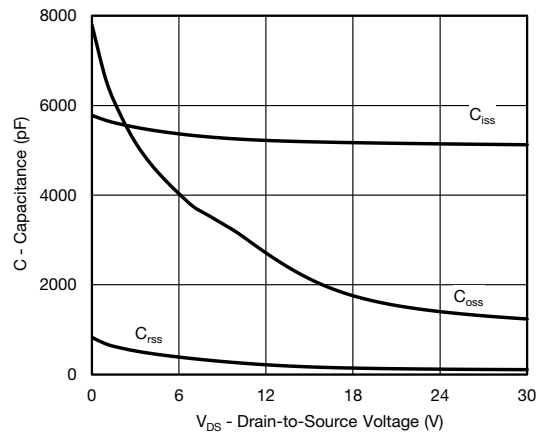
**Output Characteristics**



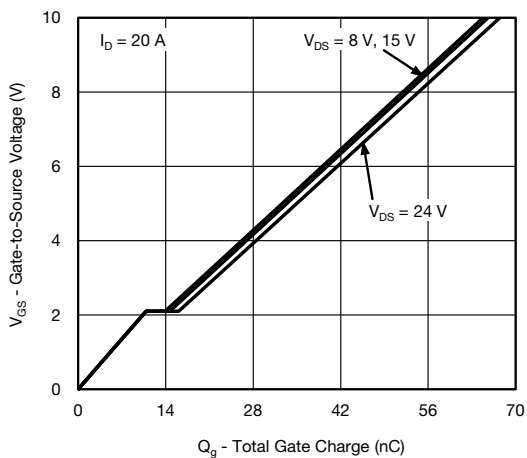
**Transfer Characteristics**



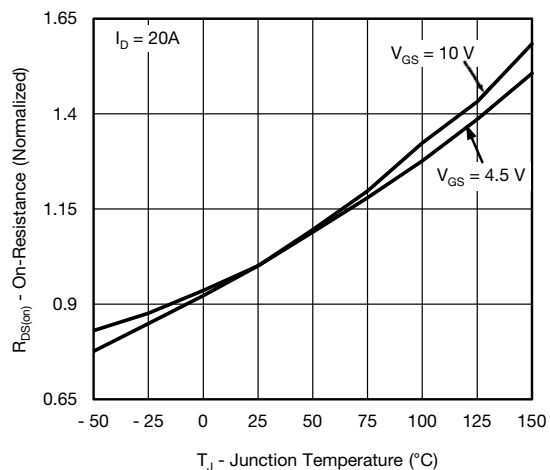
**On-Resistance vs. Drain Current**



**Capacitance**



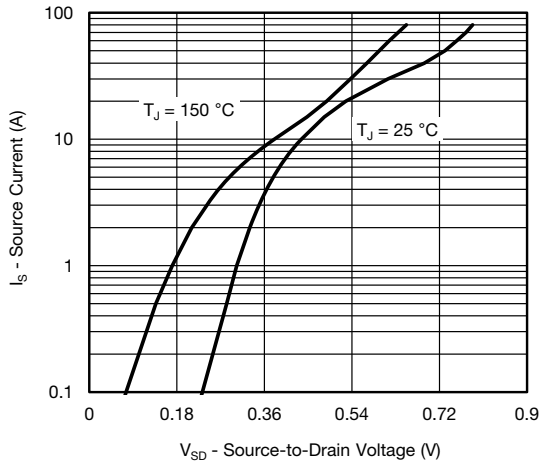
**Gate Charge**



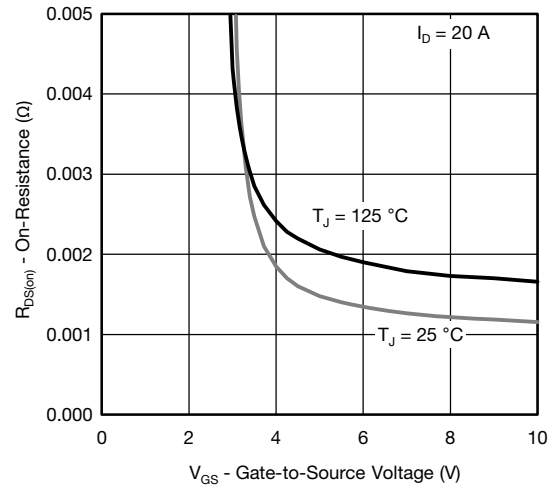
**On-Resistance vs. Junction Temperature**



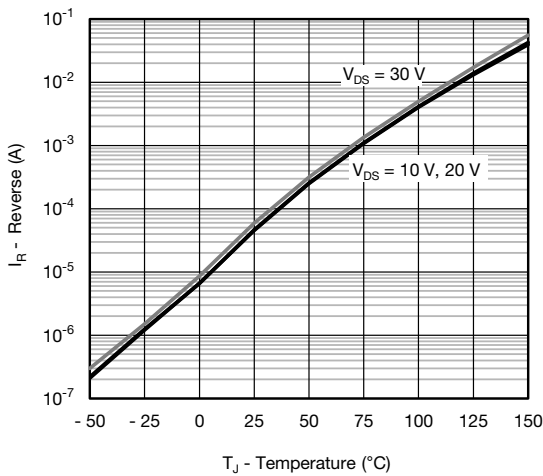
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



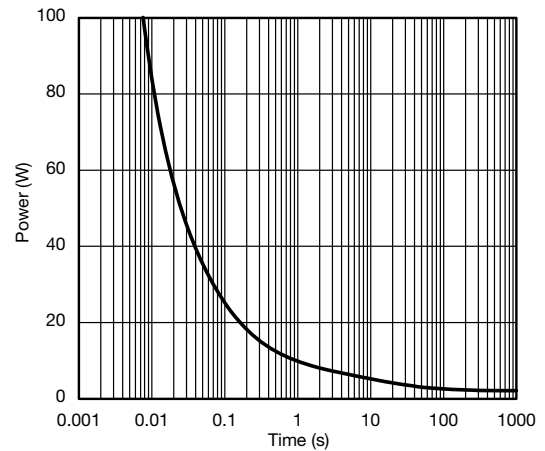
Source-Drain Diode Forward Voltage



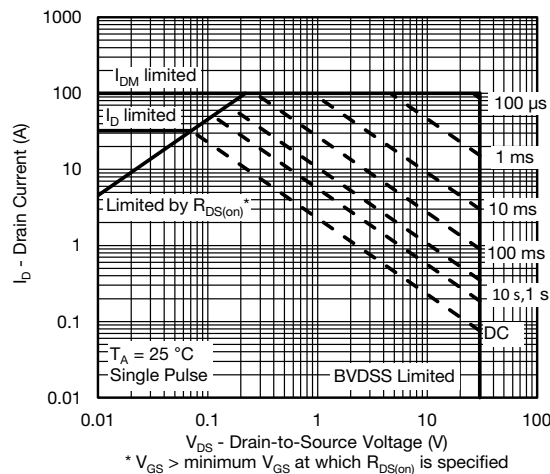
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)

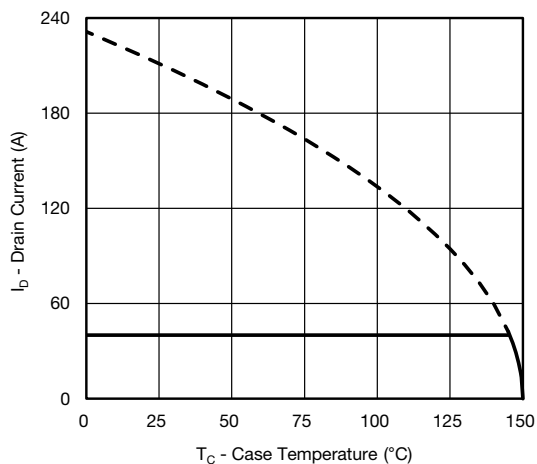


Single Pulse Power, Junction-to-Ambient

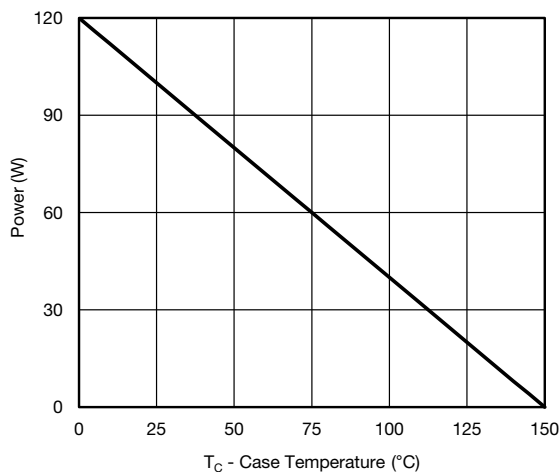


Safe Operating Area, Junction-to-Ambient

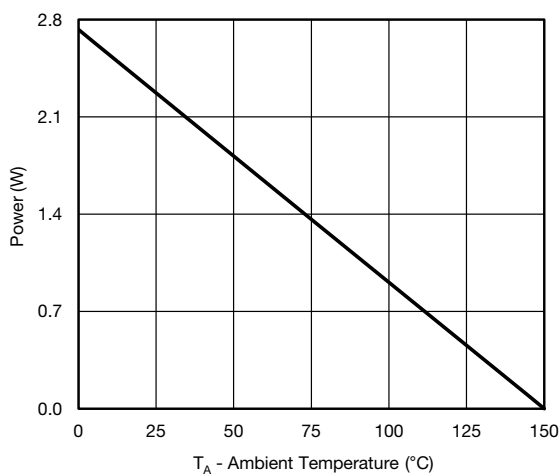
## CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



**Current Derating\***



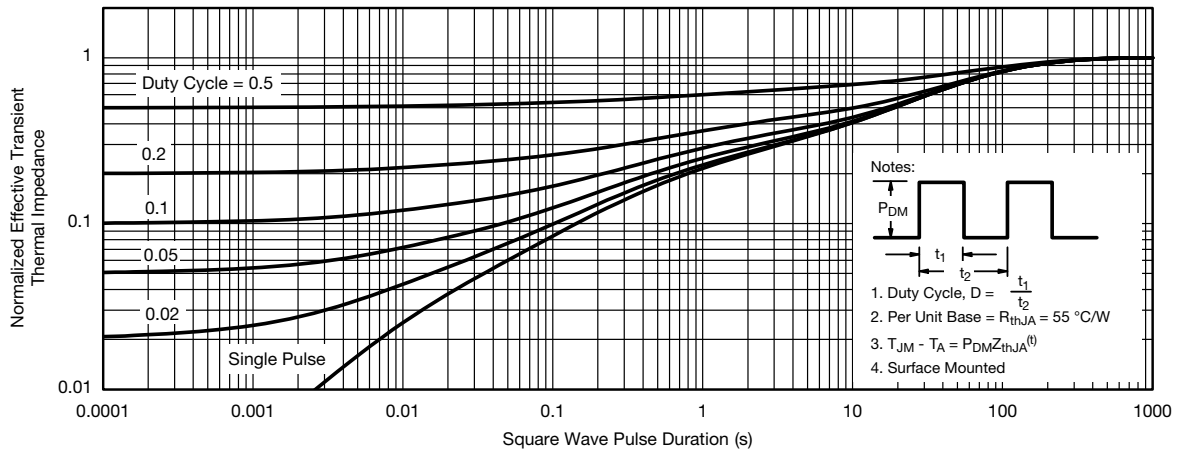
**Power, Junction-to-Case**



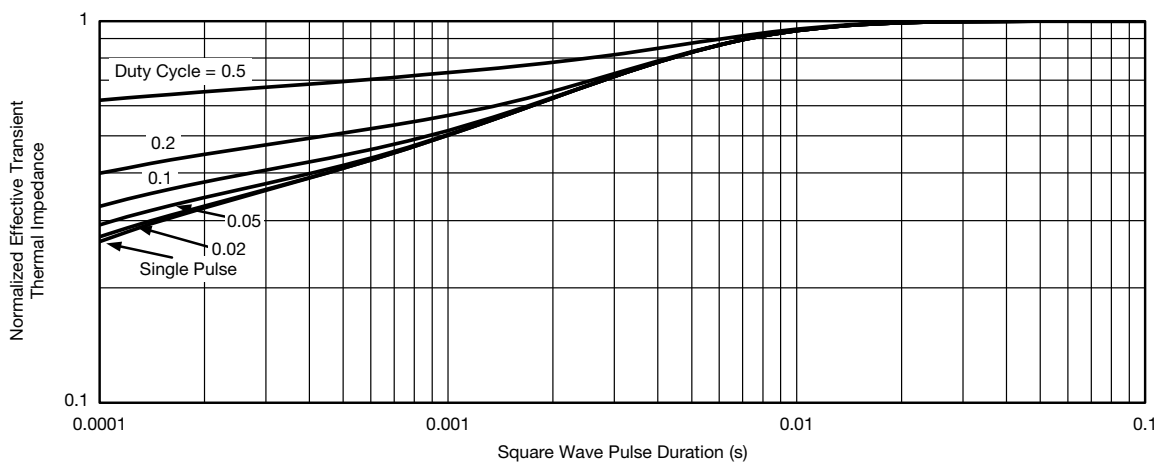
**Power, Junction-to-Ambient**

\* The power dissipation P<sub>D</sub> is based on T<sub>J(max.)</sub> = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**CHANNEL-2 TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?62905](http://www.vishay.com/ppg?62905).



# PowerPAIR® 6 x 5 Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	-	0.10	0.000	-	0.004
A3	0.15	0.20	0.25	0.006	0.007	0.009
b	0.43	0.51	0.61	0.017	0.020	0.024
b1	0.25 BSC			0.010 BSC		
D	4.90	5.00	5.10	0.192	0.196	0.200
D1	3.75	3.80	3.85	0.148	0.150	0.152
E	5.90	6.00	6.10	0.232	0.236	0.240
E1 Option AA (for W/B)	2.62	2.67	2.72	0.103	0.105	0.107
E1 Option AB (for BWL)	2.42	2.47	2.52	0.095	0.097	0.099
E2	0.87	0.92	0.97	0.034	0.036	0.038
e	1.27 BSC			0.050 BSC		
K Option AA (for W/B)	0.45 typ.			0.018 typ.		
K Option AB (for BWL)	0.65 typ.			0.025 typ.		
K1	0.66 typ.			0.025 typ.		
L	0.33	0.43	0.53	0.013	0.017	0.020
L3	0.23 BSC			0.009 BSC		
z	0.34 BSC			0.013 BSC		
ECN: T14-0782-Rev. C, 22-Dec-14						
DWG: 6005						



# Recommended Minimum PAD for PowerPAIR® 6 x 5



Dimensions in millimeters (inch)

**Note**

- Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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