KODENSHI AUK

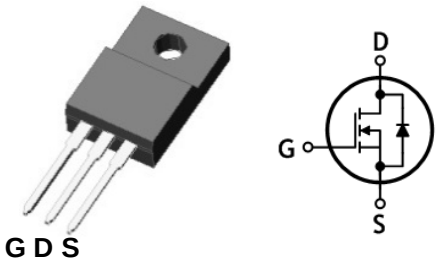
SJMN088R65FD

Super Junction MOSFET

N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: V_{DS}=700V (@T_J=150°C)
- Low drain-source On resistance: $R_{DS(on)}$=0.088Ω (Max.)
- Ultra low gate charge: Qg=76nC(Typ.)
- RoHS compliant device
- 100% avalanche tested

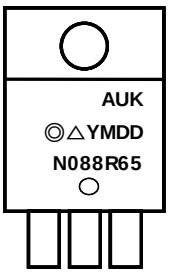


TO-220F-3L

Ordering Information

Part Number	Marking	Package
SJMN088R65FD	N088R65	TO-220F-3L

Marking Information



Column 1: Manufacturer
Column 2: Production Information
e.g.) ◎△YMDD
-. ◎△: Factory Management Code
-. YMDD: Date Code (Year, Month, Daily)
Column 3: Device Code

Absolute maximum ratings (T_C=25°C unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V_{DSS}		650	V
Gate-source voltage	V_{GSS}		±30	V
Drain current (DC) (Note 1)	I_D	T_c=25°C	40	A
		T_c=100°C	25	A
Drain current (Pulsed) (Note 1)	I_{DM}		160	A
Single pulsed avalanche energy (Note 2)	E_{AS}		720	mJ
Repetitive avalanche current (Note 1)	I_{AR}		12	A
Repetitive avalanche energy (Note 1)	E_{AR}		4.5	mJ
Power dissipation	P_D		45	W
Diode dv/ dt ruggedness (Note 3)	dv/ dt		4.5	V/ ns
MOSFET dv/ dt ruggedness (Note 4)	dv/ dt		50	V/ ns
Junction temperature	T_J		150	°C
Storage temperature range	T_{stg}		-55~150	°C

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.78	°C/ W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	I_D=250uA, V_{GS}=0	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	I_D=250uA, V_{DS}=V_{GS}	2	3	4	V
Drain-source cut-off current	I_{DSS}	V_{DS}=650V, V_{GS}=0V	-	-	1	uA
		V_{DS}=650V, T_J=125°C	-	-	100	uA
Gate leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±30V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=15.4A	-	0.072	0.088	Ω
Input capacitance	C_{iss}	V_{DS}=50V, V_{GS}=0V, f=1MHz	-	3280	-	pF
Output capacitance	C_{oss}		-	256	-	
Reverse transfer capacitance	C_{rss}		-	16	-	
Turn-on delay time (Note 5)	$t_{d(on)}$	V_{DS}=400V, I_D=15.4A, R_G=25Ω	-	45	-	ns
Rise time (Note 5)	t_r		-	85	-	
Turn-off delay time (Note 5)	$t_{d(off)}$		-	16	-	
Fall time (Note 5)	t_f		-	180	-	
Total gate charge (Note 6)	Q_g	V_{DS}=480V, V_{GS}=10V, I_D=30.8A	-	76	-	nC
Gate-source charge (Note 6)	Q_{gs}		-	20	-	
Gate-drain charge (Note 6)	Q_{gd}		-	24	-	
Gate plateau voltage (Note 6)	$V_{plateau}$		-	5.5	-	V

Source-Drain Diode Ratings and Characteristics (T_C=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	40	A
Source current (Pulsed)	I_{SM}		-	-	160	A
Forward voltage	V_{SD}	V_{GS}=0V, I_S=40A	-	-	1.5	V
Reverse recovery time (Note 5, 6)	t_{rr}	I_S=15.4A, V_{GS}=0V, dI_S/dt=100A/us	-	380	-	ns
Reverse recovery charge (Note 5, 6)	Q_{rr}		-	6.08	-	uC

Note:
1. Calculated continuous current based on maximum allowable junction temperature
2. L=10mH, I_{AS}=12A, V_{DD}=90V, Starting T_J=25°C
3. I_S≤15.4A, V_{DS}≤400V, dI_S/dt≤100A/us, T_J=25°C
4. V_{DS}≤400V, T_J=25°C
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width≤300us, Duty cycle≤2%

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

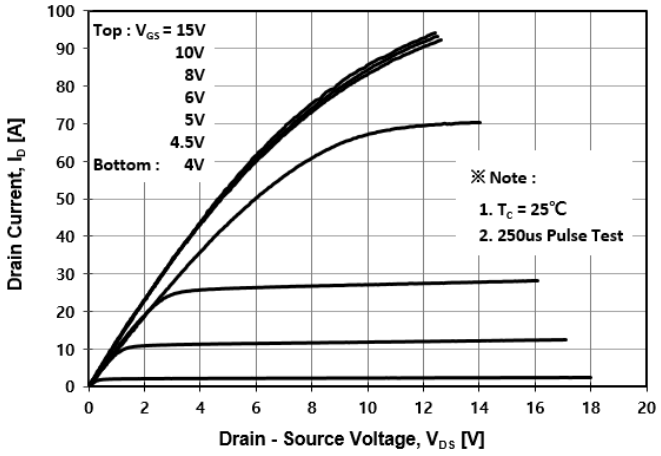


Fig. 2 Typical Transfer Characteristics

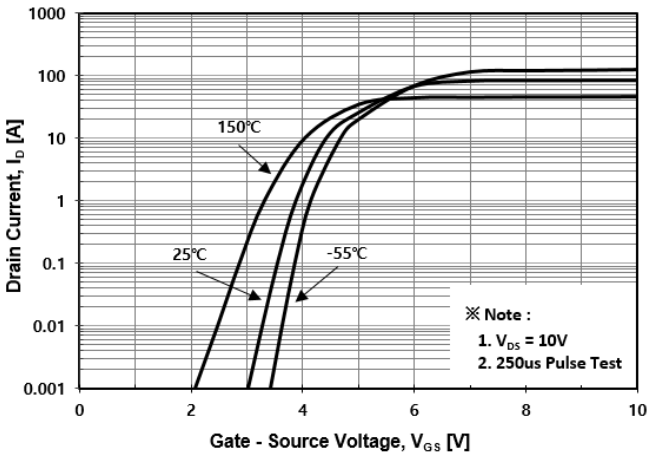


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

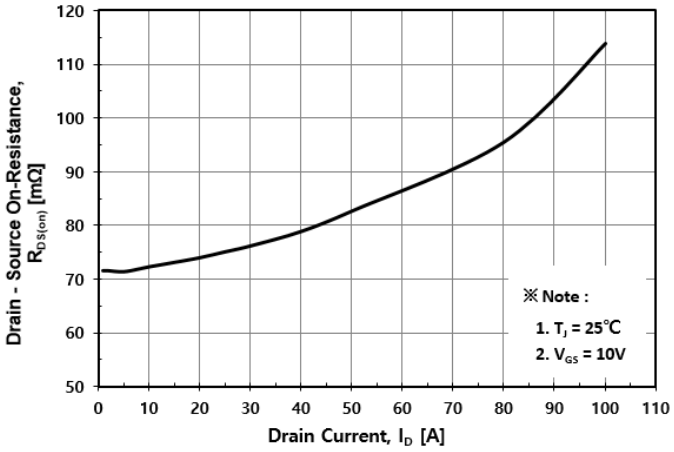


Fig. 4 Body Diode Forward Voltage Variation with Source Current

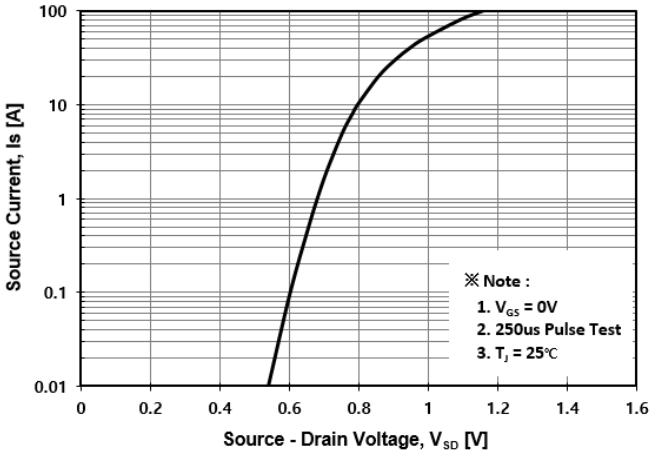


Fig. 5 Typical Capacitance Characteristics

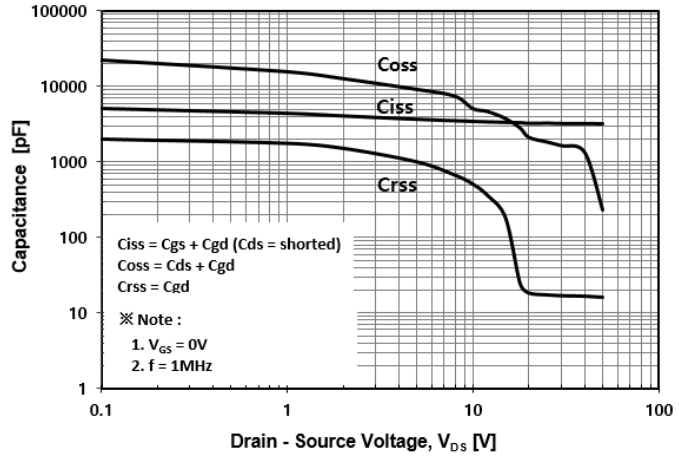


Fig. 6 Typical Total Gate Charge Characteristics

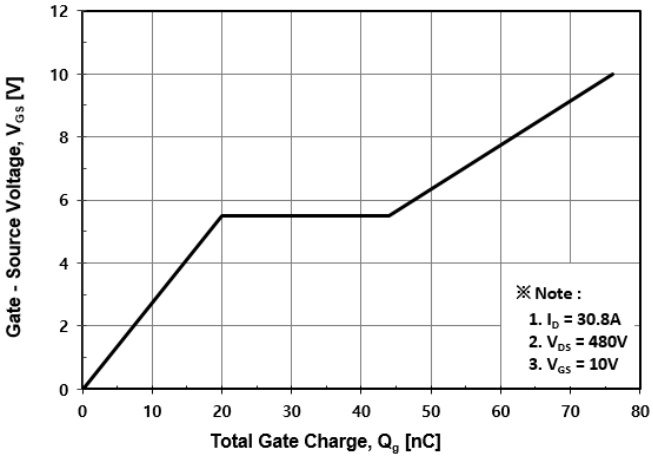


Fig. 7 Breakdown Voltage Variation vs. Temperature

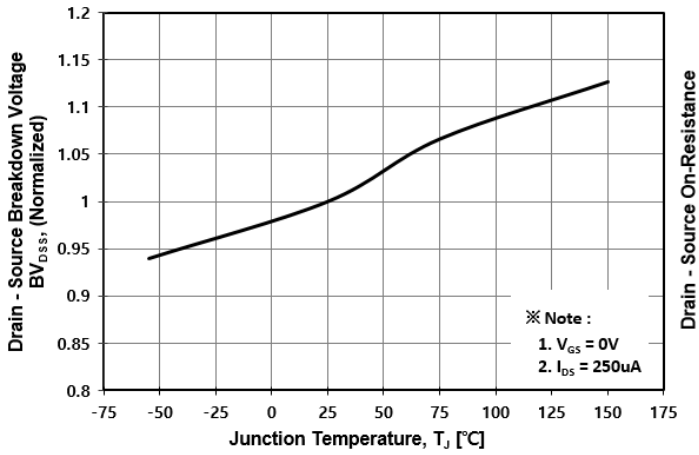


Fig. 8 On-Resistance Variation vs. Temperature

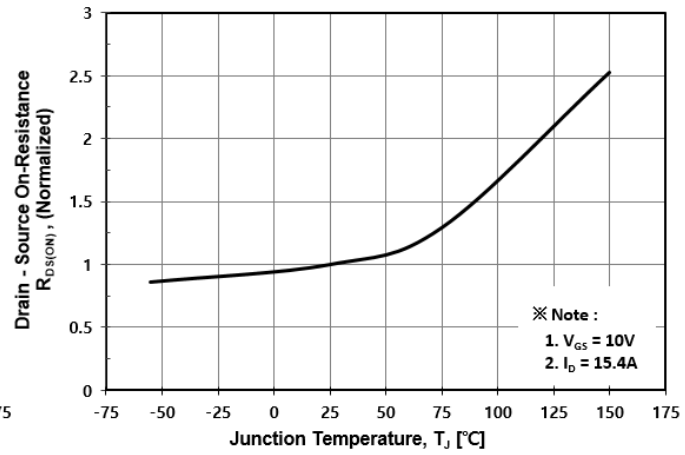


Fig. 9 Maximum Drain Current vs. Case Temperature

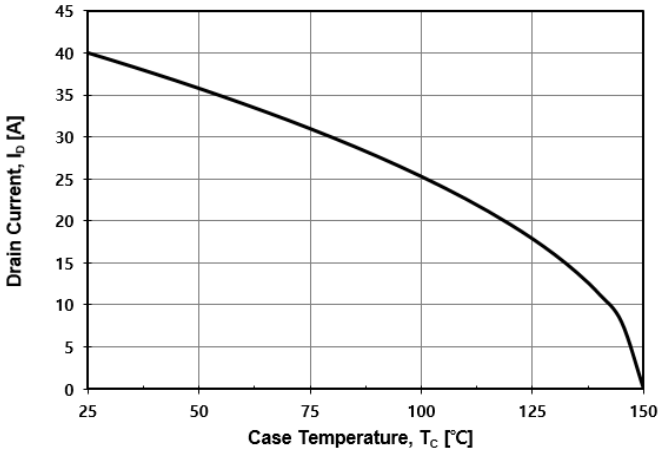


Fig. 10 Maximum Safe Operating Area

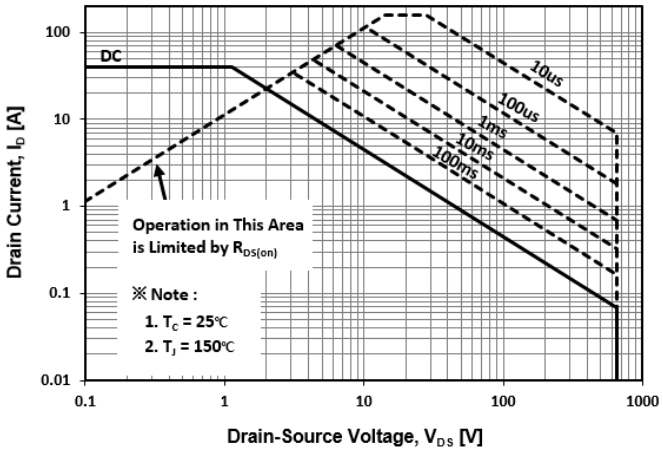


Fig. 11 Transient Thermal Impedance

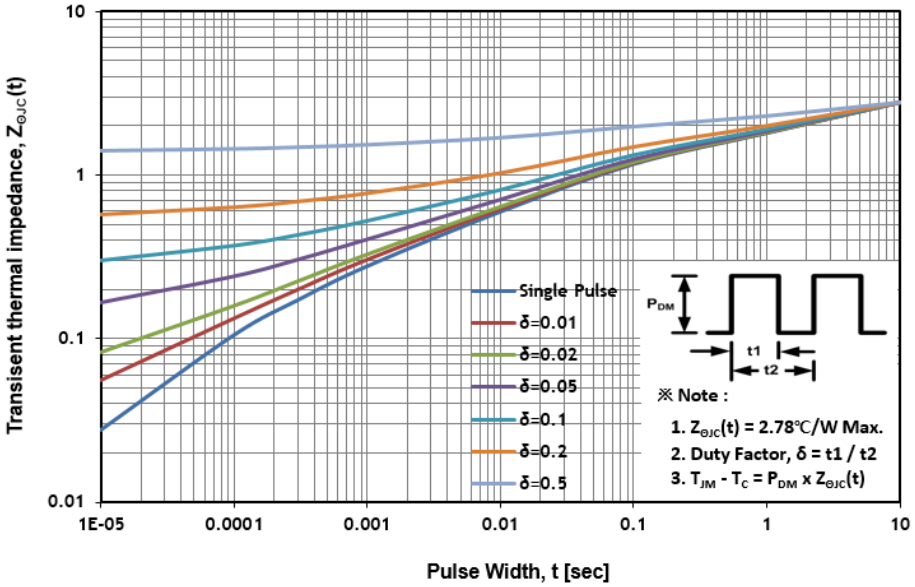
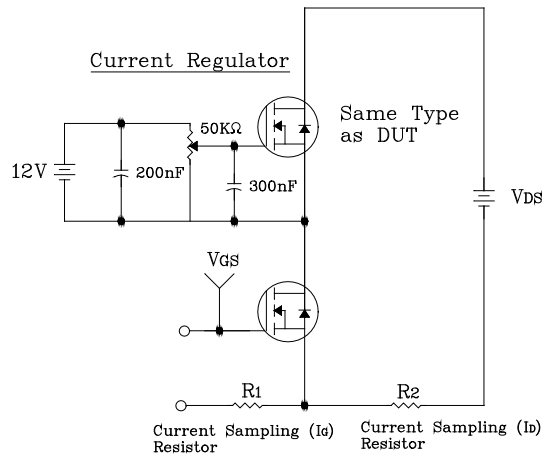


Fig. 12 Gate Charge Test Circuit & Waveform



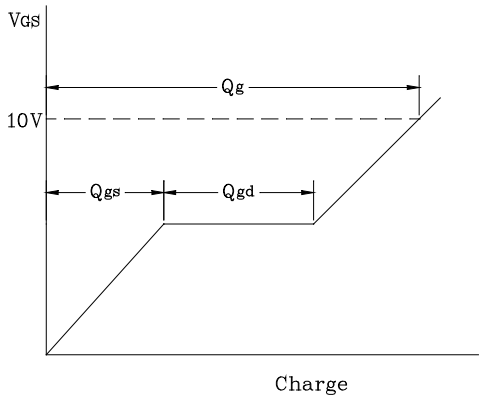
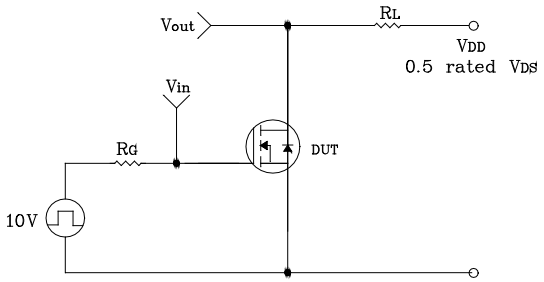


Fig. 13 Resistive Switching Test Circuit & Waveform



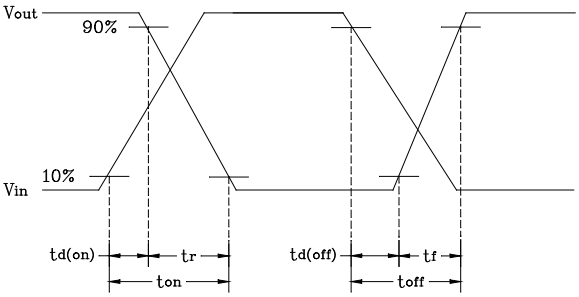
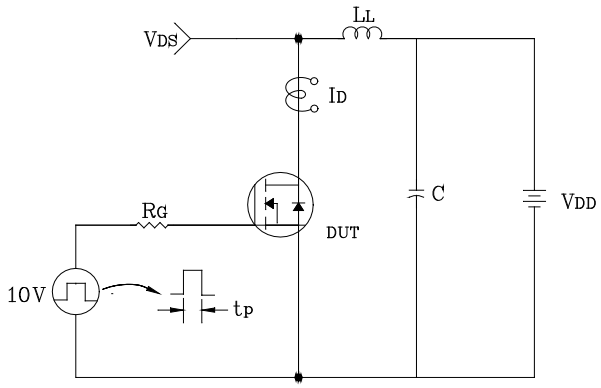


Fig. 14 E_{AS} Test Circuit & Waveform



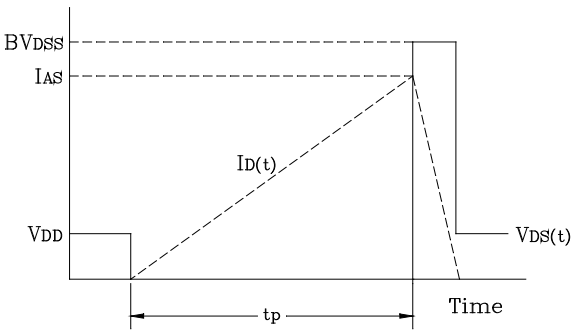
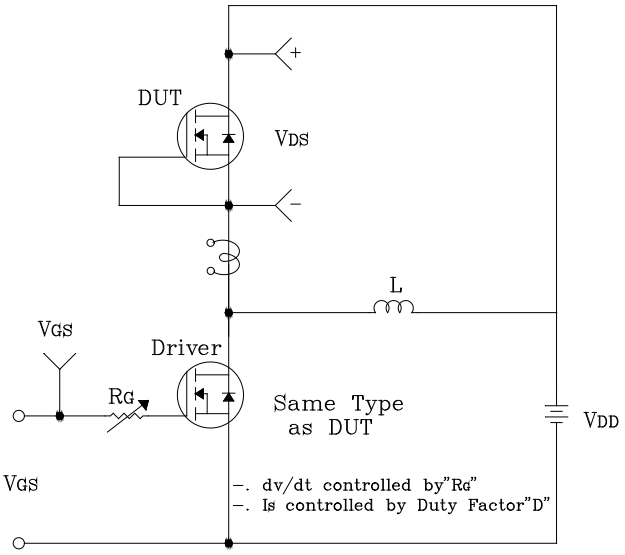
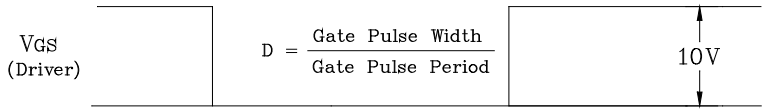
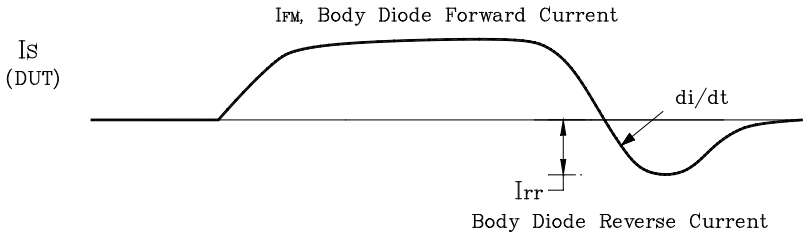
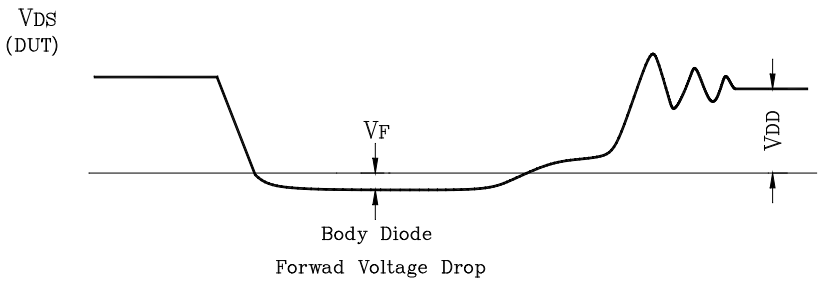


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

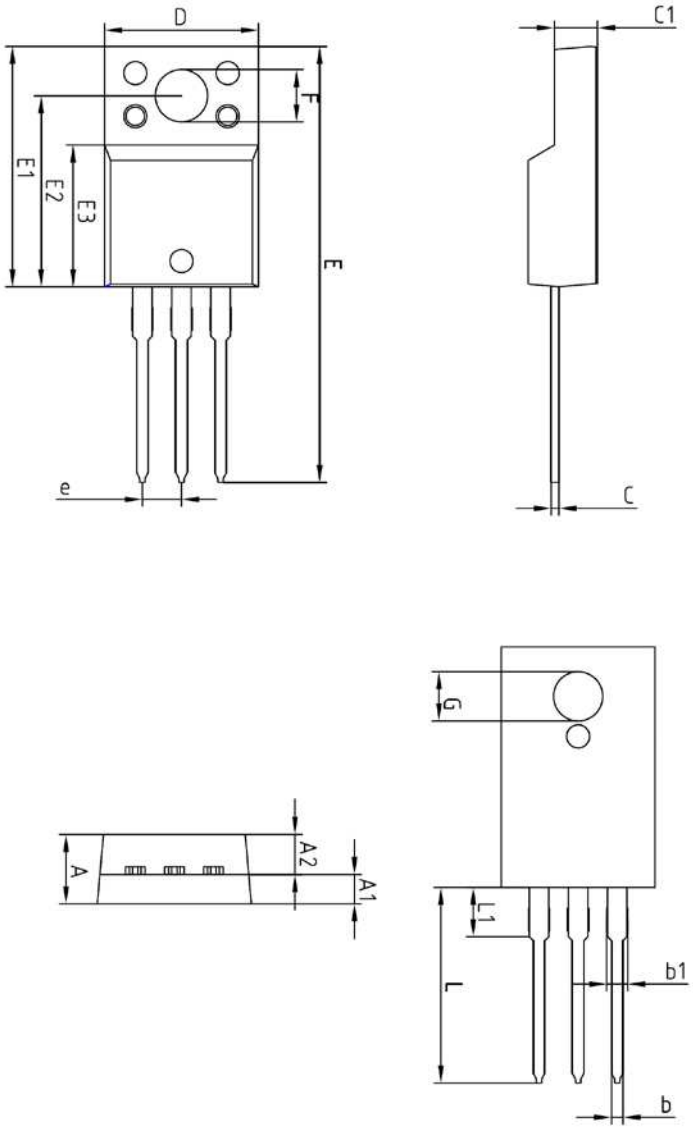








Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	–	–	4.60	
A1	2.45	2.50	2.55	
A2	1.95	2.00	2.05	
b	0.65	0.75	0.85	
b1	1.07	1.27	1.47	
C	0.40	0.50	0.60	
C1	2.70	2.80	2.90	
D	9.90	10.00	10.10	
E	28.00	–	28.60	
E1	15.50	15.60	15.70	
E2	12.30	12.40	12.50	
E3	9.15	9.20	9.25	
F	3.30	3.40	3.50	
G	3.10	3.20	3.30	
e	2.54 BSC			
L	12.40	–	13.00	
L1	3.46 BSC			

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