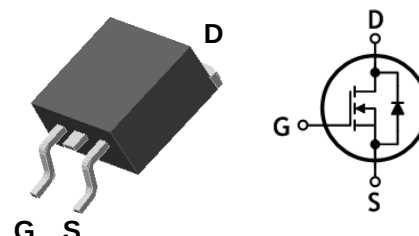


N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=750V$ ($@T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.38\Omega$ (Max.)
- Ultra low gate charge: $Q_g=20nC$ (Typ.)
- RoHS compliant device
- 100%avalanche tested

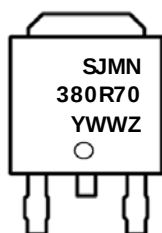


Ordering Information

Part Number	Marking	Package
SJMN380R70B	SJMN380R70	TO-263 (D ² -PAK)

TO-263 (D²-PAK)

Marking Information



Column 1, 2: Device Code
Column 3: Production Information
e.g.) YWWZ
-. YWW: Date Code (year, week)
-. Z: Management Code

Absolute maximum ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V _{DSS}		700	V
Gate-source voltage	V _{GSS}		±30	V
Drain current (DC) ^(Note 1)	I _D	T _c =25°C	11	A
		T _c =100°C	7	A
Drain current (Pulsed) ^(Note 1)	I _{DM}		44	A
Single pulsed avalanche energy ^(Note 2)	E _{AS}		263	mJ
Repetitive avalanche current ^(Note 1)	I _{AR}		7	A
Repetitive avalanche energy ^(Note 1)	E _{AR}		10.5	mJ
Power dissipation	P _D		105	W
Diode dv/ dt ruggedness ^(Note 3)	dv/ dt		15	V/ ns
MOSFET dv/ dt ruggedness ^(Note 4)	dv/ dt		50	V/ ns
Junction temperature	T _J		150	°C
Storage temperature range	T _{stg}		-55~150	°C

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.19	°C/ W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics (T_c=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu A, V_{GS}=0$	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu A, V_{DS}=V_{GS}$	2	3	4	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=700V, V_{GS}=0V$	-	-	1	uA
		$V_{DS}=700V, T_J=125^\circ C$	-	-	100	uA
Gate leakage current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 30V$	-	-	±100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=5.5A$	-	0.3	0.38	Ω
Internal gate resistance	R_g	f=1MHz, Open drain	-	20	-	Ω
Input capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V, f=1MHz$	-	858	-	pF
Output capacitance	C_{oss}		-	470	-	
Reverse transfer capacitance	C_{rss}		-	21	-	
Turn-on delay time (Note 5)	$t_{d(on)}$	$V_{DS}=350V, I_D=11A, R_G=25\Omega$	-	17	-	ns
Rise time (Note 5)	t_r		-	14	-	
Turn-off delay time (Note 5)	$t_{d(off)}$		-	40	-	
Fall time (Note 5)	t_f		-	5	-	
Total gate charge (Note 6)	Q_g	$V_{DS}=400V, V_{GS}=10V, I_D=6A$	-	20	-	nC
Gate-source charge (Note 6)	Q_{gs}		-	6.5	-	
Gate-drain charge (Note 6)	Q_{gd}		-	5.5	-	

Source-Drain Diode Ratings and Characteristics (T_c=25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	11	A
Source current (Pulsed)	I_{SM}		-	-	44	A
Forward voltage	V_{SD}	$V_{GS}=0V, I_S=11A$	-	-	1.2	V
Reverse recovery time (Note 5, 6)	t_{rr}	$I_S=11A, V_{GS}=0V, dI_S/dt=100A/\mu s$	-	270	-	ns
Reverse recovery charge (Note 5, 6)	Q_{rr}		-	2.8	-	uC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. L=10mH, $I_{AS}=7A, V_{DD}=50V$, Starting $T_J=25^\circ C$
3. $I_S \leq 11A, V_{DS} \leq 400V, dI_S/dt \leq 100A/\mu s, T_J=25^\circ C$
4. $V_{DS} \leq 400V, I_S \leq 11A$
5. Guaranteed by design, not subject to production testing
6. Pulse test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

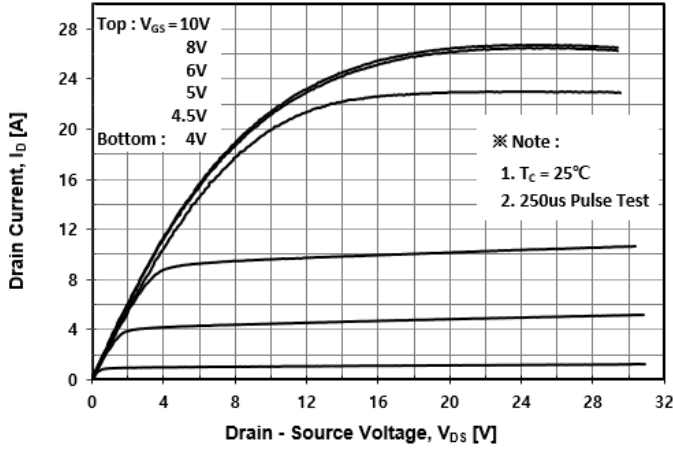


Fig. 2 Typical Transfer Characteristics

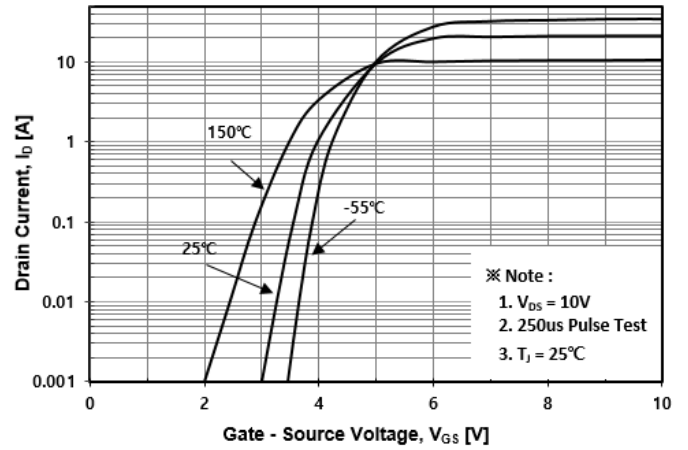


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

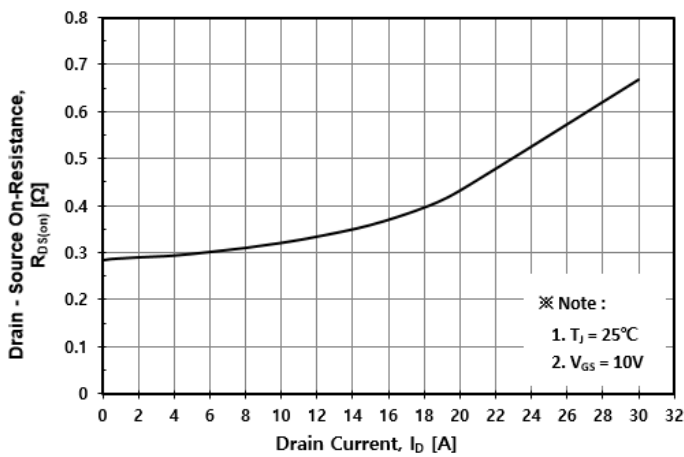


Fig. 4 Body Diode Forward Voltage Variation with Source Current

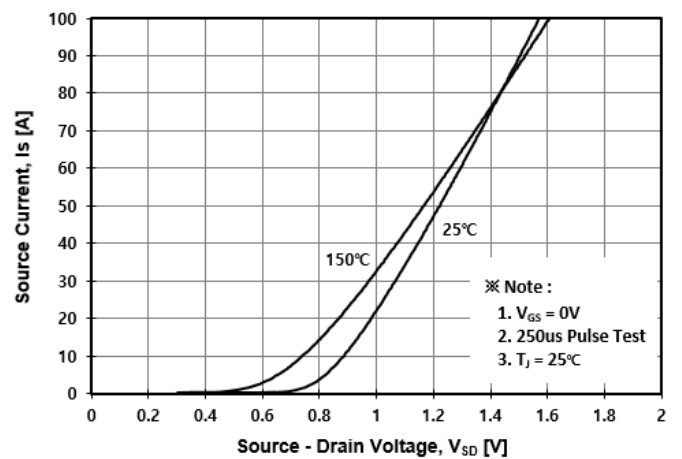


Fig. 5 Typical Capacitance Characteristics

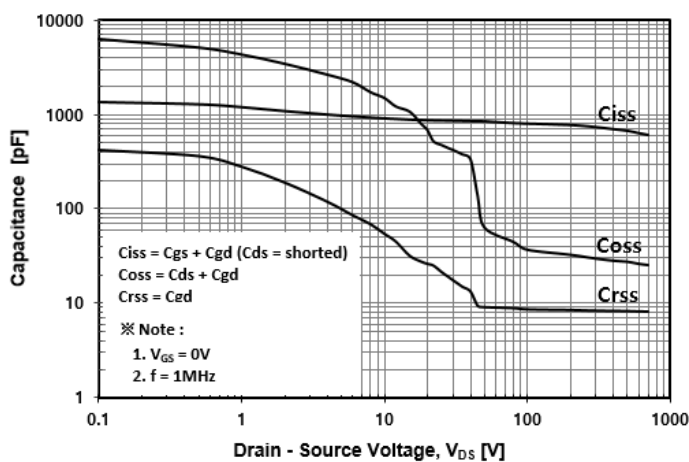


Fig. 6 Typical Total Gate Charge Characteristics

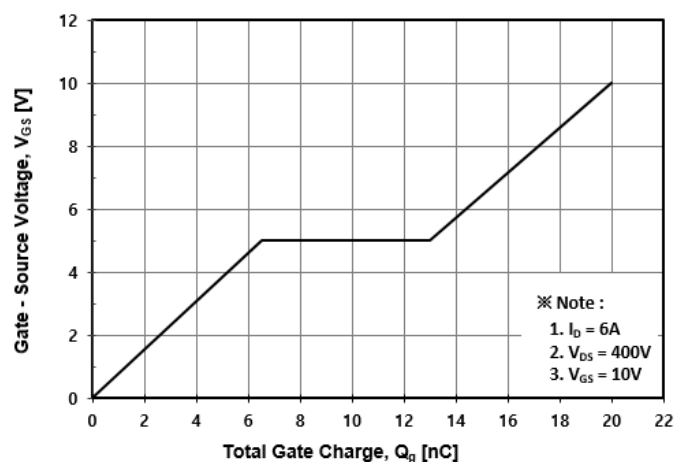


Fig. 7 Breakdown Voltage Variation vs. Temperature

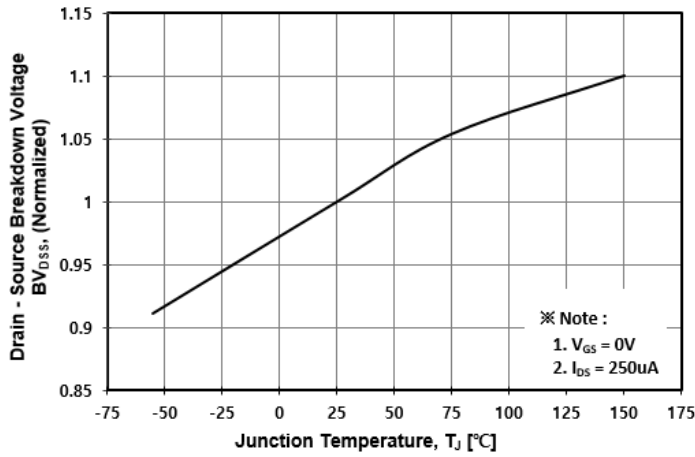


Fig. 8 On-Resistance Variation vs. Temperature

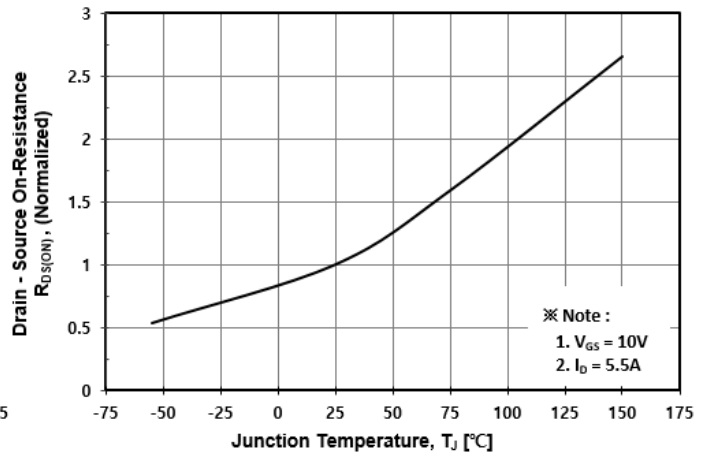


Fig. 9 Maximum Drain Current vs. Case Temperature

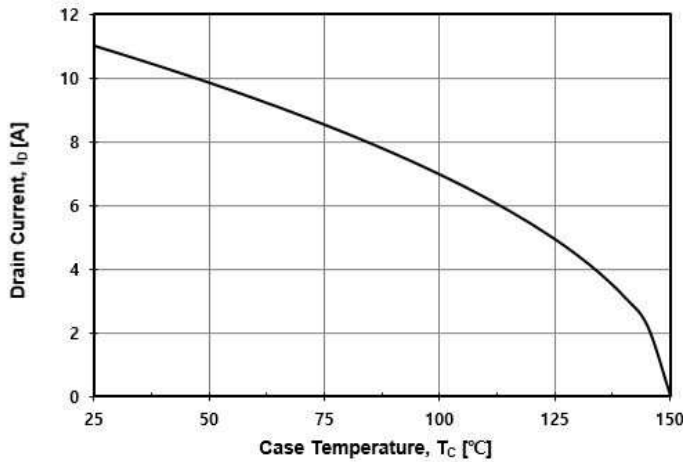


Fig. 10 Maximum Safe Operating Area

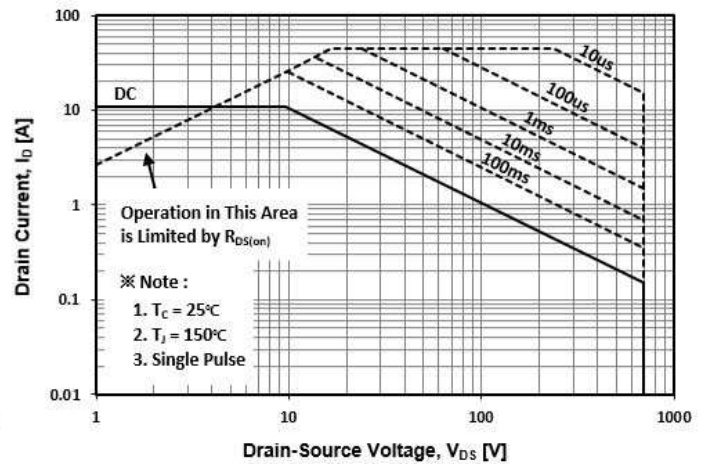


Fig. 11 Transient Thermal Impedance

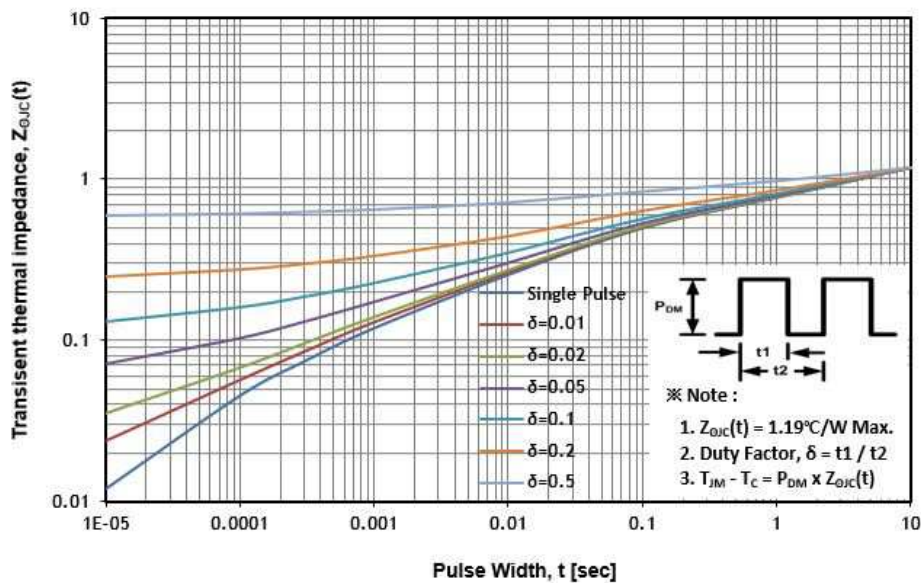


Fig. 12 Gate Charge Test Circuit & Waveform

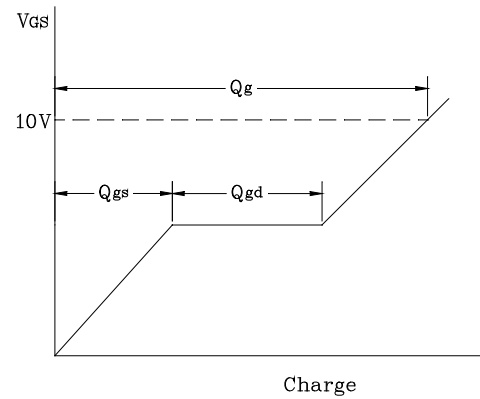
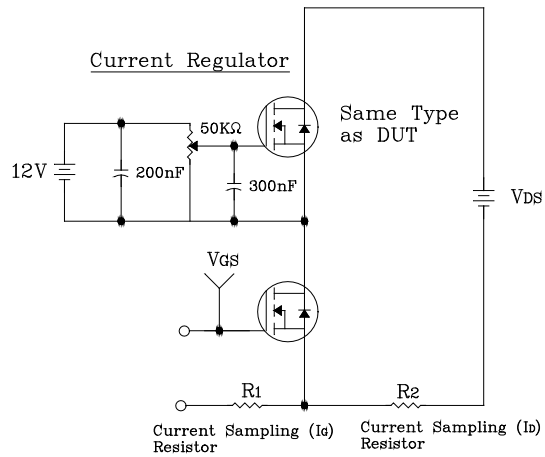


Fig. 13 Resistive Switching Test Circuit & Waveform

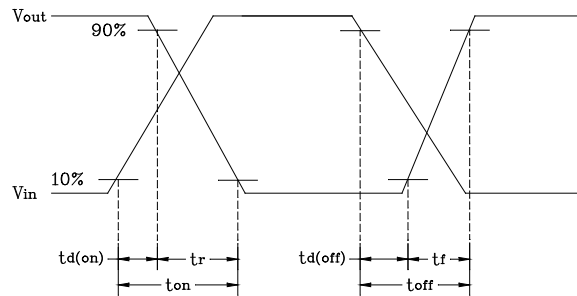
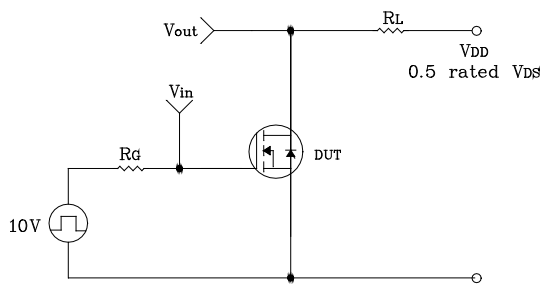


Fig. 14 E_{AS} Test Circuit & Waveform

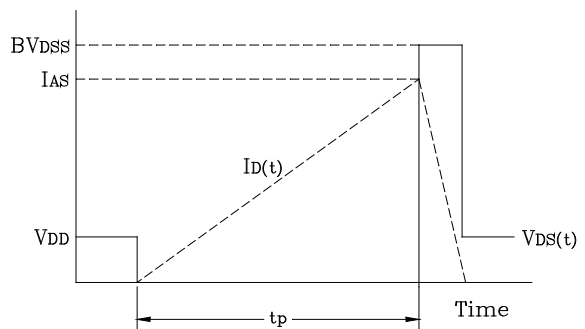
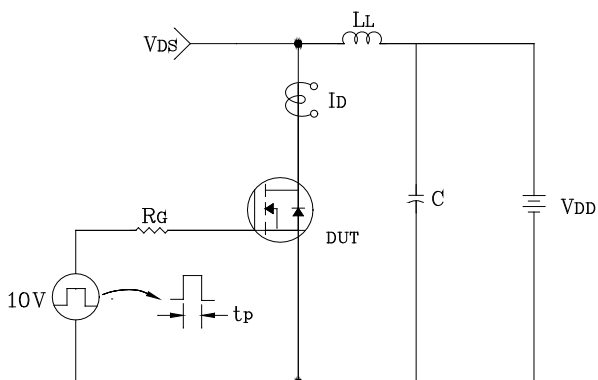
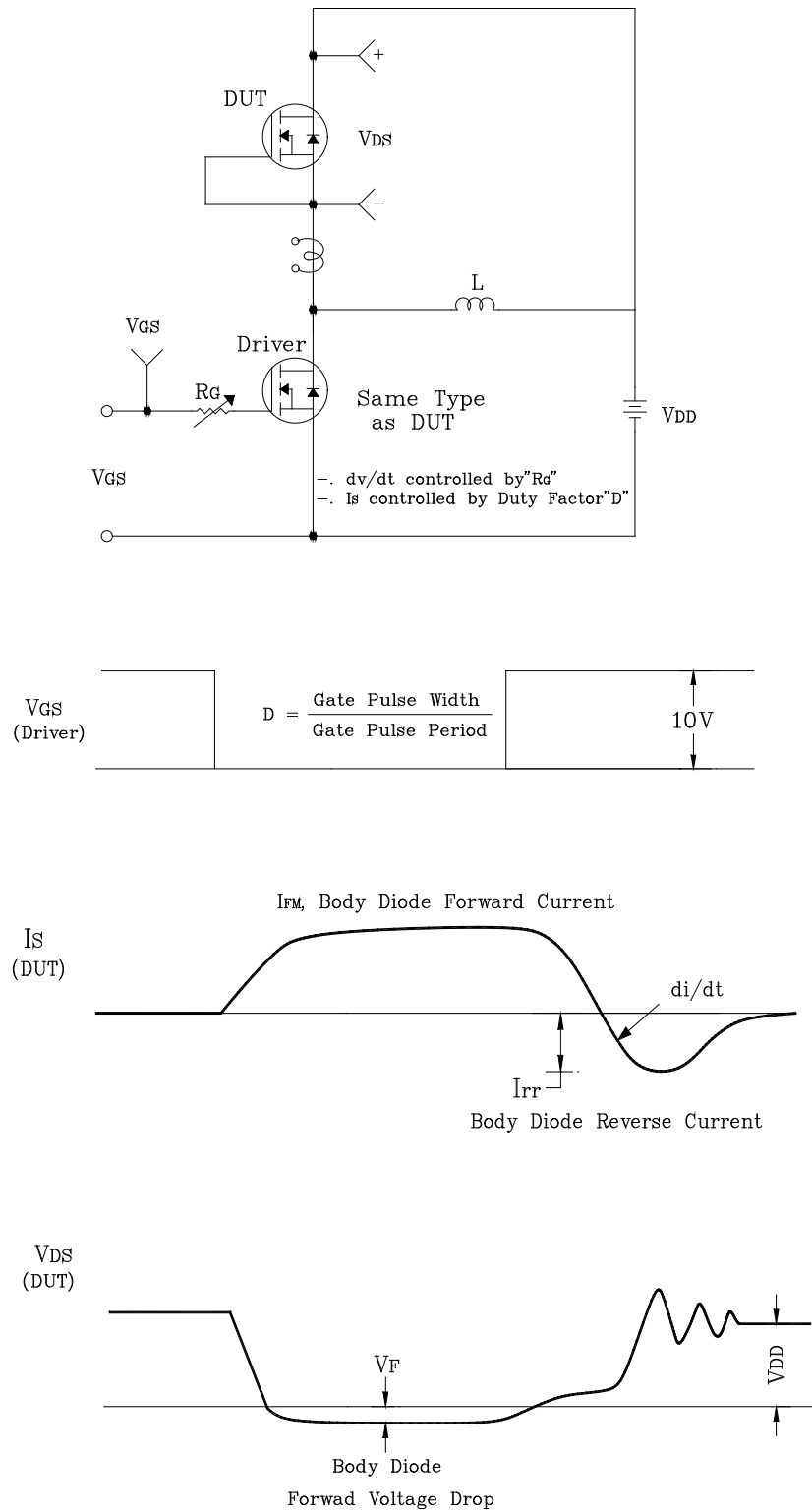
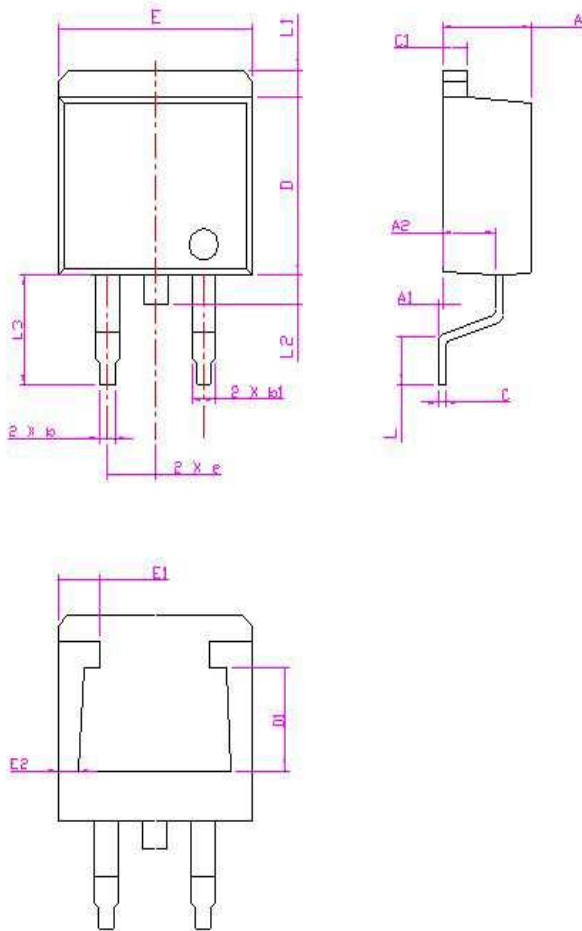


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform

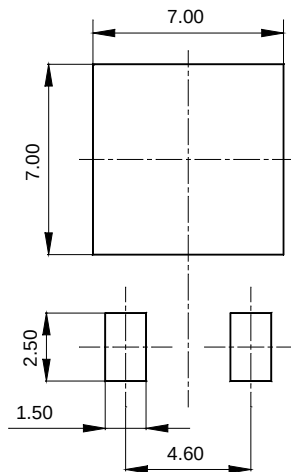


Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	4.49	4.69	4.89	
A1	0.00	—	0.20	
A2	2.69 BSC			
b	0.713	0.813	0.913	
b1	1.27 BSC			
C	0.281	0.381	0.481	
C1	1.17	1.27	1.37	
D	8.45	8.65	8.85	
D1	5.00 BSC			
E	10.00	10.20	10.40	
E1	2.00	2.20	2.40	
E2	0.90	1.10	1.30	
e	2.54 BSC			
L	2.54 BSC			
L1	1.26 BSC			
L2	1.40 BSC			
L3	5.10	5.30	5.50	

Recommended Land Pattern [unit: mm]



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