

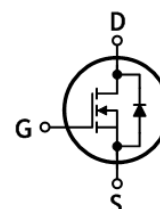
N-Channel Super Junction MOSFET

Features

- Drain-Source voltage: $V_{DS}=700V$ (@ $T_J=150^{\circ}C$)
- Low drain-source On resistance: $R_{DS(on)}=0.12\Omega$ (Typ.)
- Ultra low gate charge: $Q_g=50nC$ (Typ.)
- RoHS compliant device
- 100% avalanche tested

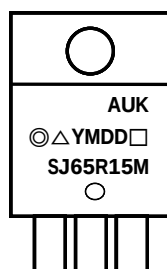
Ordering Information

Part Number	Marking	Package
SJMN65R15FM	SJ65R15M	TO-220FM-3L



TO-220FM-3L

Marking Information



Column 1: Manufacturer
 Column 2: Production Information
 e.g.) ◎△YMDD□
 -. ◎△: Factory Management Code
 -. YMDD: Date Code (Year, Month, Daily)
 -. □: Package Option Code
 Column 3: Device Code

Absolute maximum ratings ($T_c=25^{\circ}C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	650	V
Gate-source voltage	V_{GSS}	± 30	V
Drain current (DC) (Note 1)	I_D	$T_c=25^{\circ}C$	20
		$T_c=100^{\circ}C$	13
Drain current (Pulsed) (Note 1)	I_{DM}	60	A
Single pulsed avalanche energy (Note 2)	E_{AS}	720	mJ
Power dissipation	P_D	32	W
Junction temperature	T_J	150	$^{\circ}C$
Storage temperature range	T_{stg}	-55~150	$^{\circ}C$

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 3.9	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	650	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	2.5	3.5	4.5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=650\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=520\text{V}$, $T_J=125^\circ\text{C}$	-	-	10	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=10\text{A}$	-	0.12	0.15	Ω
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	2893	-	pF
Output capacitance	C_{oss}		-	2181	-	
Reverse transfer capacitance	C_{rss}		-	48	-	
Turn-on delay time (Note 3)	$t_{d(on)}$	$V_{DS}=400\text{V}$, $I_D=20\text{A}$, $R_G=25\Omega$	-	25	-	ns
Rise time (Note 3)	t_r		-	21	-	
Turn-off delay time (Note 3)	$t_{d(off)}$		-	60	-	
Fall time (Note 3)	t_f		-	4	-	
Total gate charge (Note 4)	Q_g	$V_{DS}=480\text{V}$, $V_{GS}=10\text{V}$, $I_D=20\text{A}$	-	50	-	nC
Gate-source charge (Note 4)	Q_{gs}		-	13	-	
Gate-drain charge (Note 4)	Q_{gd}		-	17	-	

Source-Drain Diode Ratings and Characteristics ($T_c=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	20	A
Source current (Pulsed)	I_{SM}		-	-	60	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=20\text{A}$	-	-	1.5	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=20\text{A}$, $V_{GS}=0\text{V}$, $dI_S/dt=100\text{A}/\mu\text{s}$	-	425	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	6.8	-	μC

Note:

1. Calculated continuous current based on maximum allowable junction temperature
2. $L=10\text{mH}$, $I_{AS}=12\text{A}$, $V_{DD}=50\text{V}$, Starting $T_J=25^\circ\text{C}$
3. Guaranteed by design, not subject to production testing
4. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

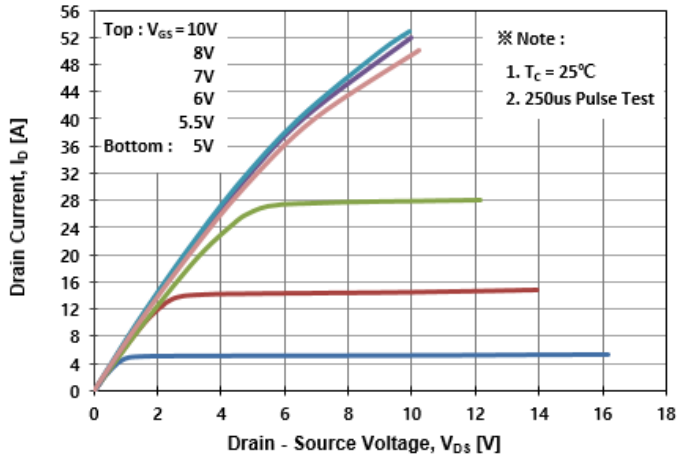


Fig. 2 Typical Output Characteristics

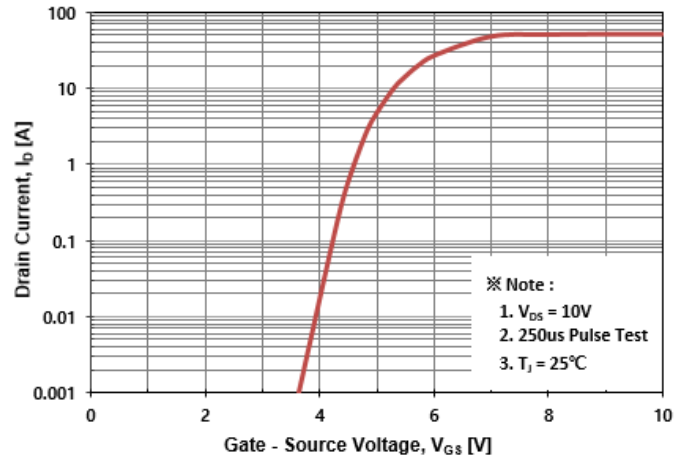


Fig.3 On-Resistance Variation with Gate Voltage

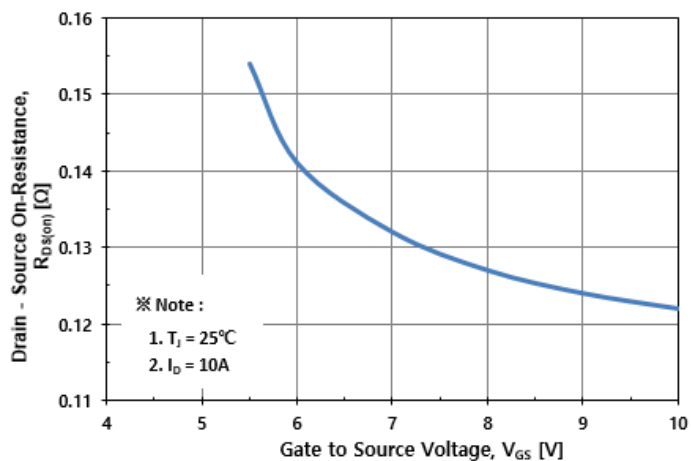


Fig. 4 Body Diode Forward Voltage Variation with Source Current

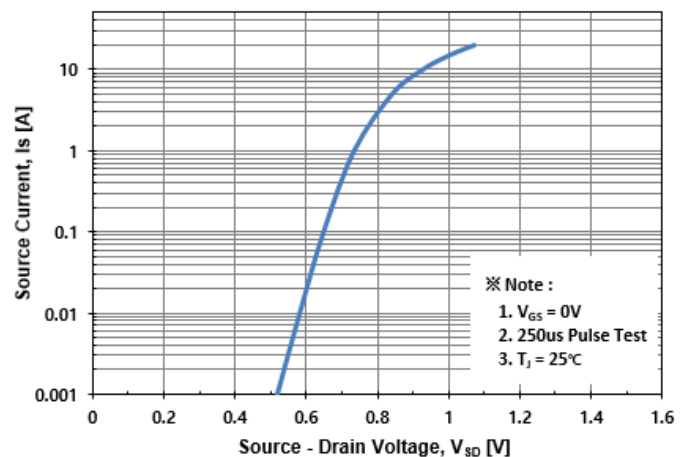


Fig. 5 Typical Capacitance Characteristics

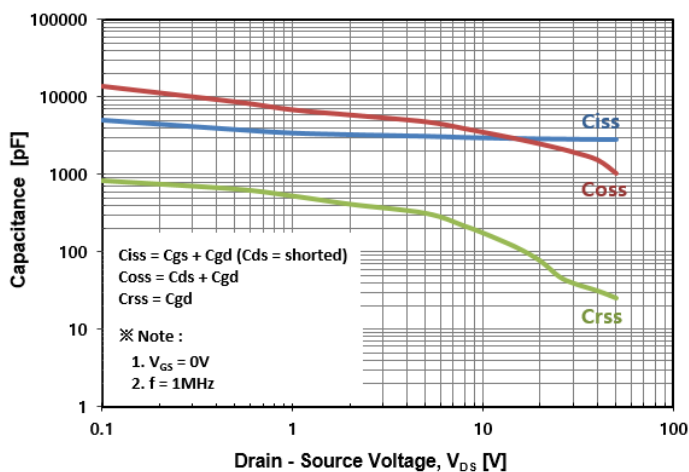


Fig. 6 Typical Total Gate Charge Characteristics

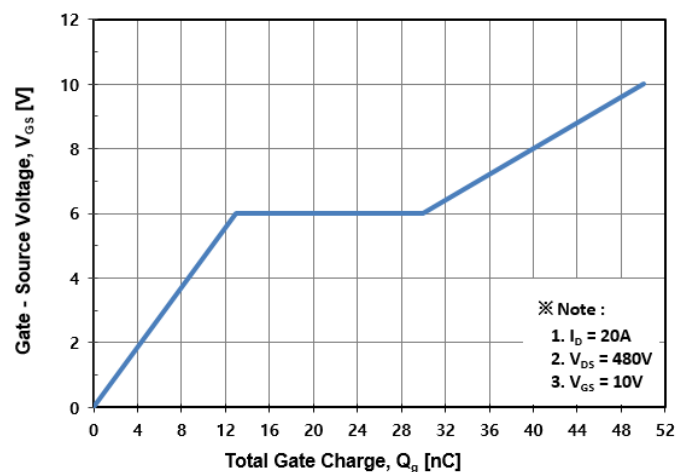


Fig. 7 Breakdown Voltage Variation vs. Temperature

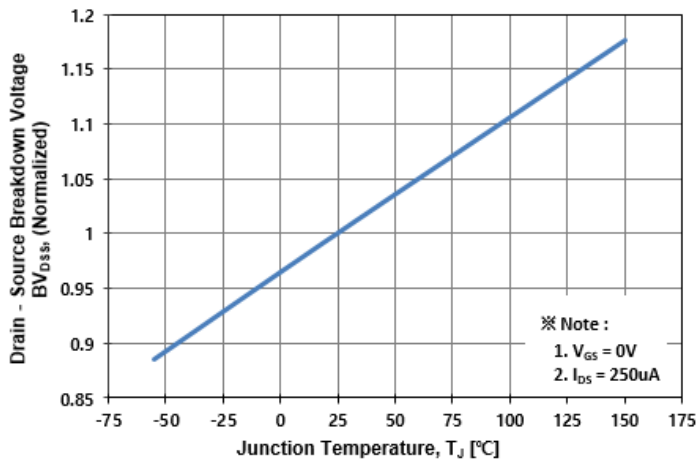


Fig. 8 On-Resistance Variation vs. Temperature

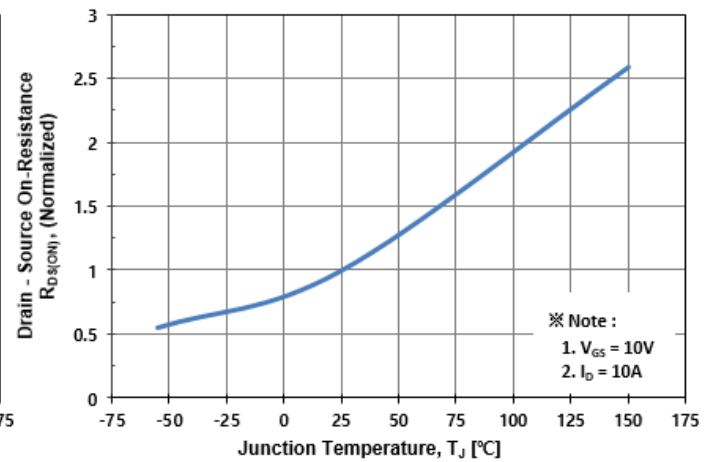


Fig. 9 Maximum Drain Current vs. Case Temperature

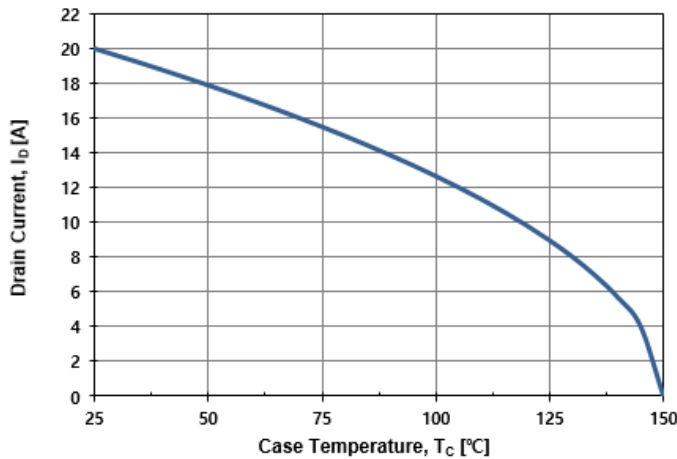


Fig. 10 Maximum Safe Operating Area

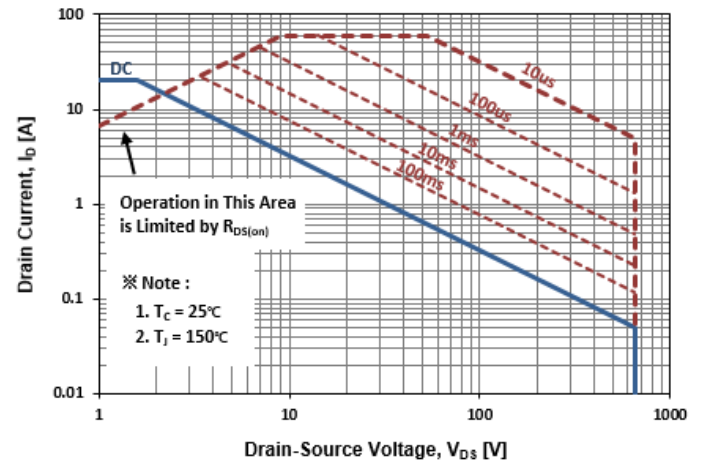


Fig. 11 Transient Thermal Impedance

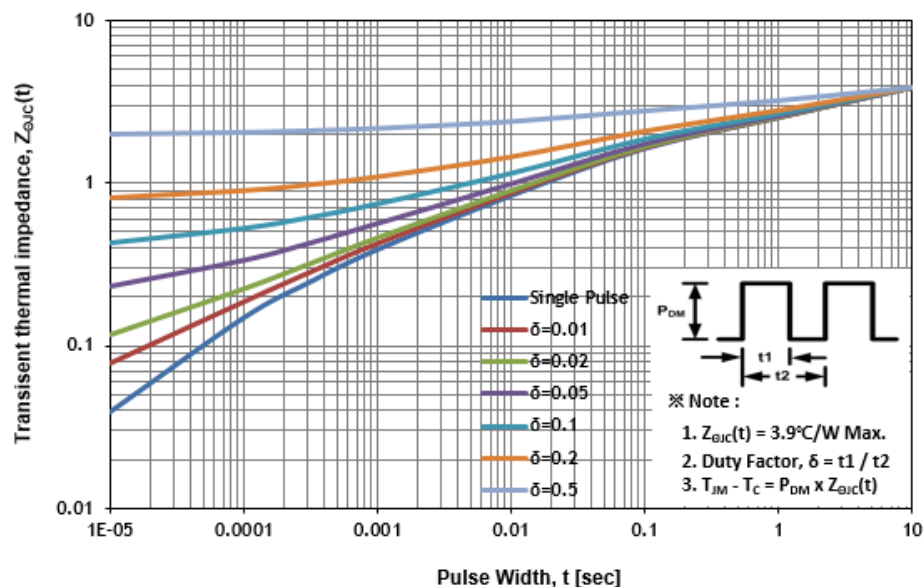


Fig. 12 Gate Charge Test Circuit & Waveform

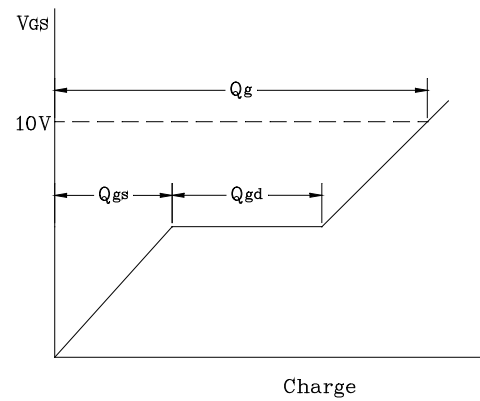
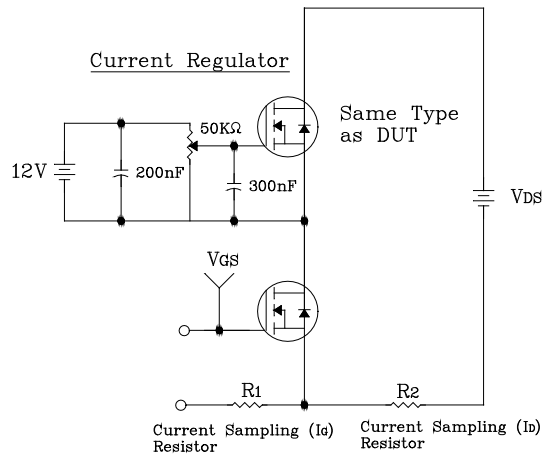


Fig. 13 Resistive Switching Test Circuit & Waveform

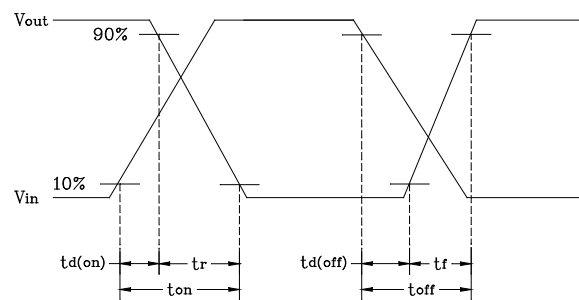
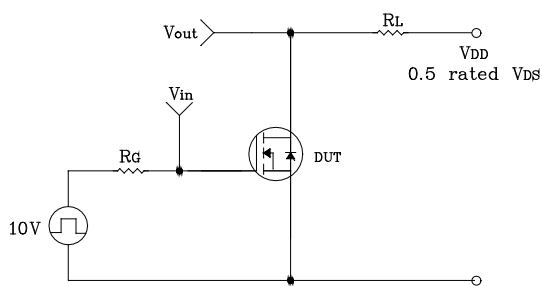


Fig. 14 E_{AS} Test Circuit & Waveform

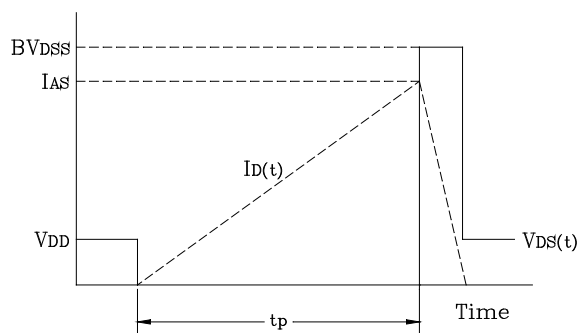
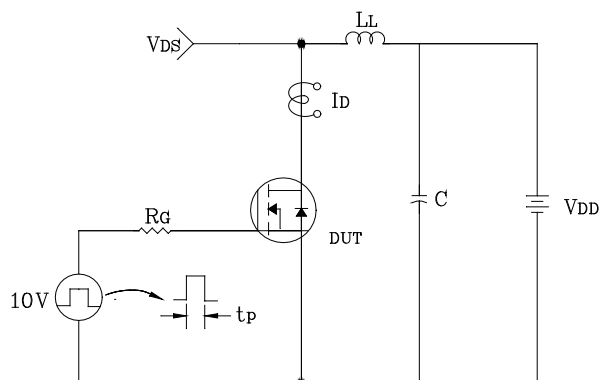
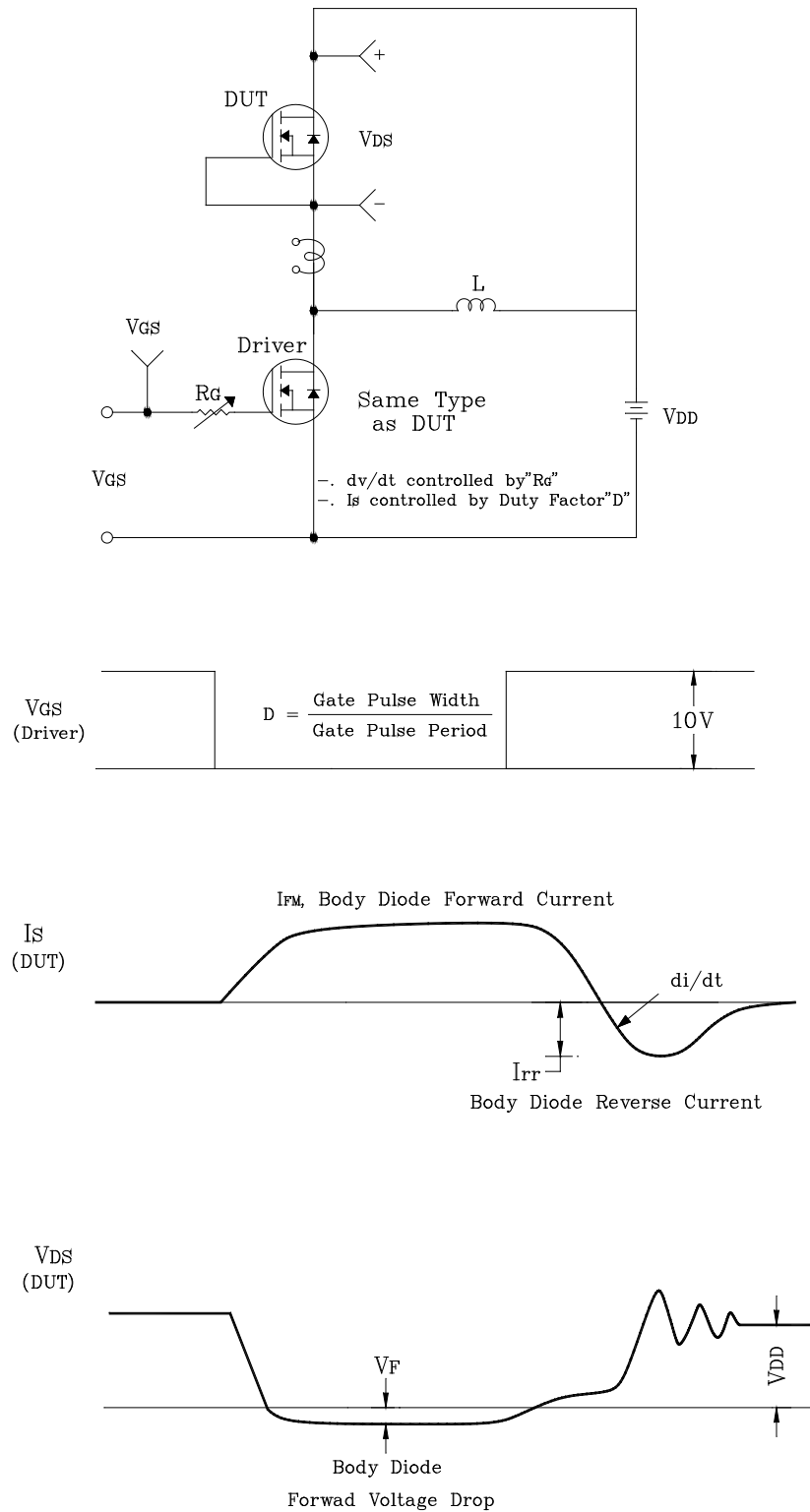
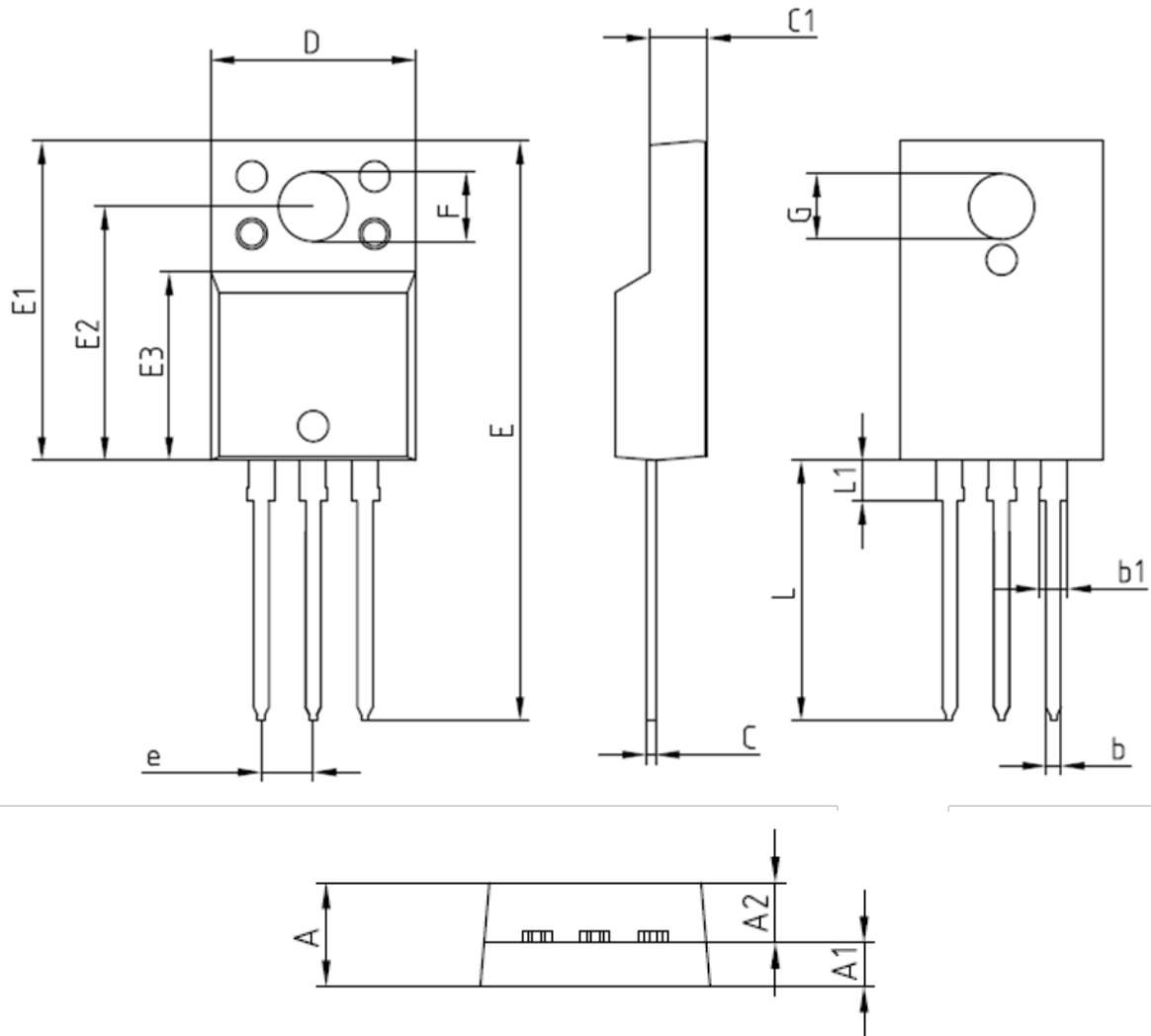


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	—	—	4.60	
A1	2.45	2.50	2.55	
A2	1.95	2.00	2.05	
b	0.65	0.75	0.85	
b1	1.07	1.27	1.47	
C	0.40	0.50	0.60	
C1	2.70	2.80	2.90	
D	9.90	10.00	10.10	
E	28.00	—	28.60	
E1	15.50	15.60	15.70	
E2	12.30	12.40	12.50	
E3	9.15	9.20	9.25	
F	3.30	3.40	3.50	
G	3.10	3.20	3.30	
e	2.34	2.54	2.74	
L	12.40	—	13.00	
L1	1.80	2.00	2.20	

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