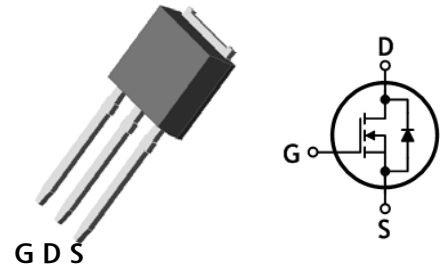


Power Switching Application

Features

- Drain-source breakdown voltage: $BV_{DSS}=900V$
- Low gate charge device: $Q_g=13nC$ (Typ.)
- Low drain-source On-resistance: $R_{DS(on)}=1\Omega$ (Typ.)
- Advanced trench process technology
- High avalanche energy, 100% test

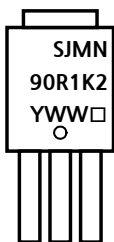


I-PAK

Ordering Information

Part Number	Marking	Package
SJMN90R1K2I	SJMN90R1K2	I-PAK

Marking Information



Column 1, 2: Device Code
Column 3: Production Information
e.g.) YWW□
- YWW: Date Code (year, week)
- □: Management Code

Absolute maximum ratings ($T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol		Rating	Unit
Drain-source voltage	V _{DSS}		900	V
Gate-source voltage	V _{GSS}		±30	V
Drain current (DC) *	I _D	T _C =25°C	6.5	A
		T _C =100°C	4	A
Drain current (Pulsed) *	I _{DM}		19.5	A
Single pulsed avalanche energy ^(Note 1)	E _{AS}		120	mJ
Single avalanche current	I _{AS}		2	A
Power dissipation	P _D		83	W
Operating junction temperature	T _J		150	°C
Storage temperature range	T _{stg}		-55 to 150	°C

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 1.5	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62	

Electrical Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	900	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	2.5	3.5	4.5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=900\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=720\text{V}$, $T_J=125^{\circ}\text{C}$	-	-	10	
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=3.5\text{A}$	-	1.0	1.2	Ω
Gate resistance	R_G	$f=1\text{MHz}$, open drain	-	6	-	Ω
Input capacitance	C_{iss}	$V_{DS}=100\text{V}$, $V_{GS}=0\text{V}$, $f=1\text{MHz}$	-	600	-	pF
Output capacitance	C_{oss}		-	25.1	-	
Reverse transfer capacitance	C_{rss}		-	1.8	-	
Turn-on delay time (Note 2,3,4)	$t_{d(on)}$	$V_{DD}=580\text{V}$, $I_D=3.5\text{A}$ $R_G=12\Omega$, $V_{GS}=10\text{V}$	-	13	-	ns
Rise time (Note 2,3,4)	t_r		-	11	-	
Turn-off delay time (Note 2,3,4)	$t_{d(off)}$		-	32	-	
Fall time (Note 2,3,4)	t_f		-	7	-	
Total gate charge (Note 2,3)	Q_g	$V_{DS}=580\text{V}$, $V_{GS}=10\text{V}$ $I_D=3.5\text{A}$	-	13	-	nC
Gate-source charge (Note 2,3)	Q_{gs}		-	2.5	-	
Gate-drain charge (Note 2,3)	Q_{gd}		-	6.5	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	6.5	A
Source current (Pulsed)	I_{SM}		-	-	19.5	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=3.5\text{A}$	-	-	1.2	V
Reverse recovery time (Note 2,4)	t_{rr}	$I_S=6.5\text{A}$, $V_{GS}=0\text{V}$ $di_S/dt=100\text{A}/\mu\text{s}$	-	520	-	ns
Reverse recovery charge (Note 2,4)	Q_{rr}		-	1.7	-	μC

Note:

1. $L=60\text{mH}$, $I_{AS}=2\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^{\circ}\text{C}$
2. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 1.5\%$
3. Essentially independent of operating temperature typical characteristic
4. Guaranteed by design, not subject to production testing

Typical Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

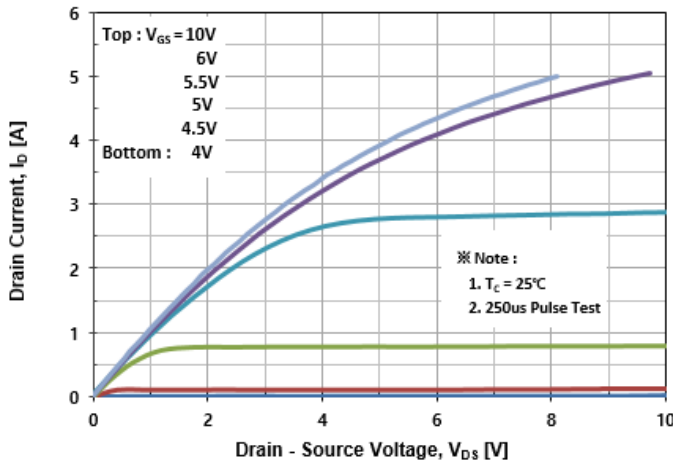


Fig. 2 Typical Transfer Characteristics

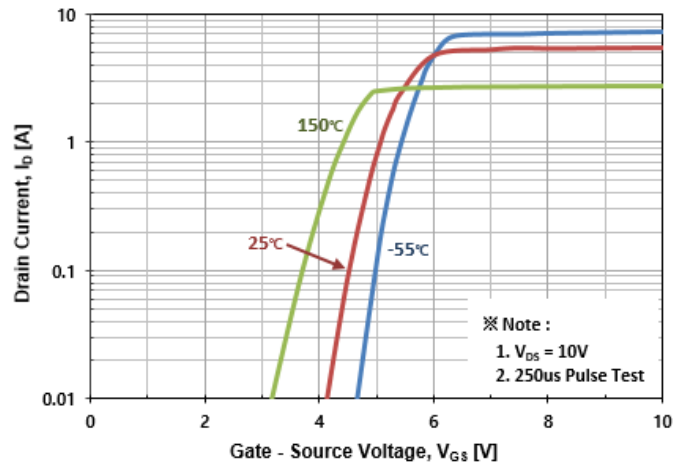


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

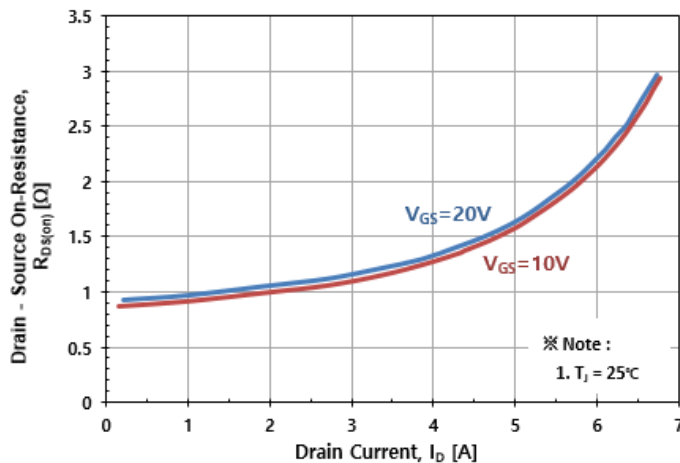


Fig. 4 Body Diode Forward Voltage Variation with Source Current

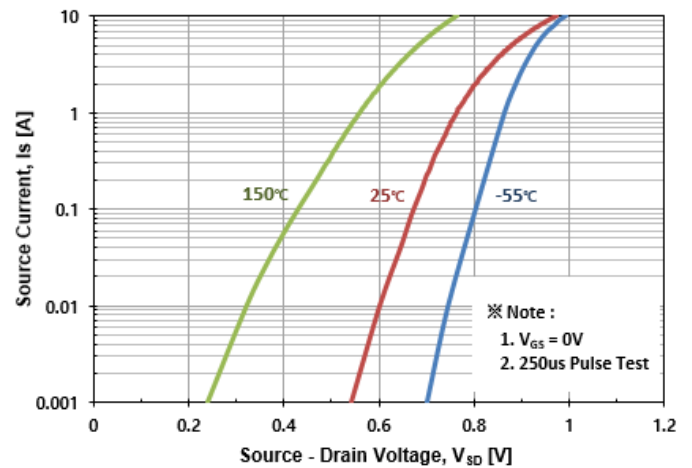


Fig. 5 Typical Capacitance Characteristics

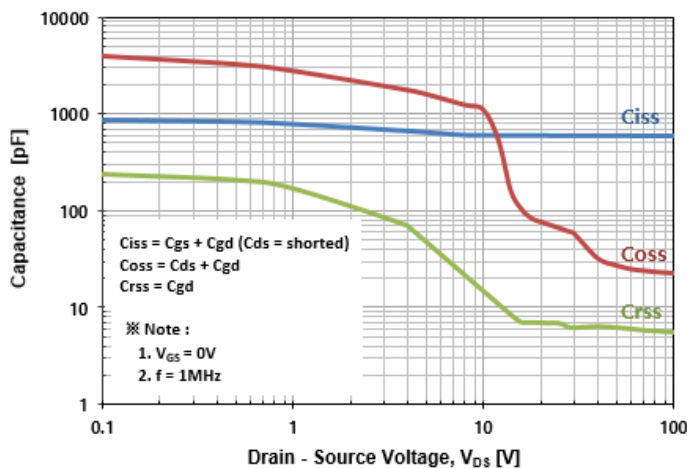
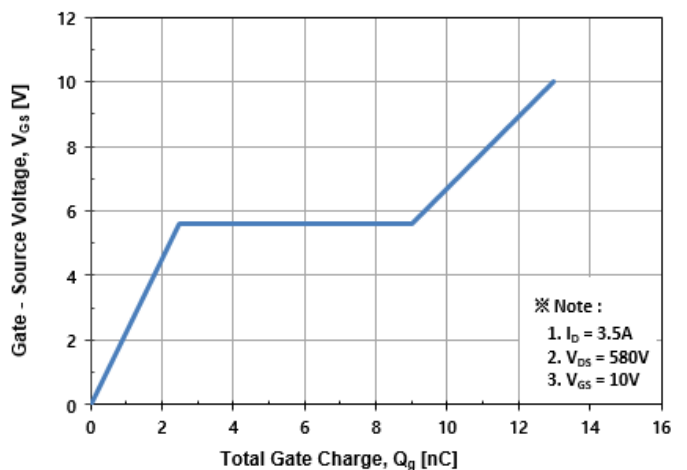


Fig. 6 Typical Total Gate Charge Characteristics



SJMN90R1K2I

Fig. 7 Breakdown Voltage Variation vs. Temperature

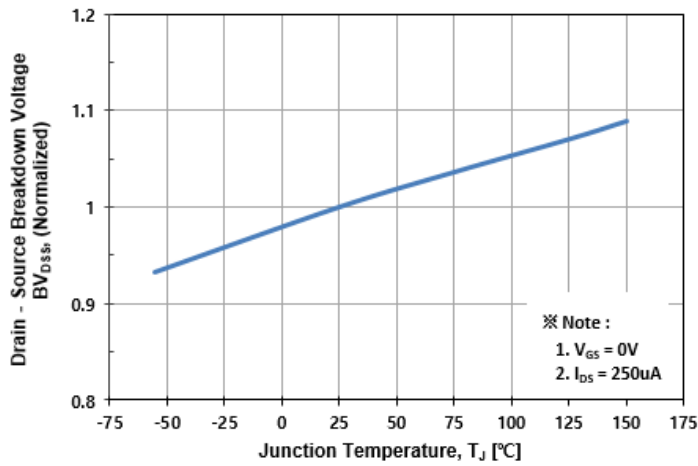


Fig. 8 On-Resistance Variation vs. Temperature

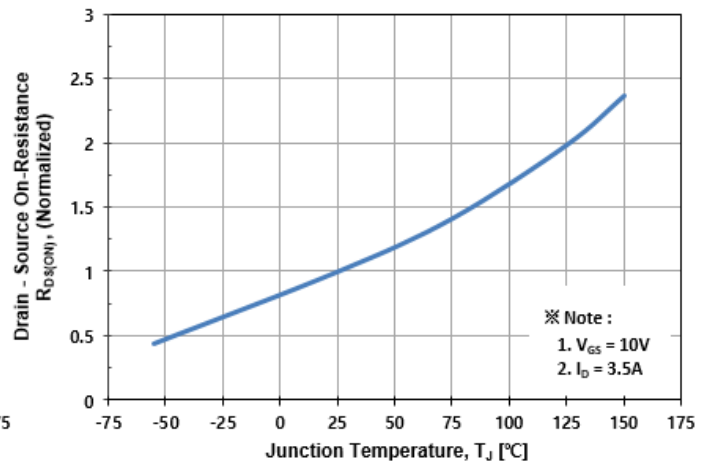


Fig. 9 Maximum Drain Current vs. Case Temperature

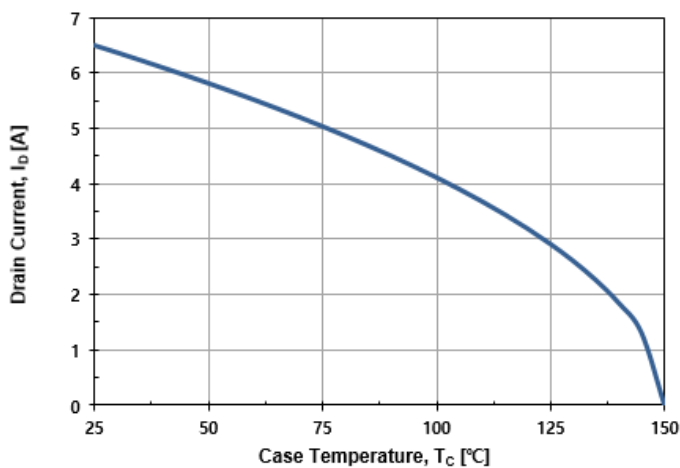


Fig. 10 Maximum Safe Operating Area

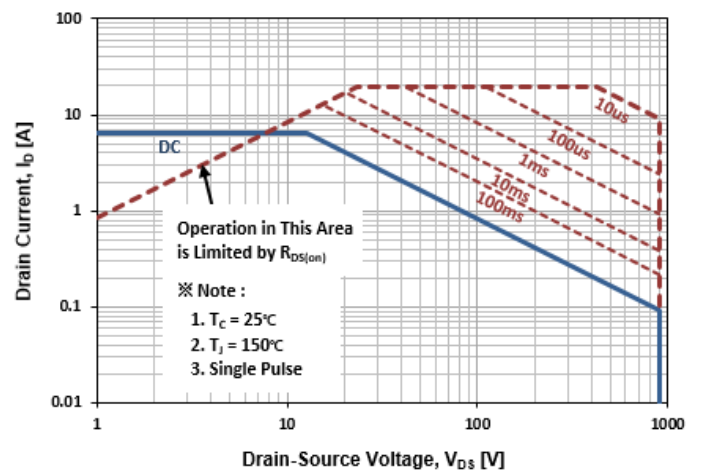


Fig. 11 Transient Thermal Impedance

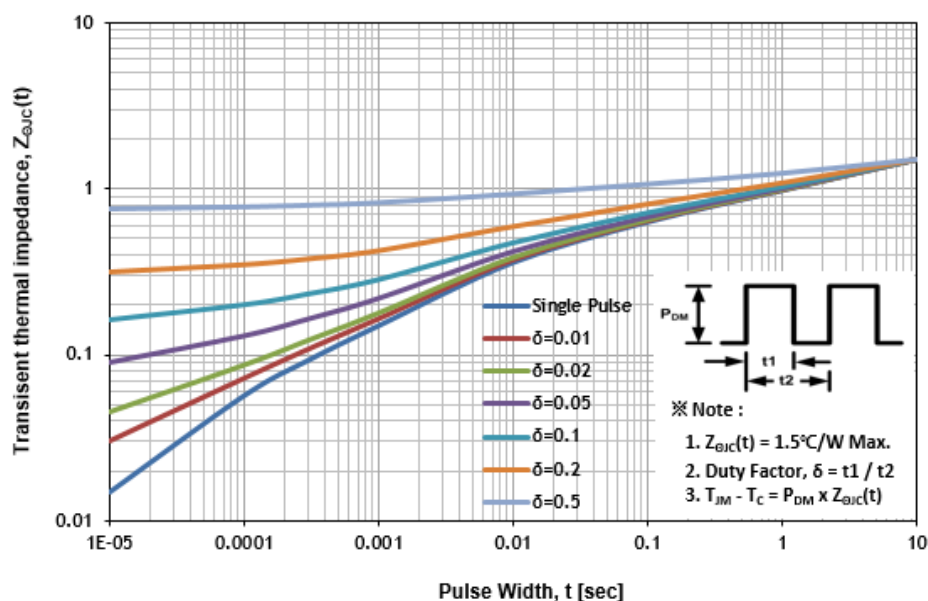


Fig. 12 Gate Charge Test Circuit & Waveform

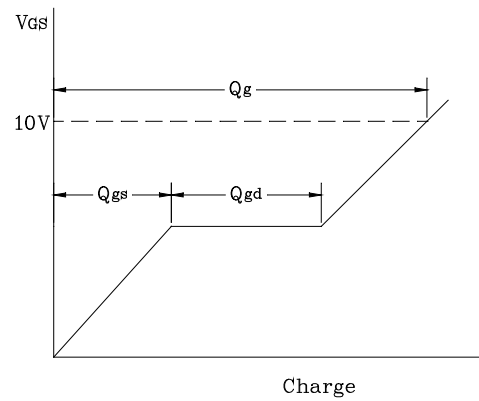
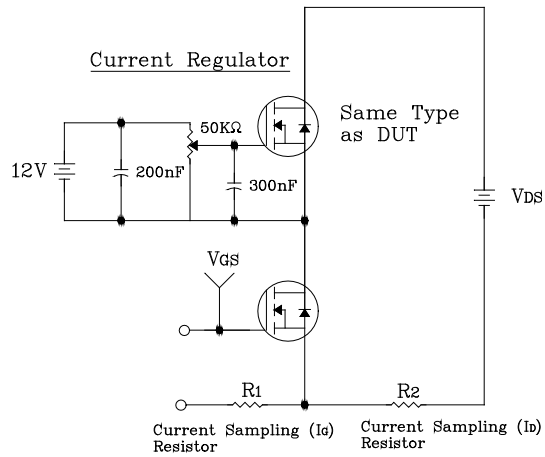


Fig. 13 Resistive Switching Test Circuit & Waveform

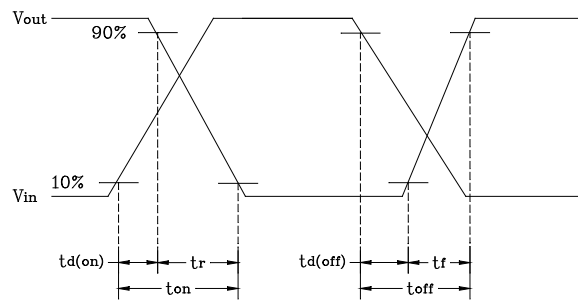
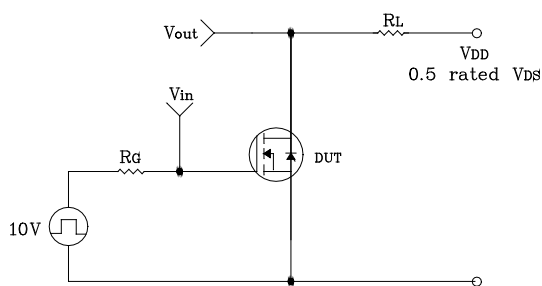


Fig. 14 E_{AS} Test Circuit & Waveform

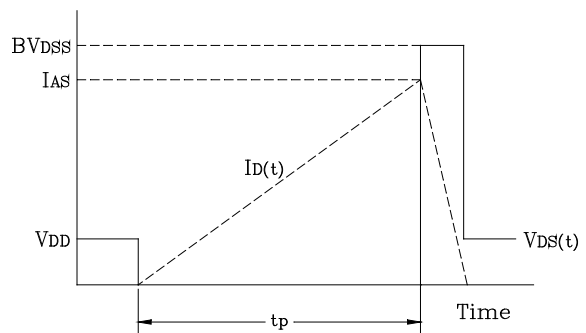
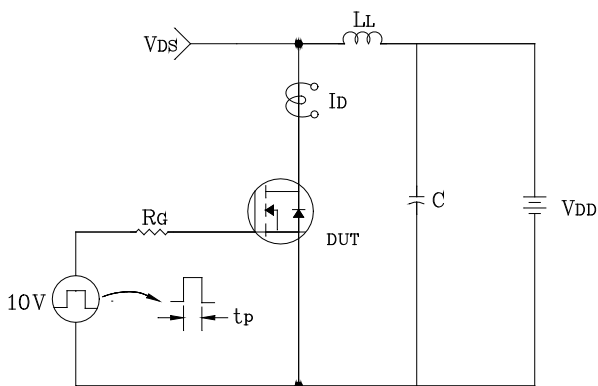
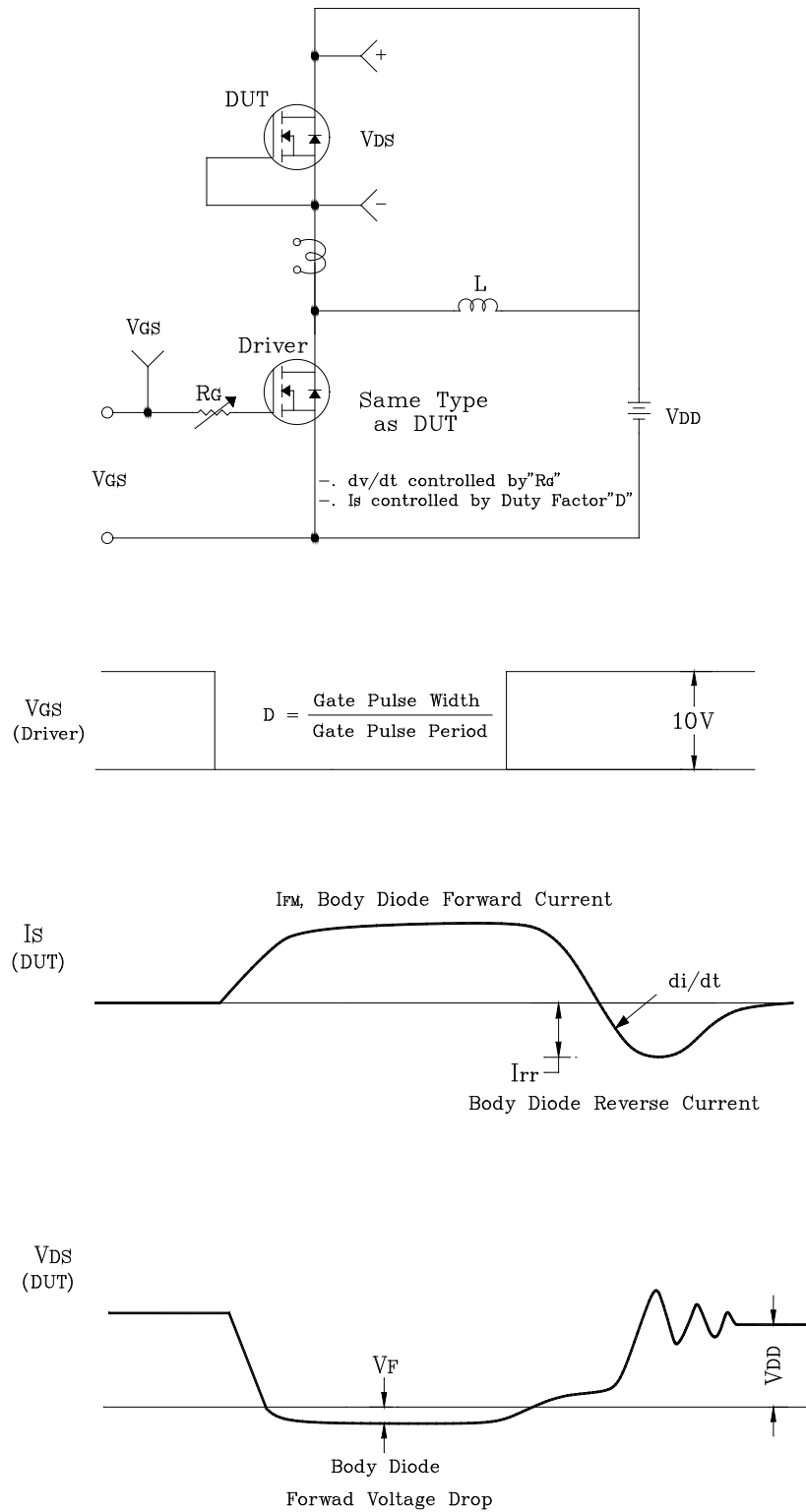
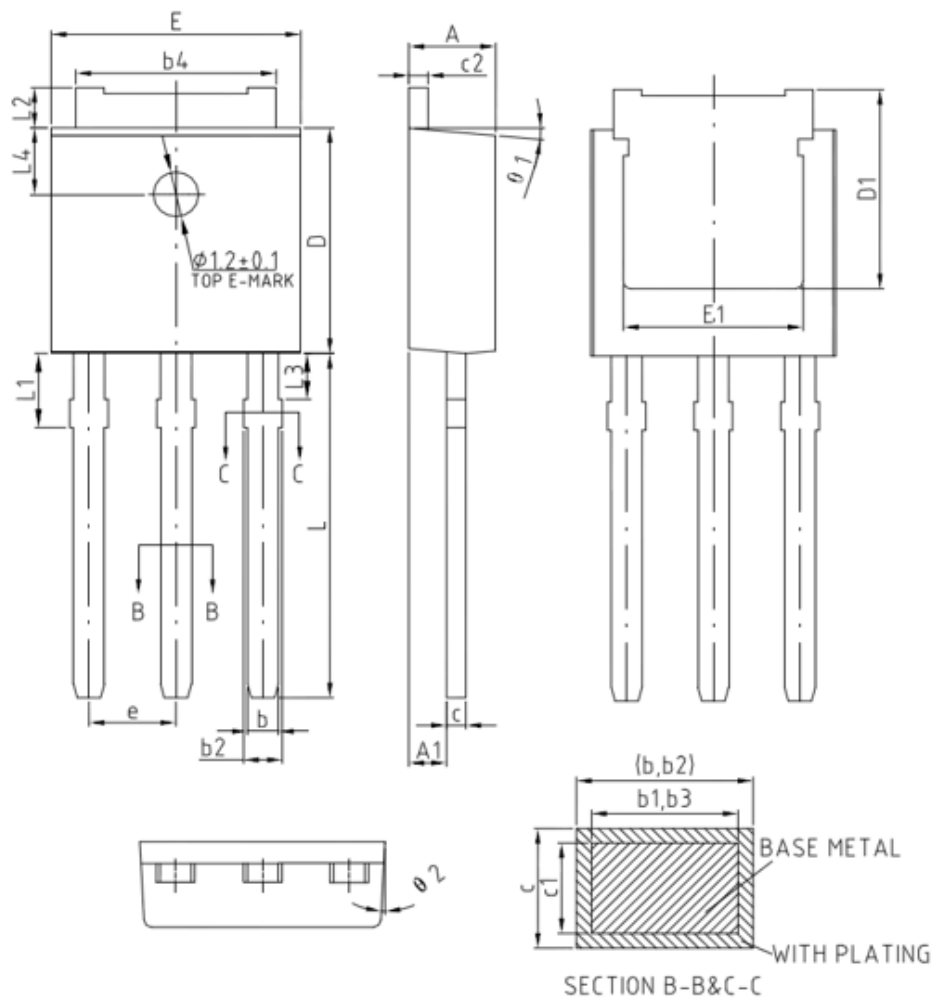


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions (Unit: mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	2.20	2.30	2.38
A1	0.90	1.00	1.10
b	0.77	—	0.89
b1	0.76	0.81	0.86
b2	0.77	—	1.10
b3	0.77	—	1.10
b4	5.23	5.33	5.43
c	0.47	—	0.60
c1	0.46	0.51	0.56
c2	0.47	—	0.60
D	6.00	6.10	6.20
D1	5.25	—	—
E	6.50	6.60	6.70
E1	4.70	—	—
e	2.28BSC		
L	9.00	9.30	9.60
L1	1.90	2.00	2.10
L2	0.90	—	1.25
L3	1.15	—	1.50
L4	1.80REF		
$\theta 1$	3°	5°	7°
$\theta 2$	1°	3°	5°

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