SJTU07N70C

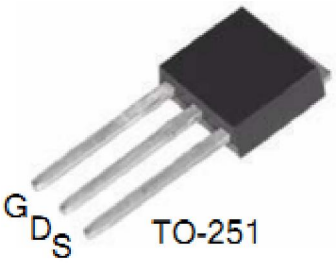
Super-Junction MOSFET

Lead Free Package and Finish

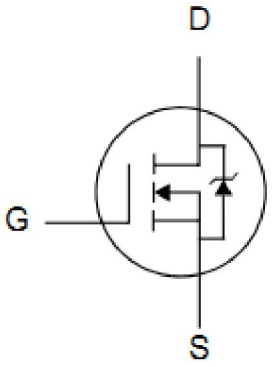
Applications:
- Adaptor
- Charger
- SMPS

V_{DSS}	$R_{DS(ON)}$(Typ.)	I_D
700V	0.74Ω	7A

Features:
- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves



Packages
Not to Scale



Ordering Information

PART NUMBER	PACKAGE	BRAND
SJTU07N70C	TO-251	***IPS***

Absolute Maximum Ratings

T_C=25℃ unless otherwise specified

Symbol	Parameter	SJTU07N70C	Units
V_{DSS}	Drain-to-Source Voltage	700	V
I_D	Continuous Drain Current	7	A
I_{DM}	Pulsed Drain Current, V_{GS}@10V (NOTE *1)	21	A
P_D	Power Dissipation	63	W
	Derating Factor above 25℃	0.5	W/℃
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS}	Single Pulse Avalanche Energy(NOTE *2)	162	mJ
E_{AR}	Avalanche Energy ,Repetitive (NOTE *1)	0.2	mJ
I_{AR}	Avalanche Current (NOTE *1)	1.4	A
T_L	Maximum Temperature for Soldering	300	℃
T_J and T_{STG}	Operating Junction and Storage Temperature Range	150，-55 to150	

Thermal Resistance

Symbol	Parameter	Typ.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	2.0	℃/W	Water cooled heatsink, P_D adjusted for a peak junction temperature of +150℃.
$R_{\theta JA}$	Junction-to-Ambient	62		1 cubic foot chamber, free air.

OFF Characteristics T_C=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	700	--	--	V	V_{GS}=0V, I_D=250μA
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	V_{DS}=700V, V_{GS}=0V T_J=25℃
		--	--	100		V_{DS}=700V, V_{GS}=0V T_J=150℃
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	V_{GS}=+30V
	Gate-to-Source Reverse Leakage	--	--	-100		V_{GS}= -30V

ON Characteristics T_J=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	StaticDrain-to-Source On-Resistance(NOTE *3)	--	0.74	0.85	Ω	V_{GS}=10V, I_D=3A
$V_{GS(TH)}$	Gate Threshold Voltage	2.5	--	4	V	V_{DS}=V_{GS},I_D=250μA
g_{fs}	Forward Transconductance(NOTE *3)	--	5	--	S	V_{DS}=10V, I_D=3A

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	587	--	pF	V_{GS}= 0V,V_{DS} = 50V f =1.0MHz
C_{oss}	Output Capacitance	--	31	--		
C_{rss}	Reverse Transfer Capacitance	--	4	--		
Q_g	Total Gate Charge	--	14.5	--	nC	I_D=7A,V_{DD}=560V V_{GS} = 10V
Q_{gs}	Gate-to-Source Charge	--	3	--		
Q_{gd}	Gate-to-Drain (“Miller”) Charge	--	5.2	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	39	--	ns	V_{DD}=400V, I_D=7A, V_G=10V R_G=25Ω
t_{rise}	Rise Time	--	25	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	100	--		
t_{fall}	Fall Time	--	18	--		

Source-Drain Diode Characteristics Tc=25℃ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	--	--	6.3	A	T_C=25℃
I_{SM}	Maximum Pulsed Current (Body Diode)	--	--	19	A	
V_{SD}	Diode Forward Voltage	--	--	1.2	V	I_{SD}=7A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	250	--	ns	I_F= I_S di/dt=100A/us
Q_{rr}	Reverse Recovery Charge	--	2.1	--	uC	

Notes:

*1. Repetitive rating; pulse width limited by maximum junction temperature.

*2. V_{DD} =50V, I_D=1.4A, Start T_J=25℃

*3. Pulse width < 300μs; duty cycle < 2%.

Characteristics Curve：

Figure 1.Typical Output Characteristics

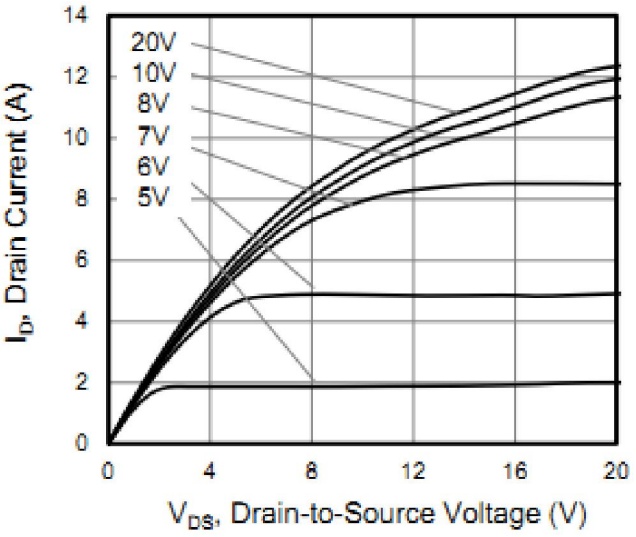


Figure 2. Typical Transfer Characteristics

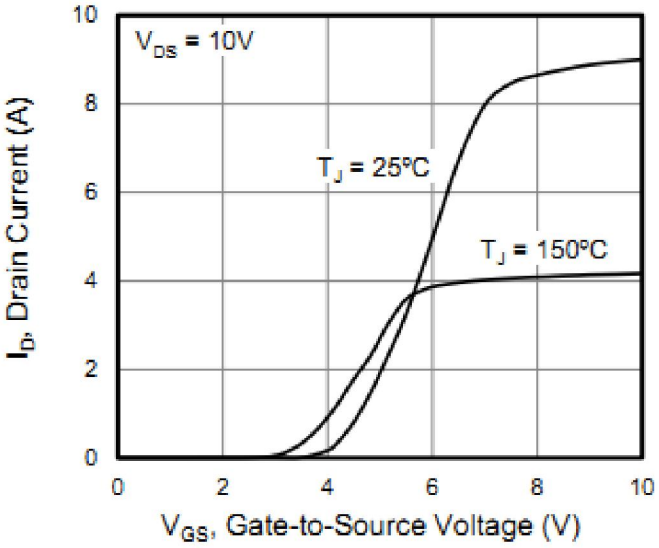


Figure 3. Typical Body Diode Transfer Characteristics

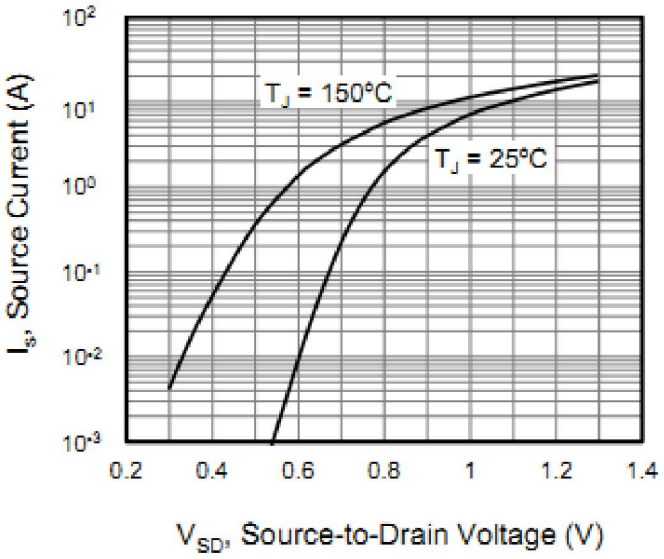


Figure 4. on ResistanceVS Drain Current

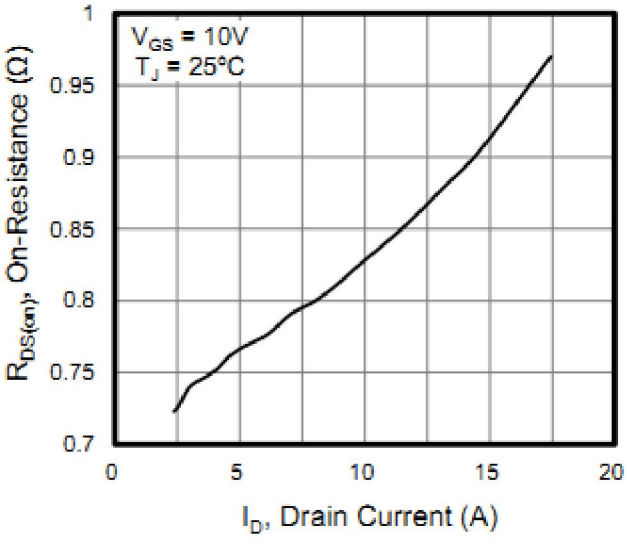


Figure 5. Capacitance VS Drain-to-Source Voltage

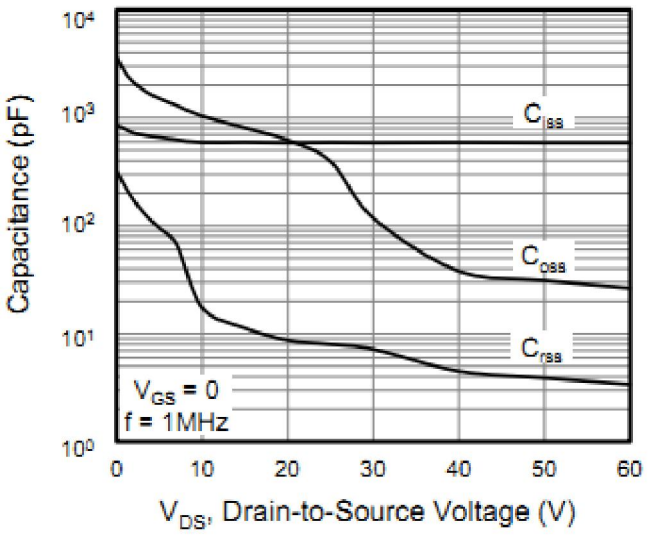


Figure 6. Gate Charge VS Gate-to-Source Voltage

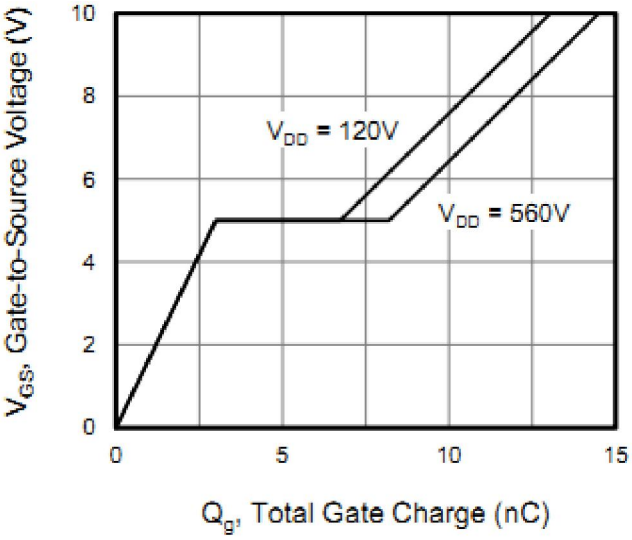


Figure 7. Threshold Voltage VS Temperature

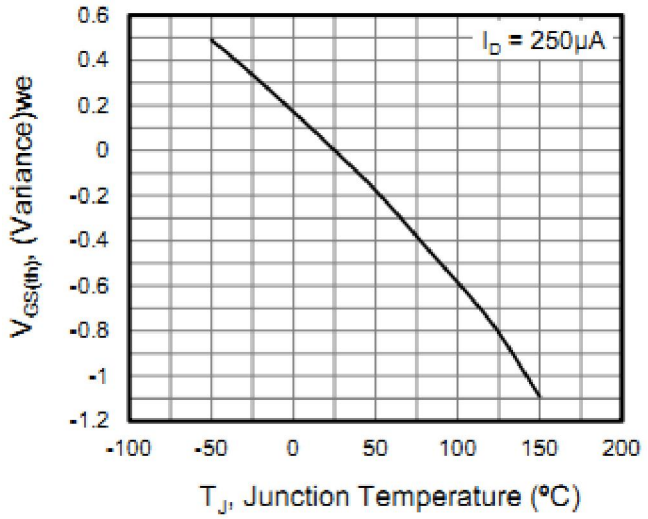


Figure 8 on-Resistance VS Temperature

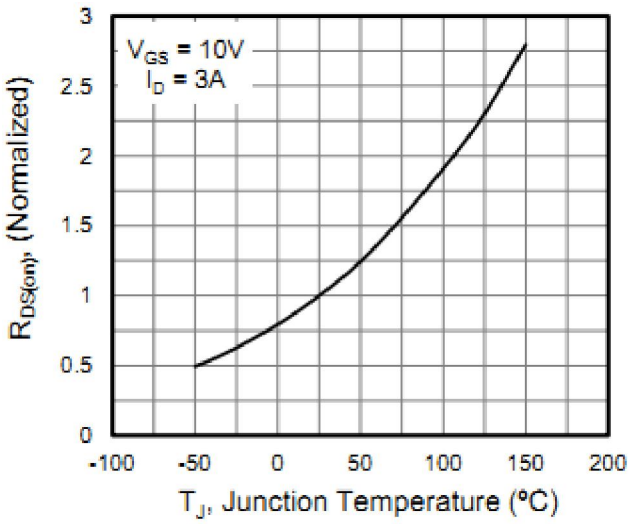


Figure 9.Maximum Effective Thermal Impedance，Junction-to-Case

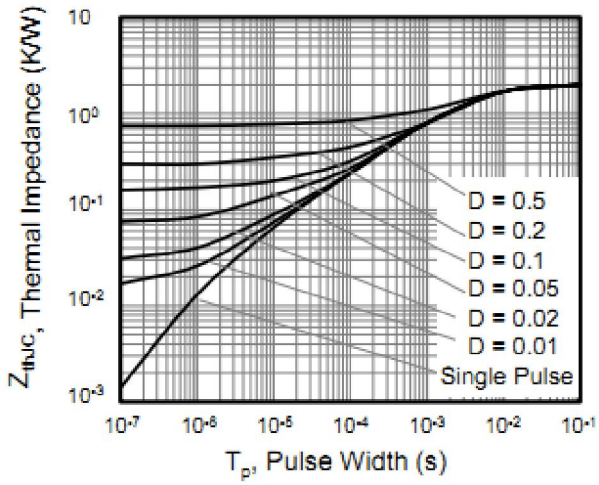


Figure 10. Gate Charge Test Circuit

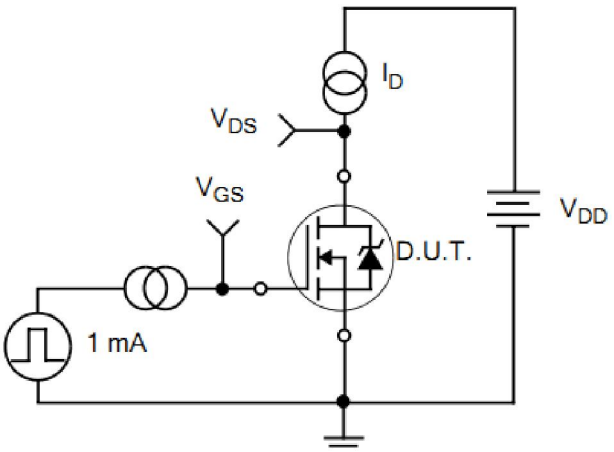


Figure 11. Gate Charge Waveforms

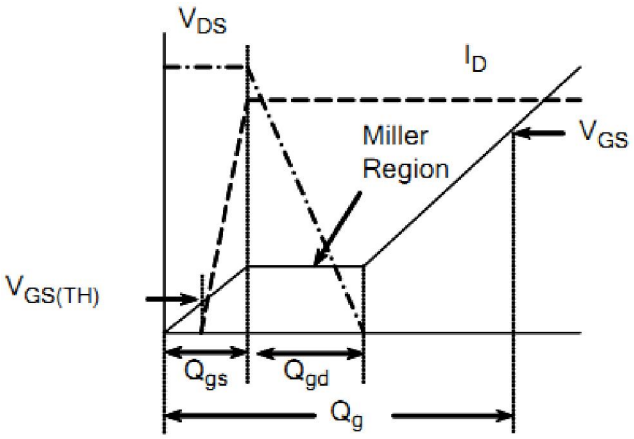


Figure 12. Resistive Switching Test Circuit

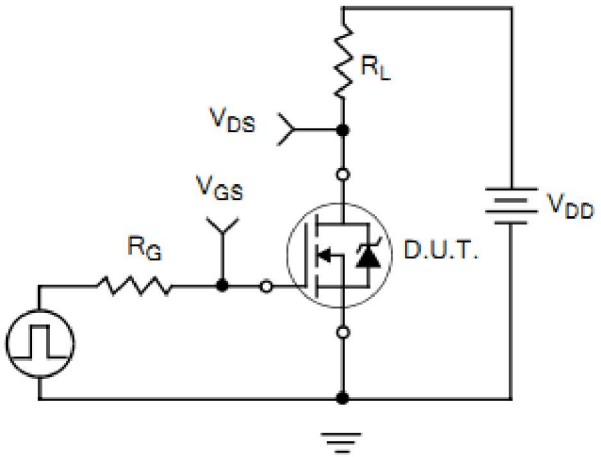


Figure 13. Resistive Switching Waveforms

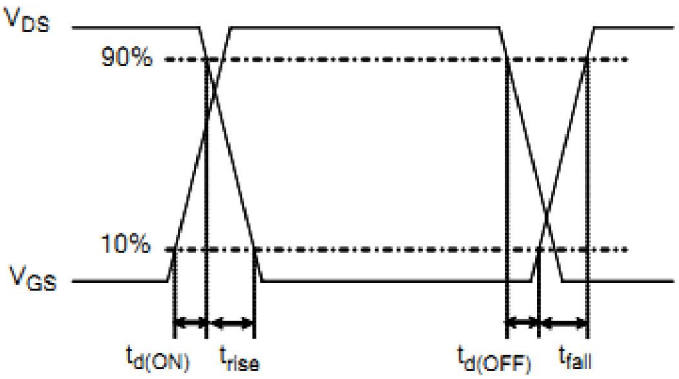


Figure 14. Diode Reverse Recovery Test Circuit

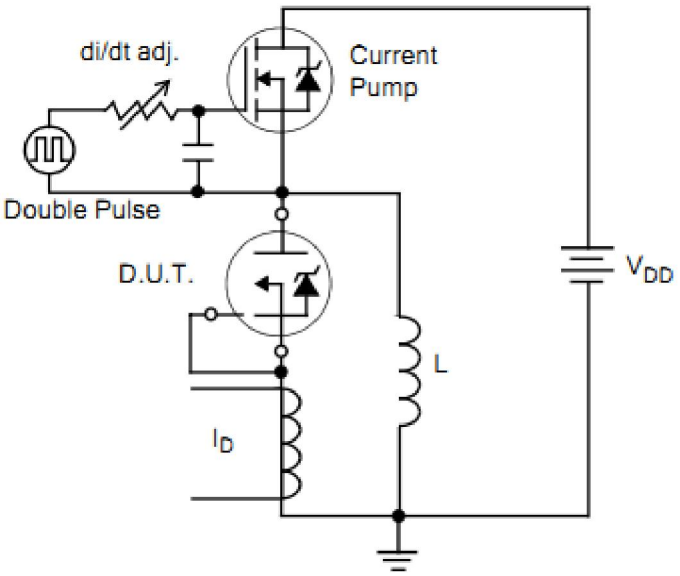


Figure 15. Diode Reverse Recovery Waveform

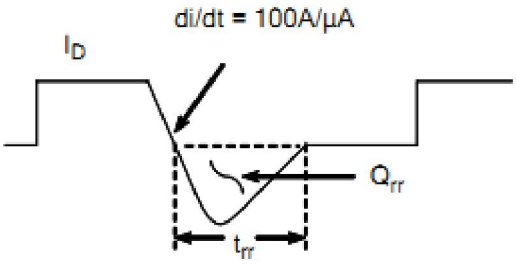


Figure16.Unclamped Inductive Switching Test Circuit

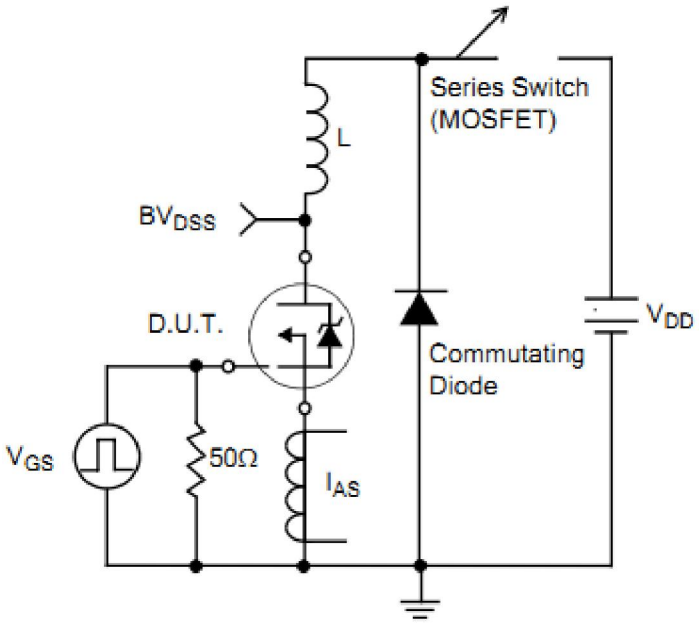
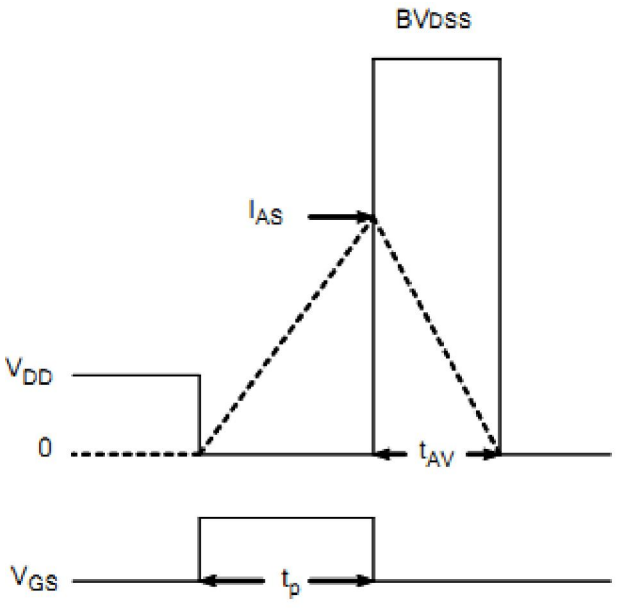


Figure17.Unclamped Inductive Switching Waveform



$$E_{AS} \quad \frac{I_{AS}^{2} L}{2}$$

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