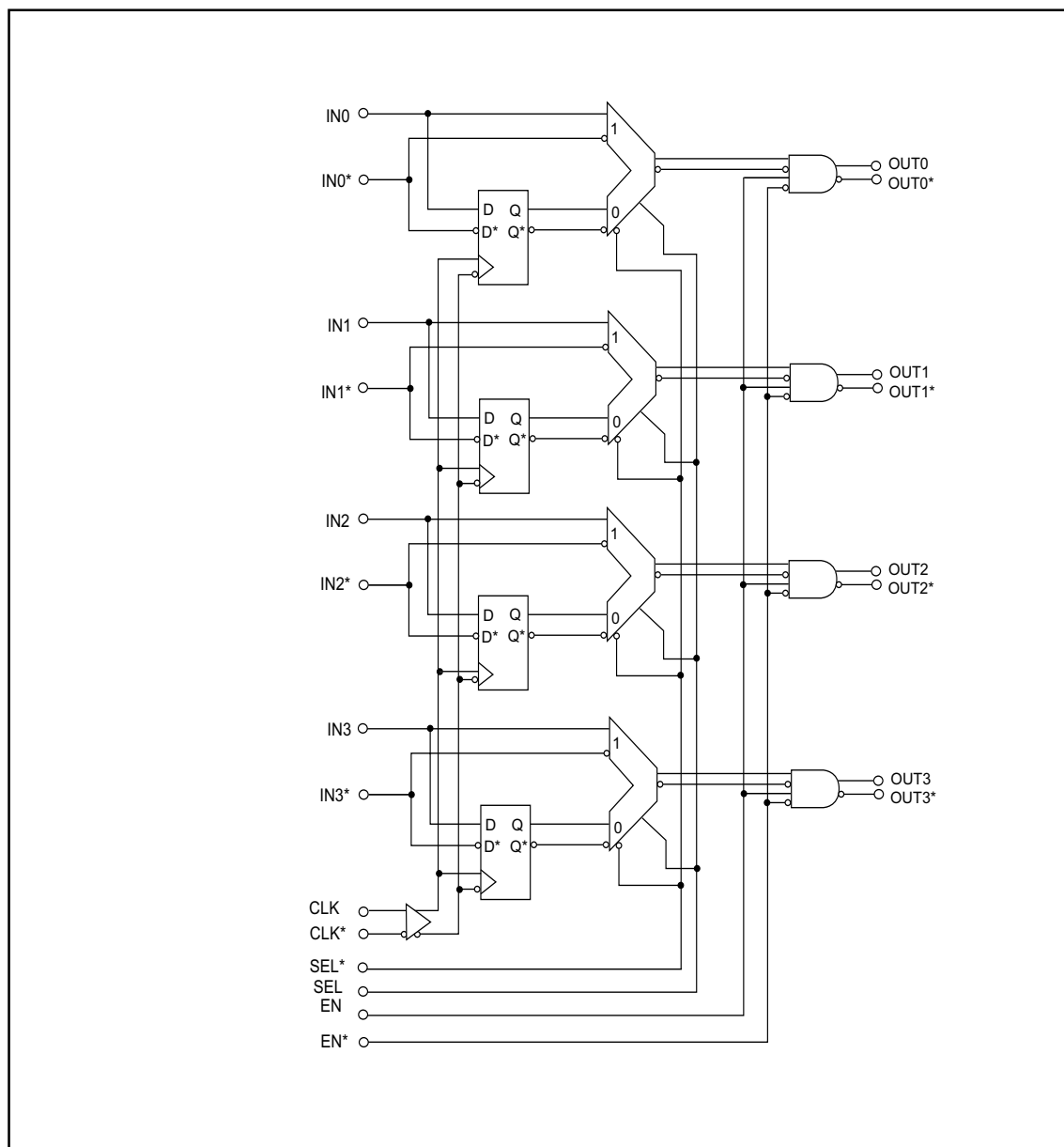


SK44XX Family Functional Block Diagram



SK44XX Family Product Selection Guide

Quad Buffer/Receiver

3 GHz

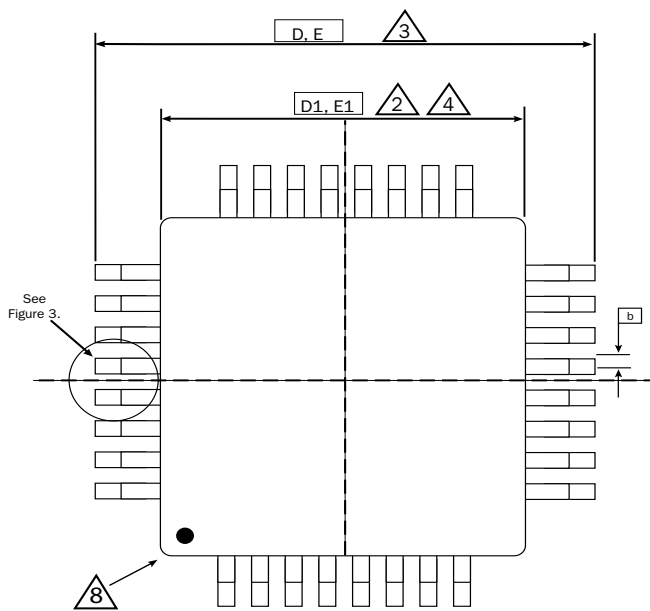
Synch / Asynch Operation

Logic Family

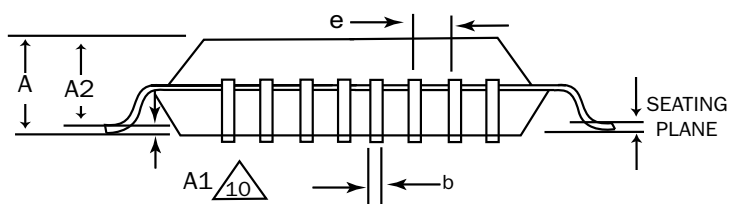
	Power Supply		Input Termination		Output Configuration		Output Swing	Availability
Product	3.3V	5.2V	Open	100Ω	Open Emitter	50Ω Output	Output Swing	
SK4400	●	●	●		●		ECL / PECL	Now
SK4401		●	●		●		Double Swing / TTL	Now
SK4404	●	●	●			●	ECL / PECL	Now
SK4410	●	●		●	●		ECL / PECL	Now
SK4411		●		●	●		Double Swing / TTL	Now
SK4414	●	●		●		●	ECL / PECL	Now

Logic / Translation Family

	Translation	Input Termination		Output Configuration		Availability
Product		Open	100Ω	Open Emitter	50Ω Output	
SK4425	Anything to PECL	●		●		Now
SK4426	Anything to ECL	●		●		Now
SK4429	Anything to PECL	●			●	Now
SK4430	Anything to ECL	●			●	Now
SK4435	Anything to PECL		●	●		Now
SK4436	Anything to ECL		●	●		Now
SK4439	Anything to PECL		●		●	Now
SK4440	Anything to ECL		●		●	Now

SK44XX Family Package Information
5mm x 5mm TQFP

Top View



Side View

SK44XX Family Package Information (continued)
5mm x 5mm TQFP

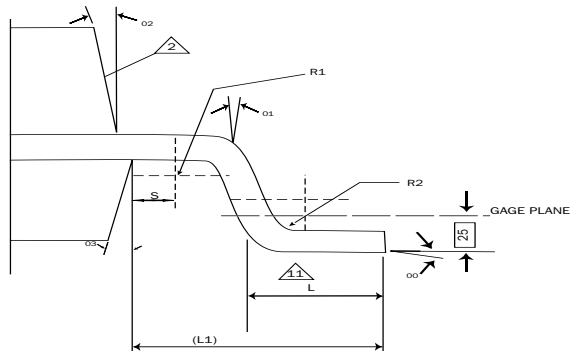


Figure 1.

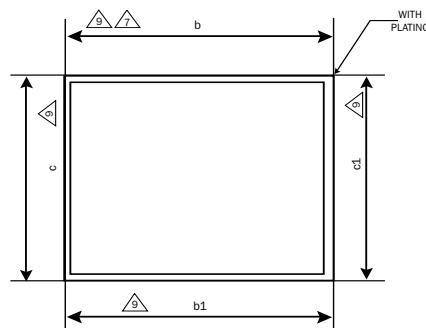


Figure 2.

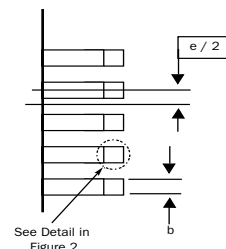


Figure 3.

1. All dimensions and tolerancing conforms to ANSI Y14.5M-1982.
2. The top package body size may be smaller than the bottom package body size by as much as 0.15 mm.
3. To be determined at seating plane.
4. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
5. Details of Pin 1 identifier optional, but must be located within the zone indicated.
6. All dimensions are in millimeters.
7. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
8. Exact shape of each corner is optional.
9. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. A1 is defined as the distance from the seating plane to the lowest point of the package body.

JEDEC Variation All Dimensions in Millimeters					
Symbol	MIN	NOM	MAX	Note	Comments
A	1.00	1.10	1.20		Package Stand Off Height
A1	0.05	0.10	0.15		Air Gap
A2	0.95	1.00	1.05		Package Body Thickness
D	7.00 BSC			3	
D1	5.00 BSC			4, 2	Package Body Length
E	7.00 BSC			3	
E1	5.00 BSC			4, 2	Package Body Width
N	32				Lead Count
e	0.50 BSC				Lead Pitch
b	0.17	0.22	0.27	7	Lead Thickness
b1	0.17	0.20	0.23		
R1	0.08	-	-		
R2	0.08	-	0.20		
O0	0°	3.5°	7°		
O1	0°	-	-		
O2	11°	12°	13°		
O3	11°	12°	13°		
S	0.20	-	-		
c	0.09	-	0.20		
c1	0.09	-	0.16		
L	0.45	0.60	0.75		
L1	1.00 REF				
aaa	0.20				
bbb	0.20				
ccc	0.08				
ddd	0.08				

TEST AND MEASUREMENT PRODUCTS

Absolute Maximum Ratings*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply ($V_{CC} = 0V$)	-8.0 to 0	V
V_{CC}	Power Supply ($V_{EE} = 0V$)	+8.0 to 0	V
V_I	Input Voltage	$V_{CC} \geq V_I \geq V_{EE}$	V
I_{OUT}	Output Current Continuous Surge	50 100	mA mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_{sol}	Solder Temperature (<2 to 3 seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

Note:

1. Device is ESD sensitive and requires protective handling.

TEST AND MEASUREMENT PRODUCTS

Description

The SK4400 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4400 uses standard open emitter ECL outputs optimized for:

- Standard, general purpose ECL applications
- Multiple destinations (daisy chain).

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible
- Available in 32 lead, 5mm X5mm, TQFP Package

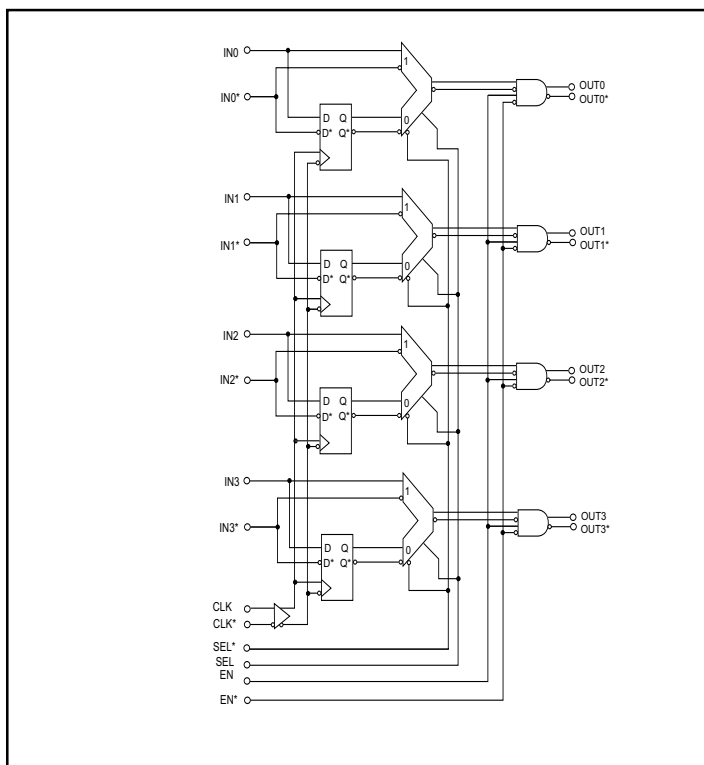
Application Notes

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram



Input Options

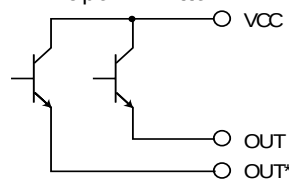
Open

IN<0 - 3> ○

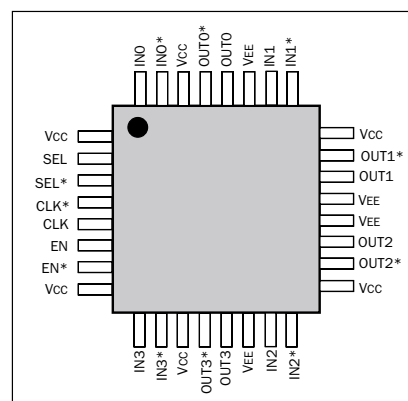
IN<0 - 3>* ○

Output Options

Open Emitter



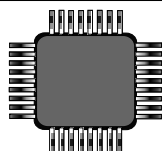
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage 1	VIH - VIL	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	-5.0 -1	+8.0 <0.5	+25 +1	μA μA
Timing Inputs (IN / IN*) Input High Current, Input Low Current	IIH, IIL	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	IIH, IIL	-500	<200	+500	μA
Outputs					
Digital Output Voltage Output Common Mode Range	OUT - OUT* (OUT + OUT*) / 2	600 VCC - 1.5	780 VCC - 1.3	VCC - 1.1	mV V
Power Supply					
Power Supply Current	IEE		90	115	mA

DC TEST CONDITIONS: Outputs terminated with 50Ω to VCC - 2V.

Note 1. Production tested to a maximum Vdiff = 1.8V.

AC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0) SEL to OUT [0:3] EN to OUT [0:3]	Tpd Tpd Tpd Tpd	200 430 300 200	350 550 430 390	550 780 650 600	ps ps ps ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency 1	Fmax	3.0			GHz
Minimum Pulse Width 1	PW min	250			ps
IN to CLK Set Up Time Hold Time	Ts Th	120 120			ps ps
Output Rise and Fall Times (20% / 80%) 1	Tr / Tf		125	165	ps
Temperature Coefficient 1	ΔTpd / ΔT		<1		ps / °C

AC TEST CONDITIONS: Outputs terminated with 50Ω to VCC - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

The SK4401 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4401 uses open emitter outputs with a double amplitude swing suitable for the following applications:

- TTL compatible destinations
- Double termination situations that require a full swing at the destination
- Long cables

Features

- Quad Buffer/Receiver
- 2 GHz Fmax
- 4.5V / 5.2V Compatible
- Available in 32 lead, 5mm X5mm, TQFP Package

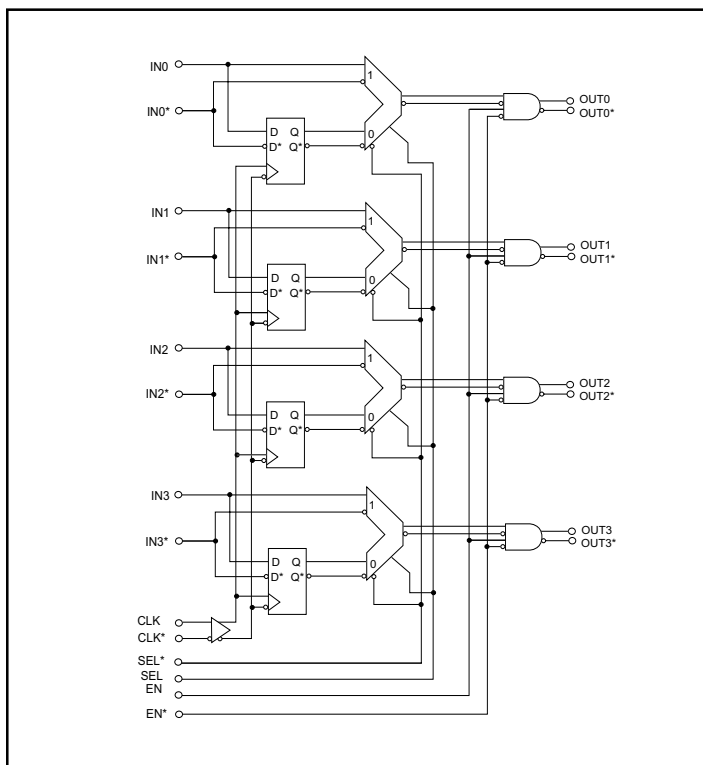
Application Notes

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL / PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram



Input Options

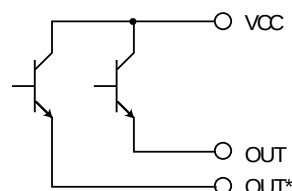
Open

IN<0 - 3> ○ —

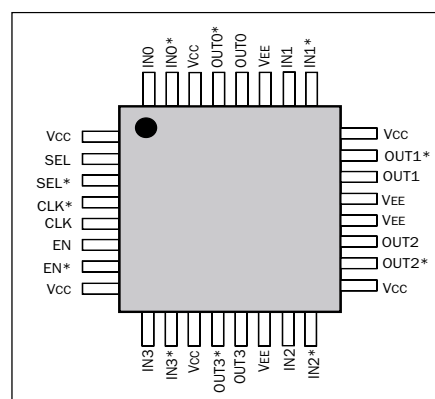
IN<0 - 3>* ○ —

Output Options

Open Emitter



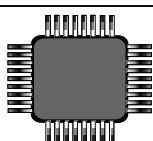
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(VCC - VEE = 4.2V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High Input Low	VIH VIL	VEE + 2.0 VEE		VCC VCC - 0.2	V V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	VIH - VIL	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current Input Low Current	IIH IIL	-5.0 -1	+8.0 <0.5	+25 +1	μA μA
Timing Inputs (IN / IN*) Input High Current, Input Low Current	IIH, IIL	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	IIH, IIL	-500	<200	+500	μA
Outputs					
Digital Output Voltage Output Common Mode Range	OUT - OUT* (OUT + OUT*) / 2	1.2 VCC - 2.2	1.5 VCC - 1.9	VCC - 1.7	V V
Power Supply					
Power Supply Current	IEE		90	115	mA

DC Test Conditions: Outputs terminated with 50Ω to VCC - 3.3V

AC Characteristics

(VCC - VEE = 4.2V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0) SEL to OUT [0:3] EN to OUT [0:3]	Tpd Tpd Tpd Tpd	200 400 300 250	450 650 530 500	800 950 850 850	ps ps ps ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency 1	Fmax	2.0			GHz
Minimum Pulse Width 1	PW min	350			ps
IN to CLK Set Up Time Hold Time	Ts Th	120 120			ps ps
Output Rise and Fall Times (20% / 80%) 1	Tr / Tf		200	350	ps
Temperature Coefficient 1	ΔTpd / ΔT		<3		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC - 3.3V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

The SK4404 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4404 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Features

- Quad Buffer/Driver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible
- Available in 32 lead, 5mm X5mm, TQFP Package

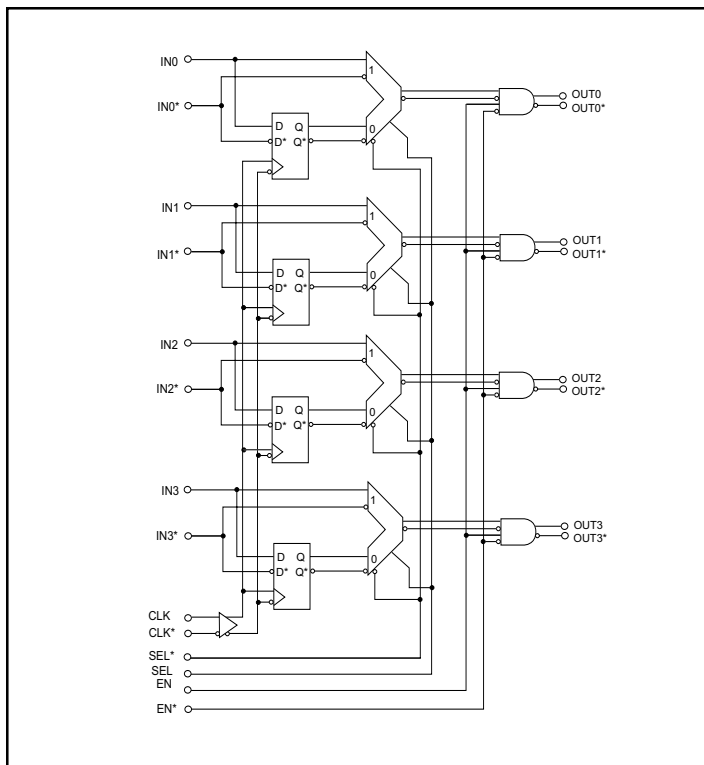
Application Notes

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

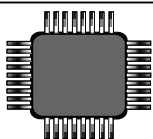
Functional Block Diagram



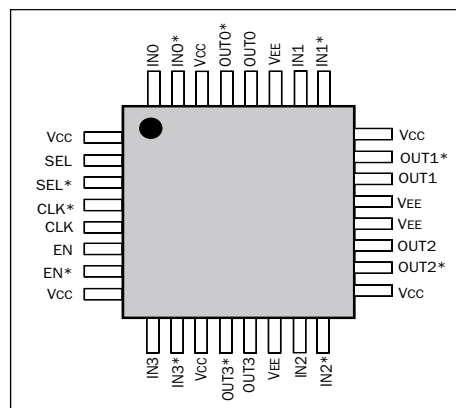
Package Information

32 pin, 5 mm X 5 mm

TQFP Package



Pin Description



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	VIH	VEE + 2.0		VCC	V
Input Low	VIL	VEE		VCC - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	VIH - VIL	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current	IIH	-5.0	+8.0	+25	μA
Input Low Current	IIL	-1	<0.5	+1	μA
Timing Inputs (IN / IN*) Input High Current, Input Low Current	IIH, IIL	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	IIH, IIL	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	VCC - 1.5	VCC - 1.3	VCC - 1.1	V
Internal Current Source	ISINK	8	10.0	13.5	mA
Output Impedance	ROUT	40	50	60	Ω
Power Supply					
Power Supply Current	IEE		170	225	mA

DC Test Conditions: Outputs unterminated.

AC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1)	Tpd	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	Tpd	430	580	780	ps
SEL to OUT [0:3]	Tpd	300	450	650	ps
EN to OUT [0:3]	Tpd	250	350	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency 1	Fmax	3.0			GHz
Minimum Pulse Width 1	PW min	250			ps
IN to CLK Set Up Time	Ts	120			ps
Hold Time	Th	120			ps
Output Rise and Fall Times (20% / 80%) 1	Tr / Tf		125	165	ps
Temperature Coefficient 1	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	VIH	VEE + 2.0		VCC	V
Input Low	VIL	VEE		VCC - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	VIH - VIL	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I _{IH}	-5.0	+8.0	+25	μA
Input Low Current	I _{IL}	-1	<0.5	+1	μA
IN / IN* Differential Input Resistance	R _{IN}	80	100	120	Ω
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	I _{IH} , I _{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	VCC - 1.5	VCC - 1.3	VCC - 1.1	V
Power Supply					
Power Supply Current	I _{EE}		90	115	mA

DC Test Conditions: Outputs terminated with 50Ω to VCC - 2V.

AC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T _{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T _{pd}	430	550	780	ps
SEL to OUT [0:3]	T _{pd}	300	430	650	ps
EN to OUT [0:3]	T _{pd}	250	360	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency ¹	F _{max}	3.0			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK					
Setup Time	T _s	120			ps
Hold Time	T _h	120			ps
Output rise and Fall Times (20%/80%) ¹	Tr/Tf		125	165	ps
Temperature Coefficient ¹	ΔT _{pd} /ΔT		<1		ps/°C

AC Test Conditions: Outputs terminated with 50Ω to VCC - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

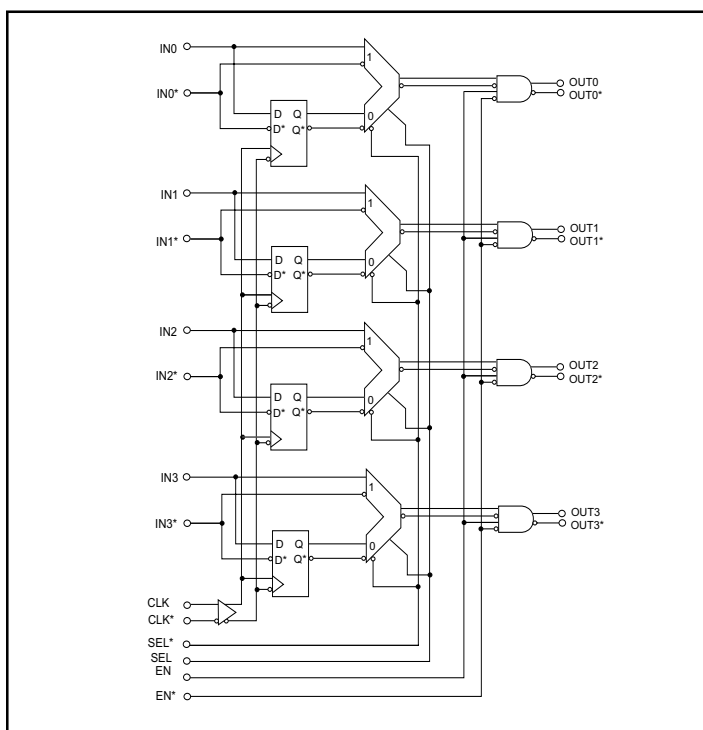
The SK4411 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4411 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4411 uses open emitter outputs with a double amplitude swing suitable for the following applications:

- TTL compatible destinations
- Double termination situations that require a full swing at the destination
- Long cables

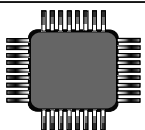
Functional Block Diagram



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



Features

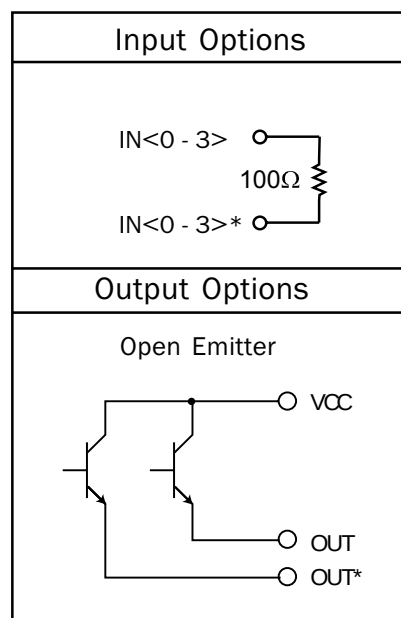
- Quad Buffer/Receiver
- 3 GHz Fmax
- 4.2V / 5.2V Compatible
- Available in 32 lead, 5mm X5mm, TQFP Package

Application Notes

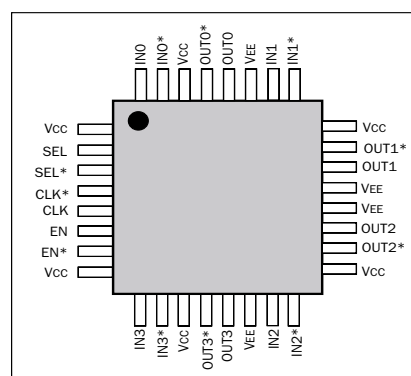
AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



Pin Description



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(VCC - VEE = 4.2V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	VIH	VEE + 2.0		VCC	V
Input Low	VIL	VEE		VCC - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	VIH - VIL	0.2		4.3	V
Timing Inputs (CLK / CLK*) Input High Current	IIH	-5.0	+8.0	+25	μA
Input Low Current	IIL	-1	<0.5	+1	μA
IN / IN* Differential Input Resistance	RIN	80	100	120	Ω
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	IIH, IIL	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	1.2	1.5		V
Output Common Mode Range	(OUT + OUT*) / 2	VCC - 2.2	VCC - 1.9	VCC - 1.7	V
Power Supply					
Power Supply Current	IEE		90	115	mA

DC Test Conditions: Outputs terminated with 50Ω to VCC – 3.3V.

AC Characteristics

(VCC - VEE = 4.2V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1)	Tpd	200	450	800	ps
CLK to OUT[0:3] (SEL = 0)	Tpd	400	650	950	ps
SEL to OUT [0:3]	Tpd	300	530	850	ps
EN to OUT [0:3]	Tpd	250	500	850	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency 1	Fmax	3.0			GHz
Minimum Pulse Width1	PW min	350			ps
IN to CLK Set Up Time	Tsu	120			ps
Hold Time	Th	120			ps
Output Rise and Fall Times (20% / 80%) 1	Tr / Tf		200	350	ps
Temperature Coefficient 1	ΔTpd /ΔT		<3		ps/°C

AC Test Conditions: Outputs terminated with 50Ω to VCC – 3.3V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

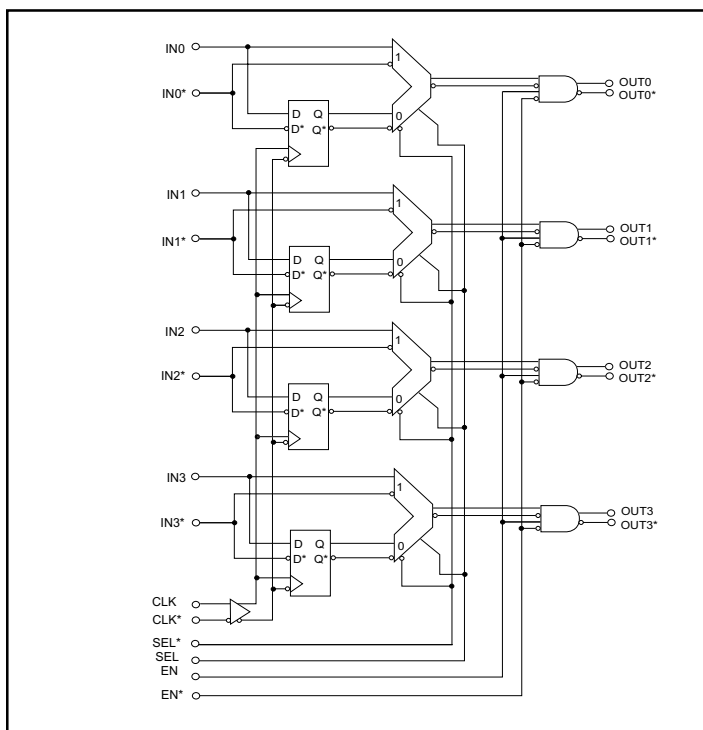
The SK4414 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input.

The SK4414 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4414 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

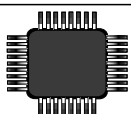
- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Functional Block Diagram



Package Information

32 pin, 5 mm X 5 mm
 TQFP Package



Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- 3.3V / 5.2V Compatible
- Available in 32 lead, 5mm X5mm, TQFP Package

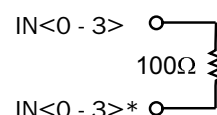
Application Notes

AN1001 - EPIC Family Product Line

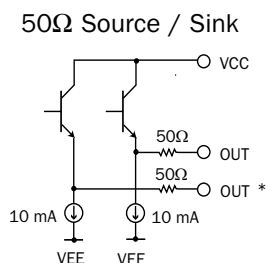
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

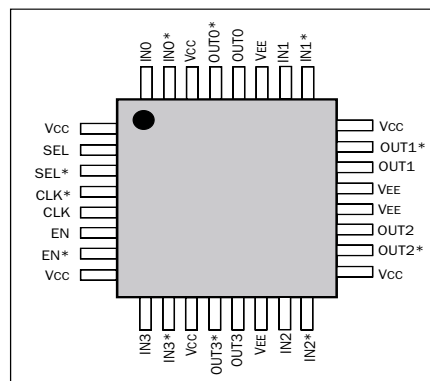
Input Options



Output Options



Pin Description



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	VIH	VEE + 2.0		VCC	V
Input Low	VIL	VEE		VCC - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	VIH - VIL	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	IIH	-5.0	+8.0	+25	μA
Input Low Current	IIL	-1	<0.5	+1	μA
IN / IN* Differential Input Resistance	RIN	80	100	120	Ω
Functional Inputs (EN / EN*, SEL / SEL*)					
Input Current	IIH, IIL	-500		+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	VCC - 1.5	VCC - 1.3	VCC - 1.1	V
Internal Current Source	ISINK	8.0	10.0	13.5	mA
Output Impedance	ROUT	40	50	60	Ω
Power Supply					
Power Supply Current	IEE		170	220	mA

DC Test Conditions: Outputs unterminated.

AC Characteristics

(VCC - VEE = 3.0V to 5.5V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	Tpd	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	Tpd	430	550	780	ps
SEL to OUT [0:3]	Tpd	300	430	650	ps
EN to OUT [0:3]	Tpd	250	360	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency ¹	Fmax	3.0			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK					
Set Up Time	Ts	120			ps
Hold Time	Th	120			ps
Output Rise and Fall Times (20% / 80%) ¹	Tr / Tf		125	165	ps
Temperature Coefficient ¹	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

The SK4425 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4425 uses standard open emitter ECL outputs optimized for:

- Standard, general purpose ECL applications
- Multiple destinations (daisy chain).

Features

- Quad Buffer / Receiver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

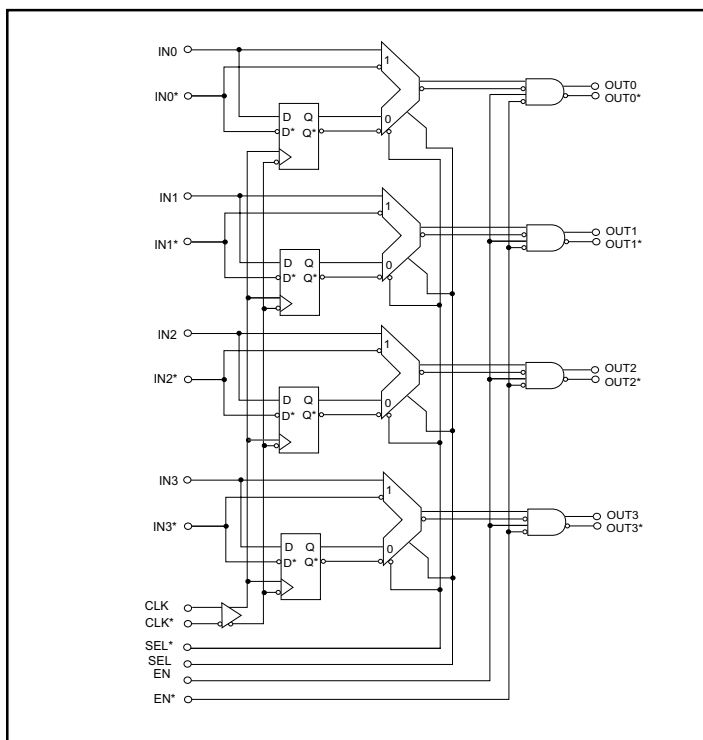
Application Notes

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL
 PECL / LVPECL Devices

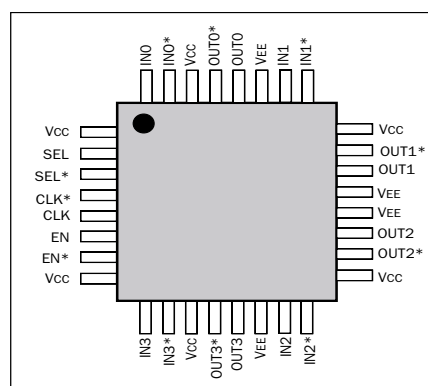
AN1004 - Interfacing Between LVDS and ECL /
 LVECL / PECL / LVPECL

Functional Block Diagram

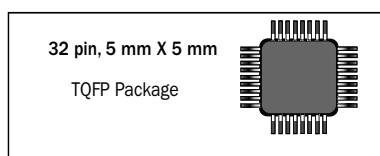


Input Options	Output Options
Open IN<0 - 3> ○ IN<0 - 3>* ○	Open Emitter

Pin Description



Package Information



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(VCC = 2.0V to 3.6V; VEE = -3.6 to -3.0V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	VIH	VEE + 2.0		VCC	V
Input Low	VIL	VEE		VCC -0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	VIH - VIL	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	IIH	- 5.0	+8.0	+25	μA
Input Low Current	IIL	-1	<0.5	+1	μA
Timing Inputs (IN / IN*) Input High Current, Input Low Current	IIH, IIL	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	IIH, IIL	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	VCC -1.5	VCC -1.3	VCC -1.1	V
Power Supply					
Power Supply Current	IEE		95	120	mA

DC Test Conditions: Outputs terminated with 50Ω to VCC - 2V.

AC Characteristics

(VCC = 2.0V to 3.6V; VEE = -3.6 to -3.0V; TA = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay IN[0:3] to OUT[0:3] (SEL = 1) CLK to OUT[0:3] (SEL = 0) SEL to OUT [0:3] EN to OUT [0:3]	Tpd Tpd Tpd Tpd	200 430 250 200	350 550 430 390	550 780 650 600	ps ps ps ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency ¹	Fmax	3.0			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK Set Up Time Hold Time	Ts Th	120 120			ps ps
Output Rise and Fall Times (20% / 80%) ¹	Tr / Tf		125	165	ps
Temperature Coefficient ¹	ΔTpd / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to VCC - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

The SK4426 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4426 uses standard open emitter ECL outputs optimized for:

- Standard, general purpose ECL applications
- Multiple destinations (daisy chain).

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

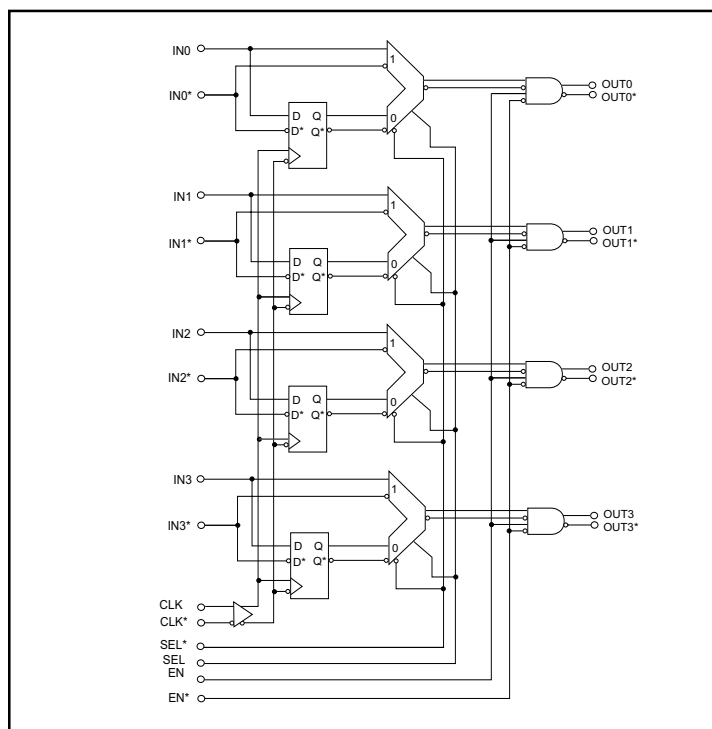
Application Notes

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

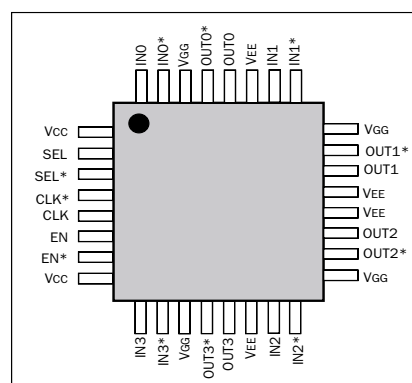
AN1004 - Interfacing Between LVDS and ECL / PECL / LVPECL

Functional Block Diagram



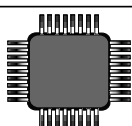
Input Options	Output Options
Open	Open Emitter
IN<0 - 3>	VGG
IN<0 - 3>*	OUT
	OUT*

Pin Description



Package Information

32 pin, 5 mm X 5 mm
TQFP Package



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V _{IH}	V _{EE} + 2.0		V _{CC}	V
Input Low	V _{IL}	V _{EE}		V _{CC} - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	V _{IH} - V _{IL}	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I _{IH}	-5.0	+8.0	+25	μA
Input Low Current	I _{IL}	-1	<0.5	+1	μA
Timing Inputs (IN / IN*)					
Input High Current, Input Low Current	I _{IH} , I _{IL}	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*)					
Input Current	I _{IH} , I _{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	V _{GG} - 1.5	V _{GG} - 1.3	V _{GG} - 1.1	V
Power Supply					
Power Supply Current	I _{EE} I _{CC}		100 70	150 110	mA mA

DC Test Conditions: Outputs terminated with 50Ω to V_{GG} - 2V.

AC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T _{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T _{pd}	430	550	780	ps
SEL to OUT [0:3]	T _{pd}	300	430	650	ps
EN to OUT [0:3]	T _{pd}	250	390	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency ¹	F _{max}	3			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK					
Set Up Time	T _s	120			ps
Hold Time	T _h	120			ps
Output Rise and Fall Times (20% / 80%) ¹	T _r / T _f		125	165	ps
Temperature Coefficient ¹	ΔT _{pd} / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to V_{GG} - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

The SK4429 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4429 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

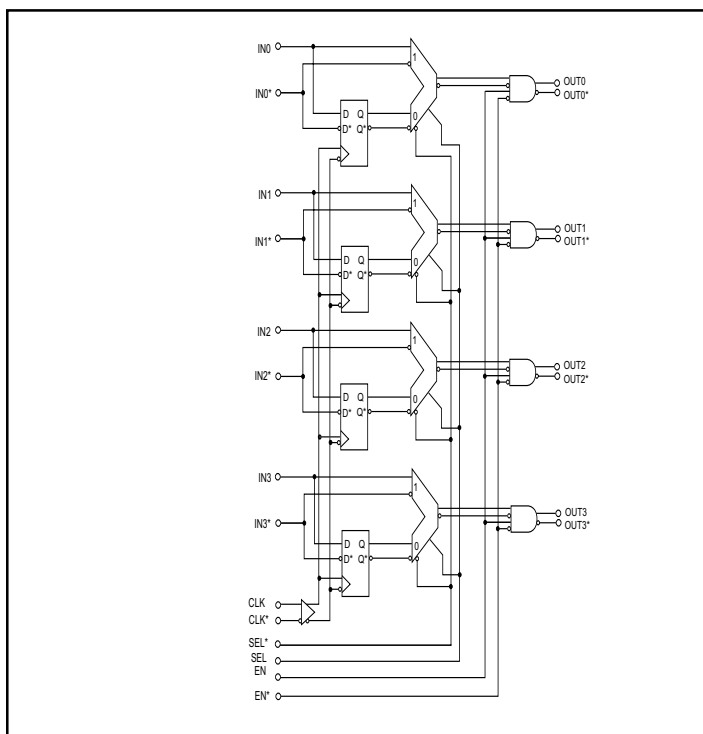
Application Notes

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

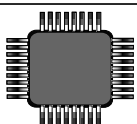
Functional Block Diagram



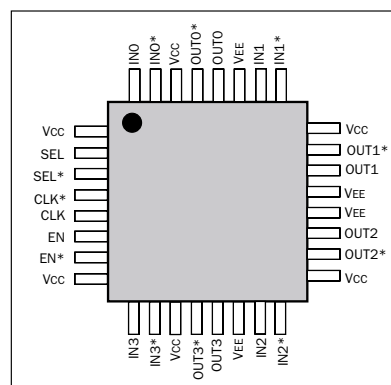
Package Information

32 pin, 5 mm X 5 mm

TQFP Package



Pin Description



Input Options	Output Options
Open	50Ω Source / Sink
IN<0 - 3>	
IN<0 - 3>*	

TEST AND MEASUREMENT PRODUCTS

DC Characteristics

($V_{CC} = 2.0V$ to $3.6V$; $V_{EE} = -3.6V$ to $-3.0V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V_{IH}	$V_{EE} + 2.0$		V_{CC}	V
Input Low	V_{IL}	V_{EE}		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I_{IH}	-5.0	+8.0	+25	μA
Input Low Current	I_{IL}	-1	<0.5	+1	μA
Timing Inputs (IN / IN*)					
Input High Current, Input Low Current	I_{IH}, I_{IL}	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*) Input Current	I_{IH}, I_{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	$ OUT - OUT^* $	600	780		mV
Output Common Mode Range	$(OUT + OUT^*) / 2$	$V_{CC} - 1.5$	$V_{CC} - 1.3$	$V_{CC} - 1.1$	V
Internal Current Source	I_{SINK}	8.0	10.5	13.5	mA
Output Impedance	R_{OUT}	40	50	60	Ω
Power Supply					
Power Supply Current	I_{EE}		170	235	mA

DC Test Conditions: Outputs unterminated.

AC Characteristics

($V_{CC} = 2.0V$ to $3.6V$; $V_{EE} = -3.6V$ to $-3.0V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T_{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T_{pd}	430	580	780	ps
SEL to OUT [0:3]	T_{pd}	300	450	650	ps
EN to OUT [0:3]	T_{pd}	250	350	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency ¹	F_{max}	3			GHz
Minimum Pulse Width ¹	PW_{min}	250			ps
IN to CLK					
Set Up Time	T_s	120			ps
Hold Time	T_h	120			ps
Output Rise and Fall Times (20% / 80%) ¹	T_r / T_f		125	165	ps
Temperature Coefficient ¹	$\Delta T_{pd} / \Delta T$		<1		ps / $^{\circ}C$

AC Test Conditions: Outputs terminated with 50Ω to $V_{CC} - 2V$

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

The SK4430 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4430 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

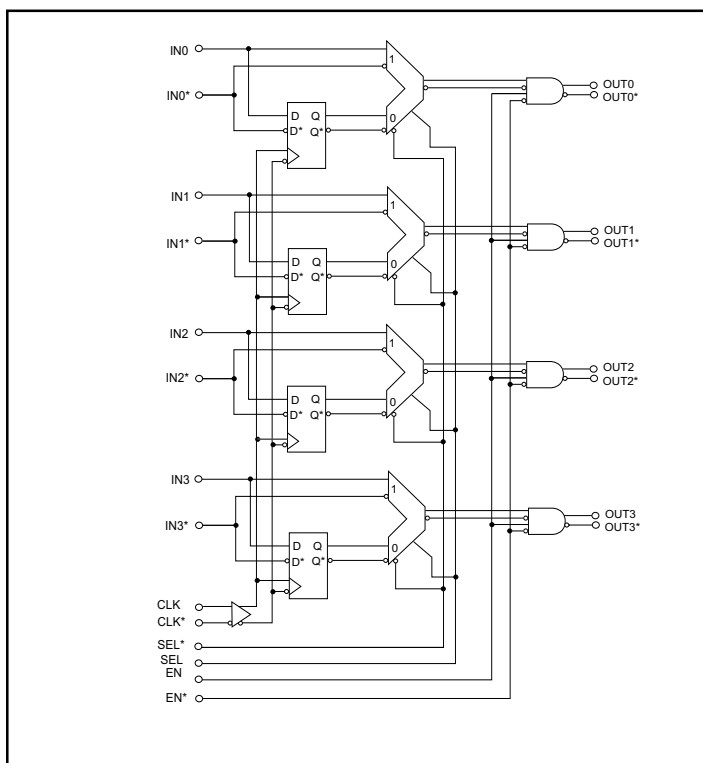
Application Notes

AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

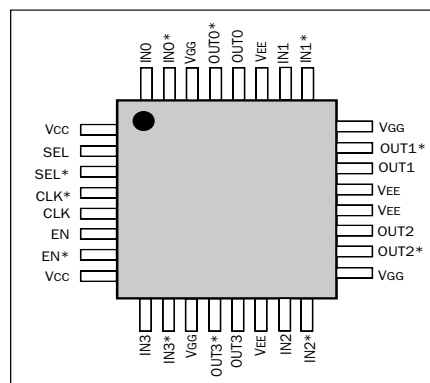
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram



Input Options	Output Options
Open	50Ω Source / Sink
IN<0 - 3> ○	
IN<0 - 3>* ○	

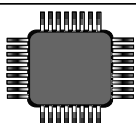
Pin Description



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

($V_{GG} = -0.1V$ to $2.0V$; $V_{CC} = 2.0V$ to $3.6V$; $V_{EE} = -3.6V$ to $-3.0V$; $T_A = 0^\circ C$ to $70^\circ C$)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V_{IH}	$V_{EE} + 2.0$		V_{CC}	V
Input Low	V_{IL}	V_{EE}		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	$ V_{IH} - V_{IL} $	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I_{IH}	-5.0	+8.0	+25	μA
Input Low Current	I_{IL}	-1	<0.5	+1	μA
Timing Inputs (IN / IN*)					
Input High Current, Input Low Current	I_{IH}, I_{IL}	-20	<40	80	μA
Functional Inputs (EN / EN*, SEL / SEL*)					
Input Current	I_{IH}, I_{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	$ OUT - OUT^* $	600	780		mV
Output Common Mode Range	$(OUT + OUT^*) / 2$	$V_{GG} - 1.5$	$V_{GG} - 1.3$	$V_{GG} - 1.1$	V
Internal Current Source	I_{SINK}	8.0	10.0	13.5	mA
Output Impedance	R_{OUT}	40	50	60	Ω
Power Supply					
Power Supply Current	I_{EE} I_{CC}		190 70	250 110	mA mA

DC Test Conditions: Outputs unterminated.

AC Characteristics

($V_{GG} = -0.1V$ to $2.0V$; $V_{CC} = 2.0V$ to $3.6V$; $V_{EE} = -3.6V$ to $-3.0V$; $T_A = 0^\circ C$ to $70^\circ C$)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T_{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T_{pd}	430	550	780	ps
SEL to OUT [0:3]	T_{pd}	300	430	650	ps
EN to OUT [0:3]	T_{pd}	250	390	600	ps
Channel to Channel Skew			40	80	ps
Maximum Operating Frequency ¹	F_{max}	3.0			GHz
IN to CLK ¹					
Setup Time	T_s	120			ps
Hold Time	T_h	120			ps
Output rise and Fall Times (20%/80%) ¹	T_r/T_f		125	165	ps
Temperature Coefficient ¹	$\Delta T_{pd}/\Delta T$		<1		ps/ $^\circ C$

AC Test Conditions: Outputs terminated with 50Ω to $V_{GG} - 2V$

Note 1. Guaranteed by characterization. Not production tested.

Description

- Standard, general purpose applications
- Multiple destinations (daisy chain).

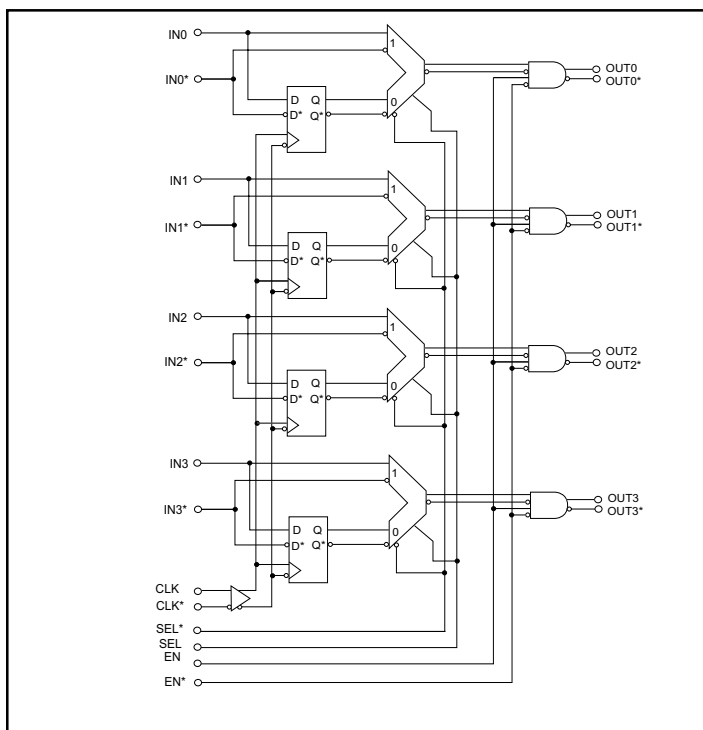
Features

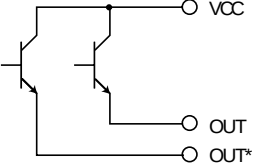
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

Application Notes

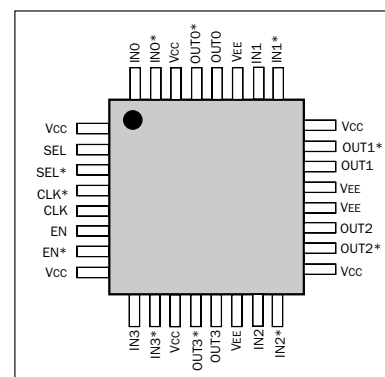
AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL

Functional Block Diagram



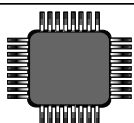
Input Options	Output Options
IN<0 - 3> 	Open Emitter 

Pin Description



Package Information

TQFP Package



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V _{IH}	V _{EE} + 2.0		V _{CC}	V
Input Low	V _{IL}	V _{EE}		V _{CC} - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	V _{IH} - V _{IL}	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I _{IH}	-5.0	+8.0	+25	μA
Input Low Current	I _{IL}	-1	<0.5	+1	μA
IN / IN* Differential Input Resistance	R _{IN}	80	100	120	Ω
Functional Inputs (EN / EN*, SEL / SEL*)					
Input Current	I _{IH} , I _{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	V _{CC} - 1.5	V _{CC} - 1.3	V _{CC} - 1.1	V
Power Supply					
Power Supply Current	I _{EE}		85	120	mA

DC Test Conditions: Outputs terminated with 50Ω to V_{CC} - 2V.

AC Characteristics

(V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T _{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T _{pd}	430	550	780	ps
SEL to OUT [0:3]	T _{pd}	300	430	650	ps
EN to OUT [0:3]	T _{pd}	250	360	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency ¹	F _{max}	3			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK					
Set Up Time	T _s	120			ps
Hold Time	T _h	120			ps
Output Rise and Fall Times (20% / 80%) ¹	T _r / T _f		125	165	ps
Temperature Coefficient ¹	ΔT _{pd} / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to V_{CC} - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

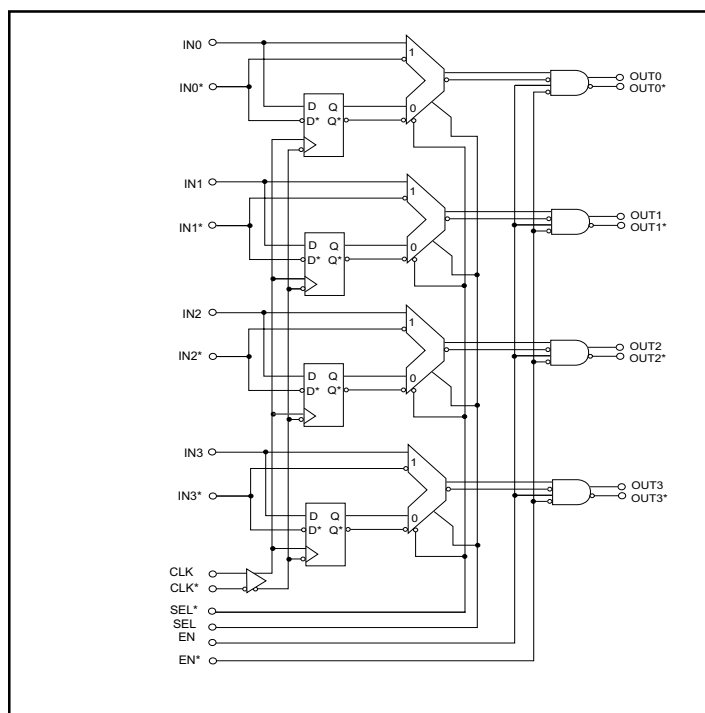
The SK4436 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4436 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

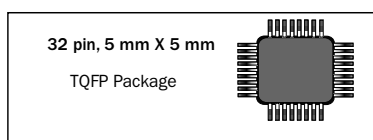
The SK4436 uses standard open emitter ECL outputs optimized for:

- Standard, general purpose applications
- Multiple destinations (daisy chain).

Functional Block Diagram



Package Information



Features

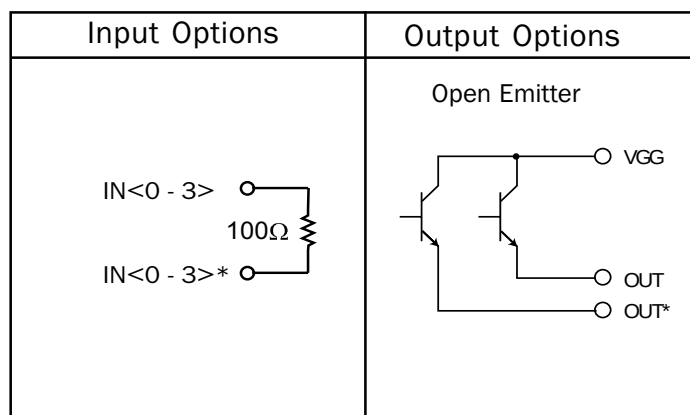
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to ECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

Application Notes

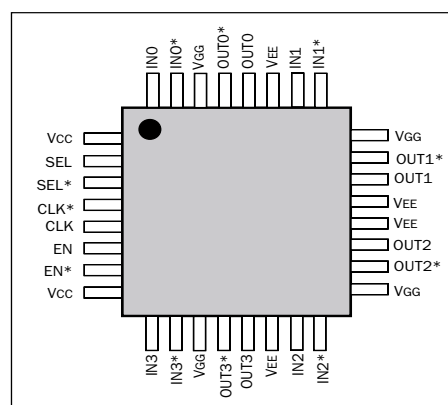
AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



Pin Description



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V _{IH}	V _{EE} + 2.0		V _{CC}	V
Input Low	V _{IL}	V _{EE}		V _{CC} - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	V _{IH} - V _{IL}	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I _{IH}	-5.0	+8.0	+25	μA
Input Low Current	I _{IL}	-1	<0.5	+1	μA
IN / IN* Differential Input Resistance	R _{IN}	80	100	120	Ω
Functional Inputs (EN / EN*, SEL / SEL*)					
Input Current	I _{IH} , I _{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	V _{GG} - 1.5	V _{GG} - 1.3	V _{GG} - 1.1	V
Power Supply					
Power Supply Current	I _{EE} I _{CC}		100 70	150 110	mA mA

DC Test Conditions: Outputs terminated with 50Ω to V_{GG} - 2V.

AC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T _{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T _{pd}	430	550	780	ps
SEL to OUT [0:3]	T _{pd}	300	430	650	ps
EN to OUT [0:3]	T _{pd}	250	390	600	ps
Channel to Channel Skew			40	80	ps
Maximum Operating Frequency ¹	F _{max}	3			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK					
Set Up Time	T _s	120			ps
Hold Time	T _h	120			ps
Output Rise and Fall Times (20% / 80%) ¹	T _r / T _f		125	165	ps
Temperature Coefficient ¹	ΔT _{pd} / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to V_{GG} - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

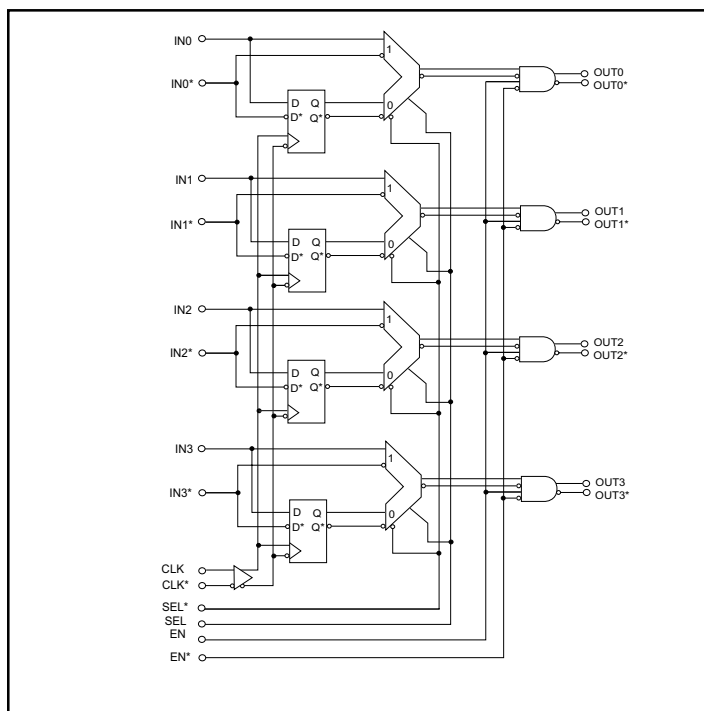
The SK4439 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4439 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4439 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

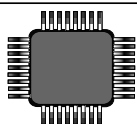
Functional Block Diagram



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



Features

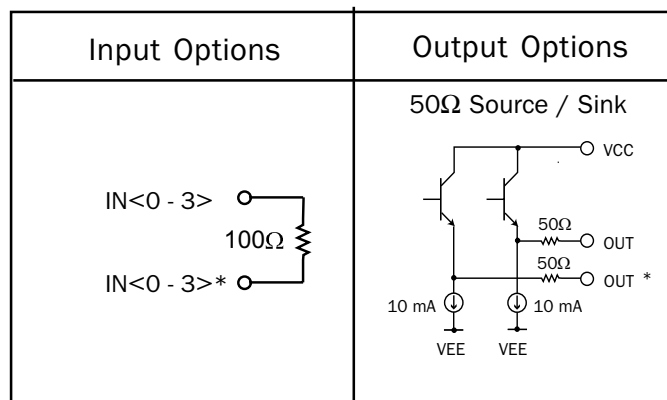
- Quad Buffer/Receiver
- 3 GHz Fmax
- Anything to PECL Translation
- Available in 32 lead, 5mm X5mm, TQFP Package

Application Notes

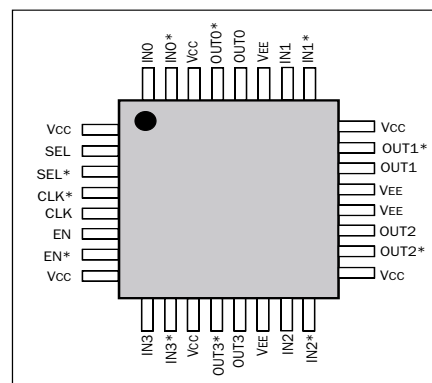
AN1001 - EPIC Family Product Line

AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / PECL / LVPECL



Pin Description



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

($V_{CC} = 2.0V$ to $3.6V$; $V_{EE} = -3.6V$ to $-3.0V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V_{IH}	$V_{EE} + 2.0$		V_{CC}	V
Input Low	V_{IL}	V_{EE}		$V_{CC} - 0.2$	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	$V_{IH} - V_{IL}$	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I _{IH}	-5.0	+8.0	+25	μA
Input Low Current	I _{IL}	-1	<0.5	+1	μA
IN / IN* Differential Input Resistance	R _{IN}	80	100	120	Ω
Functional Inputs (EN / EN*, SEL / SEL*)					
Input Current	I _{IH} , I _{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	$V_{CC} - 1.5$	$V_{CC} - 1.3$	$V_{CC} - 1.1$	V
Internal Current Source	I _{SINK}	8.0	10.0	13.5	mA
Output Impedance	R _{OUT}	40	50	60	Ω
Power Supply					
Power Supply Current	I _{EE}		170	235	mA

DC Test Conditions: Outputs unterminated.

AC Characteristics

($V_{CC} = 2.0V$ to $3.6V$; $V_{EE} = -3.6V$ to $-3.0V$; $T_A = 0^{\circ}C$ to $70^{\circ}C$)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T _{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T _{pd}	430	550	780	ps
SEL to OUT [0:3]	T _{pd}	300	430	650	ps
EN to OUT [0:3]	T _{pd}	250	360	600	ps
Channel to Channel Skew			15	40	ps
Maximum Operating Frequency ¹	F _{max}	3			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK					
Set Up Time	T _s	120			ps
Hold Time	T _h	120			ps
Output Rise and Fall Times (20% / 80%) ¹	Tr / Tf		125	165	ps
Temperature Coefficient ¹	$\Delta T_{pd} / \Delta T$		<1		ps / $^{\circ}C$

AC Test Conditions: Outputs terminated with 50Ω to $V_{CC} - 2V$

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Description

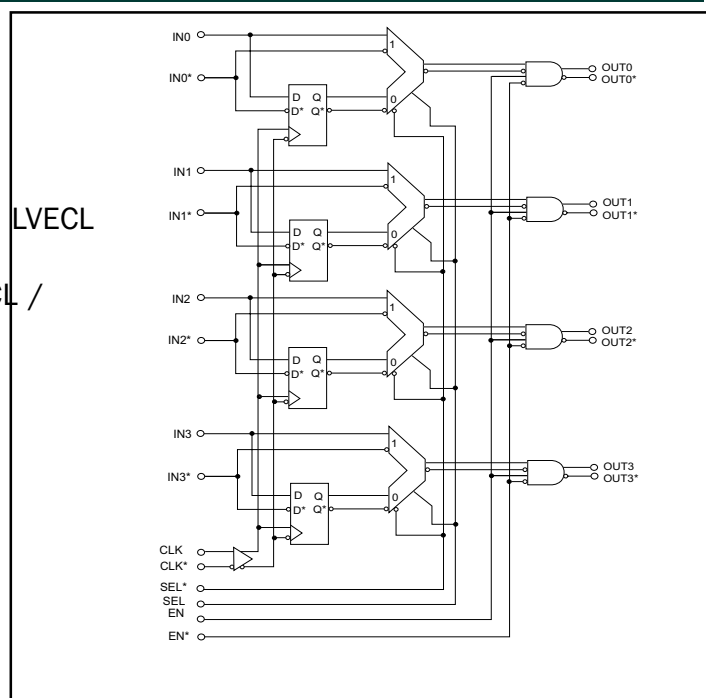
The SK4440 is an extremely fast, stable and accurate low skew quad buffer or cable driver / receiver. It can asynchronously pass four distinct signals, or it can resynchronize them to a common clock. In addition, all four outputs may be asynchronously enabled or disabled. All of the D flip-flops are triggered on the rising edge of the CLK input. It is also capable of receiving inputs of any technology or voltage level.

The SK4440 has 100Ω input termination resistors across each of the four inputs to help reduce system component count and increase integration.

The SK4440 uses 50Ω outputs with sink/source capability, and is optimized for applications that require:

- Point to point, double terminated, timing critical lines
- Point to point, series terminated, timing critical lines

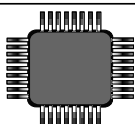
Functional Block Diagram



Package Information

32 pin, 5 mm X 5 mm

TQFP Package



Features

- Quad Buffer/Receiver
- 3 GHz Fmax
- Available in 32 lead, 5mm X5mm, TQFP Package

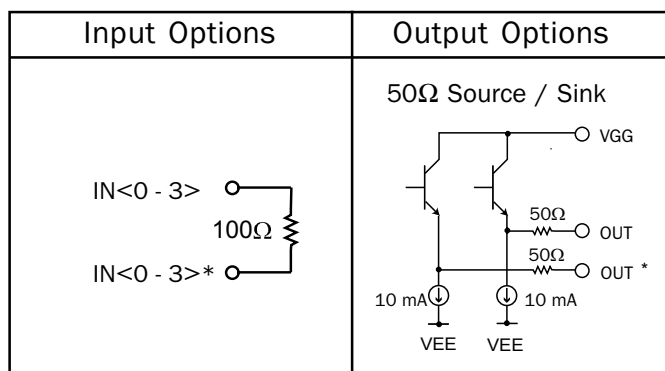
Application Notes

AN1001 - EPIC Family Product Line

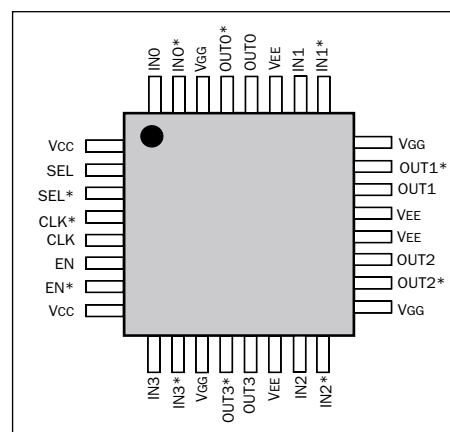
AN1003 - Termination Techniques for ECL / LVECL PECL / LVPECL Devices

AN1004 - Interfacing Between LVDS and ECL / LVECL / ECL / LVPECL

AN1008 - Interfacing with CML



Pin Description



TEST AND MEASUREMENT PRODUCTS

DC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Inputs					
Input High	V _{IH}	V _{EE} + 2.0		V _{CC}	V
Input Low	V _{IL}	V _{EE}		V _{CC} - 0.2	V
(IN - IN*, CLK - CLK*, EN - EN*, SEL - SEL*) Differential Input Voltage	V _{IH} - V _{IL}	0.2		4.3	V
Timing Inputs (CLK / CLK*)					
Input High Current	I _{IH}	-5	+8.0	+25	μA
Input Low Current	I _{IL}	-1	<0.5	+1	μA
IN / IN* Differential Input Resistance	R _{IN}	80	100	120	Ω
Functional Inputs (EN / EN*, SEL / SEL*)					
Input Current	I _{IH} , I _{IL}	-500	<200	+500	μA
Outputs					
Digital Output Voltage	OUT - OUT*	600	780		mV
Output Common Mode Range	(OUT + OUT*) / 2	V _{GG} - 1.5	V _{GG} - 1.3	V _{GG} - 1.1	V
Internal Current Source	I _{SINK}	8.0	10	13.5	mA
Output Impedance	R _{OUT}	40	50	60	Ω
Power Supply					
Power Supply Current	I _{EE} I _{CC}		190 70	250 110	mA mA

DC Test Conditions: Outputs unterminated.

AC Characteristics

(V_{GG} = - 0.1V to 2.0V; V_{CC} = 2.0V to 3.6V; V_{EE} = -3.6V to -3.0V; T_A = 0°C to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
High Performance Option					
Propagation Delay					
IN[0:3] to OUT[0:3] (SEL = 1)	T _{pd}	200	350	550	ps
CLK to OUT[0:3] (SEL = 0)	T _{pd}	430	550	780	ps
SEL to OUT [0:3]	T _{pd}	300	430	650	ps
EN to OUT [0:3]	T _{pd}	250	390	600	ps
Channel to Channel Skew			40	80	ps
Maximum Operating Frequency ¹	F _{max}	3			GHz
Minimum Pulse Width ¹	PW min	250			ps
IN to CLK					
Set Up Time	T _s	120			ps
Hold Time	T _h	120			ps
Output Rise and Fall Times (20% / 80%) ¹	T _r / T _f		125	165	ps
Temperature Coefficient ¹	ΔT _{pd} / ΔT		<1		ps / °C

AC Test Conditions: Outputs terminated with 50Ω to V_{GG} - 2V

Note 1. Guaranteed by characterization. Not production tested.

TEST AND MEASUREMENT PRODUCTS

Ordering Information

Ordering Code	Package ID
SK4400ATF	32-TQFP 5 x 5 mm
SK4401ATF	32-TQFP 5 x 5 mm
SK4404ATF	32-TQFP 5 x 5 mm
SK4410ATF	32-TQFP 5 x 5 mm
SK4411ATF	32-TQFP 5 x 5 mm
SK4414ATF	32-TQFP 5 x 5 mm
SK4425ATF	32-TQFP 5 x 5 mm
SK4426ATF	32-TQFP 5 x 5 mm
SK4429ATF	32-TQFP 5 x 5 mm
SK4430ATF	32-TQFP 5 x 5 mm
SK4435ATF	32-TQFP 5 x 5 mm
SK4436ATF	32-TQFP 5 x 5 mm
SK4439ATF	32-TQFP 5 x 5 mm
SK4440ATF	32-TQFP 5 x 5 mm

Notes:

1. For tape and reel, add the letter "T" at the end of ordering code.
2. For tape and reel information, see TMD Part Ordering Information Data Sheet.

Contact Information

Semtech Corporation
 Test and Measurement Division
 10021 Willow Creek Rd., San Diego, CA 92131
 Phone: (858) 695-1808 FAX: (858) 695-2633