SK6226Bx

Non-Crystal UFD Controller

for 2xnm MLC & TLC

Rev. 0.91

Jul. 29, 2011

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Revision History

Date	Rev	Description
Mar. 1st, 2011	0.10	● Establishment.
Jul. 25, 2011	0.90	● Modify SK6226Ax to SK6226Bx ● Modify 3.0V typo.
Jul. 29, 2011	0.91	● Modify and redraw SK6226Ax typo

Table of Contents

1. Description

The SK6226Bx is a Non-Crystal USB2.0 Flash Disk controller that complies with USB version2.0 specification and USB Mass Storage Class version 1.0 specification. Besides full speed 12 Mbps complied with USB1.1 specification, SK6226Bx can provide a 480 Mbps transfer rate. Designed with an enhanced power control circuit, the SK6226Bx fully complies with USB power specifications for bus-powered devices, making it capable of bus-powered operation.

Besides rich features for UFD application, SK6226Bx is also the best solution for next generation NAND which are manufactured in the most advance technology. In order to interface with 2x/3x nm MLC and TLC, SK6226Bx ECC capability can correct up to 70 bits error.

- **Reliable ECC for 2x nm MLC and TLC**

  SK6226Bx ECC can provide 70-bit/1KB BCH correction code for 2x/3x nm MLC and TLC.

- **Advance Wear Leveling (AWL) to improve P/E cycle of NAND**

- **Saving BOM Cost**

  Because SK6226 did not require an external crystal, it can save BOM cost a lot.

- **Performance & Low Power**

  When single-channel mode enabled, SK6226Bx can reach the theoretical limit at TBD MB/s for read access and TBD MB/s for write access in HDBench.

  In order to meet Vista Premium logo program, SK6226Bx also meet *ReadyBoost*™ requirement. Any UFD with SK6226Bx can easily meet 5 MB/sec throughput for random 4KB reads and 3 MB/sec throughput for random 512KB writes and market the UFD with enhancement for Windows® *ReadyBoost*™.

- **Support 256/384 pages of NAND**

  With our superior designs, SK6226Bx runs smoothly on all available host systems and supports MLC & TLC NAND Flash memories with 4KB and 8KB page and either 128, 192, 256 or 384 pages per block. The SK6226Bx allows the direct connection of up to 8 NAND Flash chips in the configuration of single channel by 8 CE.

Therefore, SK6226Bx will be best choice according to cost per performance.

2. Order Information

Part #	Description	Package
SK6226BAPQC	8 CE, 1 WE, 8-bit data width, Multi-Partition, 1.8V/3.3V VCCq.	64-pin LQFP
SK6226BAPMC4	4 CE, 1 WE, 8-bit data width, Multi-Partition, 1.8V/3.3V VCCq.	48-pin LQFP
SK6226BAWWC	8 CE, 1 WE, 8-bit data width, Multi-Partition, 1.8V/3.3V VCCq.	wafer

3. Features

- Support 2x/3x nm MLC and TLC NAND:
  - 70-bit/1KB BCH error control coding (ECC) for MLC.
  - Sufficient embedded buffer for 8K page NAND in single channel configuration.
  - Total addressing space is 64GB.

- Advance Wear Leveling can improve P/E cycle of NAND.

- Saving BOM cost by removing external crystal.

- Outstanding R/W performance:
  - HDBench: Read:TBD MB/s and Write: TBD MB/s with MLC in single channel.
    Read: TBD MB/s and Write: TBD MB/s with TLC in single channel.
  - *ReadyBoost*™ : >5 MB/sec throughput for random 4KB reads and,
    >3 MB/sec throughput for random 512KB writes

- USB Interface:
  - Complied with high-speed USB 2.0 interface, backward compatible with USB 1.1.
  - Complied with USB Mass Storage Class specification v1.0.
  - Complied with USB bus-powered devices specification.
  - Support HID interface for password entry in non-administrator mode.
  - Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) and Serial Interface Engine (SIE).

- Varieties of Supported NAND:
  - Samsung 21nm MLC, 27nm MLC & TLC, 32 nm TLC.
  - IM 2xnm 8KB/page MLC, 25 nm MLC & TLC.
  - Hynix 26nm MLC, 32 nm TLC.
  - Toshiba 24nm MLC, 32 nm MLC.
  - Kinds of page size: 4KB and 8KB.
  - Kinds of page per block: 128 pages, 192 pages, 256 pages and 384 pages.

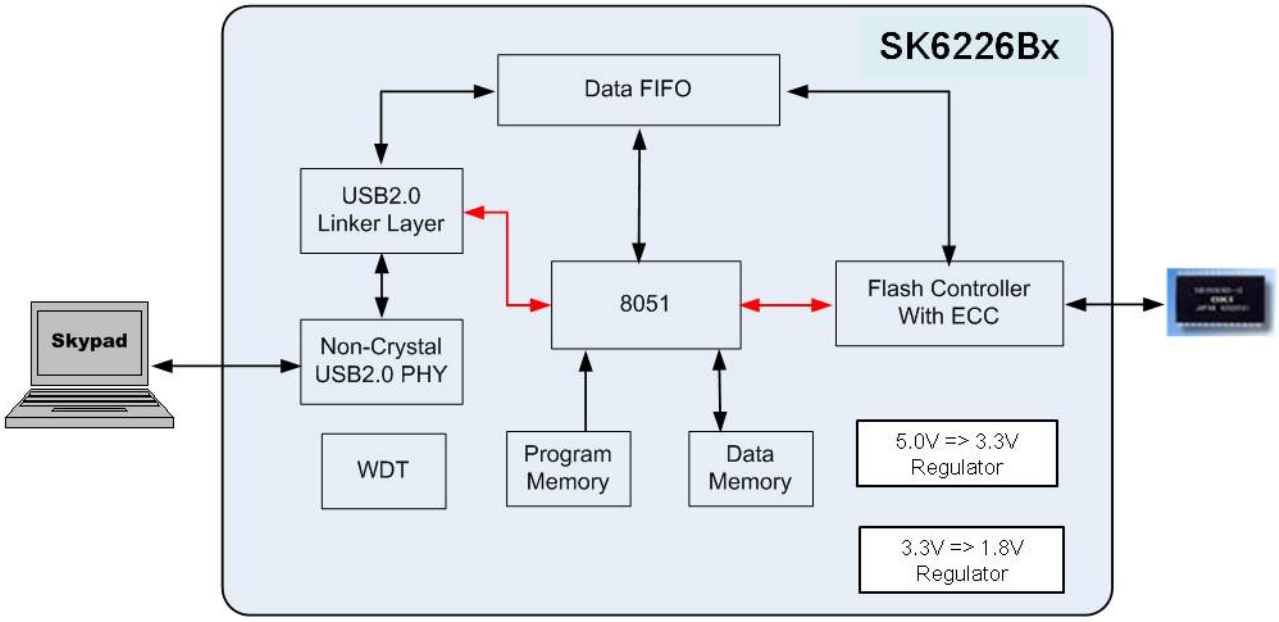
- Async. NAND Interface with 3.3V VCCq:
  - SK6226BAPQC: single channel and 8 CE/channel.
  - SK6226BAPMC4: single channel and 4 CE/channel.

- DDR NAND interface:
  - 1.8V or 3.3V VCCq DDR NAND, either ONFI 2.x NAND or Toggle-mode NAND.
  - SK6226BAPQC: single channel and 8 CE/channel with 1.8V/3.3V VCCq.
  - SK6226BAPMC4: single channel and 4 CE/channel with 1.8V/3.3V VCCq.

- Built-in Watch-Dog Timer (WDT)

- Enable Multi-Partition features:
  - One Read-only Partition, two Read-Write Partitions and one Hidden Partition.
  - Read-only Partition is designated for AutoRun feature.
  - UFD can have up to two LUNs because to two Read-Write Partitions.
  - Each Read-Write Partition can be divided into Public Zone and Private Zone further.
  - Private Zone can be protected by password.
  - Capacity of each Partition and Zone can sizeable while factory initialization or by application program through vendor specific command.

4. Block Diagram

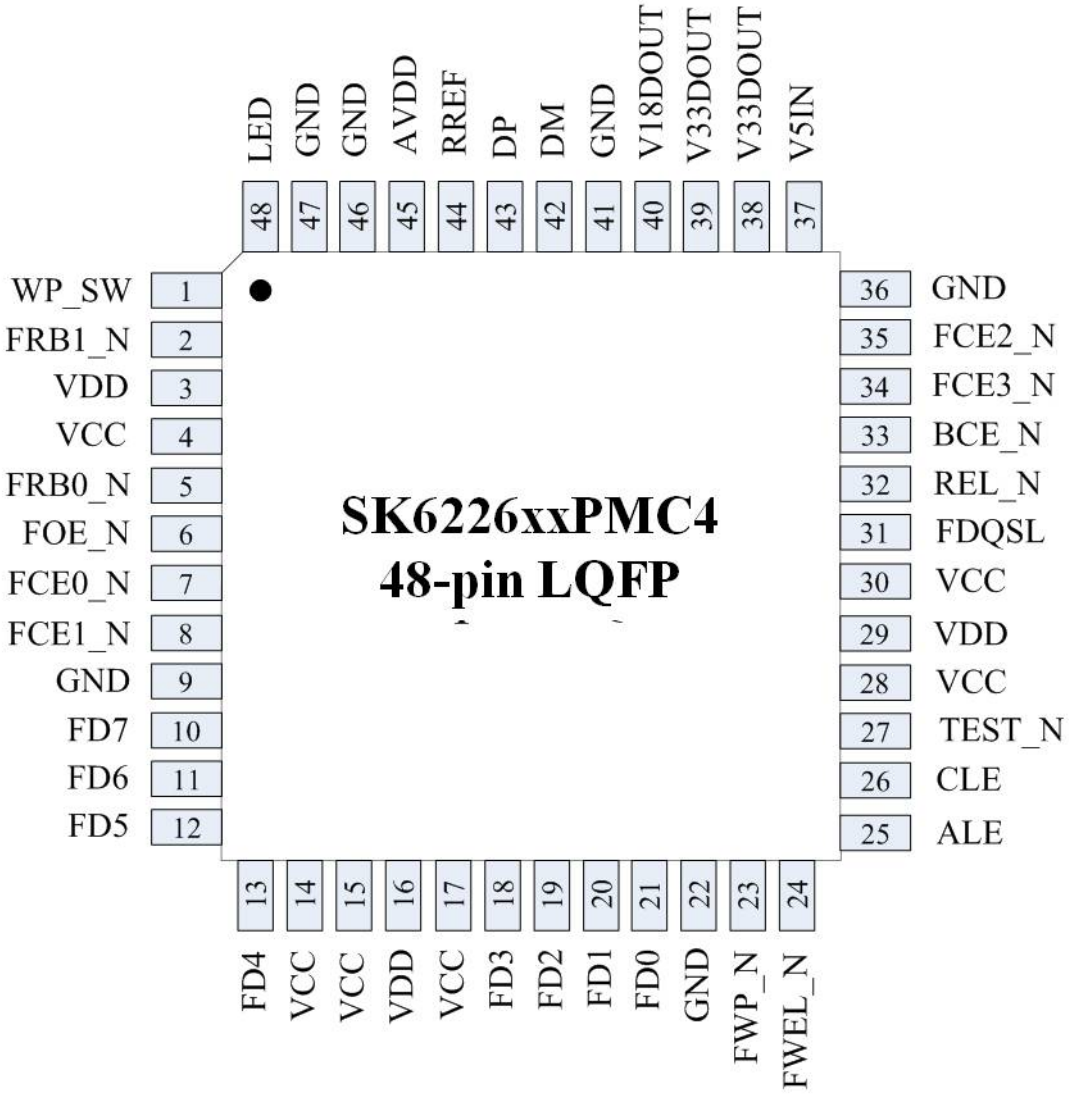


5. Pin Assignment

5.1 48-pin LQFP SK6226xxPMC4

Pin #	Pin Name	Type	Description
1	WP_SW	In	Write protect switch.
2	R/B_1	In	Flash ready/busy 1.
3	VDD	Power In	Core power.
4	VCC	Power In	I/O power.
5	R/B_0	In	Flash ready/busy 0.
6	FNRE	O	Flash output enable.
7	FCE0	O	Flash chip enable 0.
8	FCE1	O	Flash chip enable 1.
9	VSS	Power	Digital ground.
10	FD7	I/O	Flash data bus bit7.
11	FD6	I/O	Flash data bus bit6.
12	FD5	I/O	Flash data bus bit5.
13	FD4	I/O	Flash data bus bit4.
14	VCC	Power In	I/O power.
15	VCC	Power In	I/O power.
16	VDD	Power In	Core power.
17	VCC	Power In	I/O power.
18	FD3	I/O	Flash data bus bit3.
19	FD2	I/O	Flash data bus bit2.
20	FD1	I/O	Flash data bus bit1.
21	FD0	I/O	Flash data bus bit0.
22	VSS	Power	Digital ground.
23	FNWP	O	Flash write protect.
24	FNWE	O	Flash write enable for flash data.
25	FALE	O	Flash address latch enable.
26	FCLE	O	Flash command latch enable.
27	NC	------	No connection for normal use.
28	VCC	Power In	I/O power.
29	VDD	Power In	Core power.

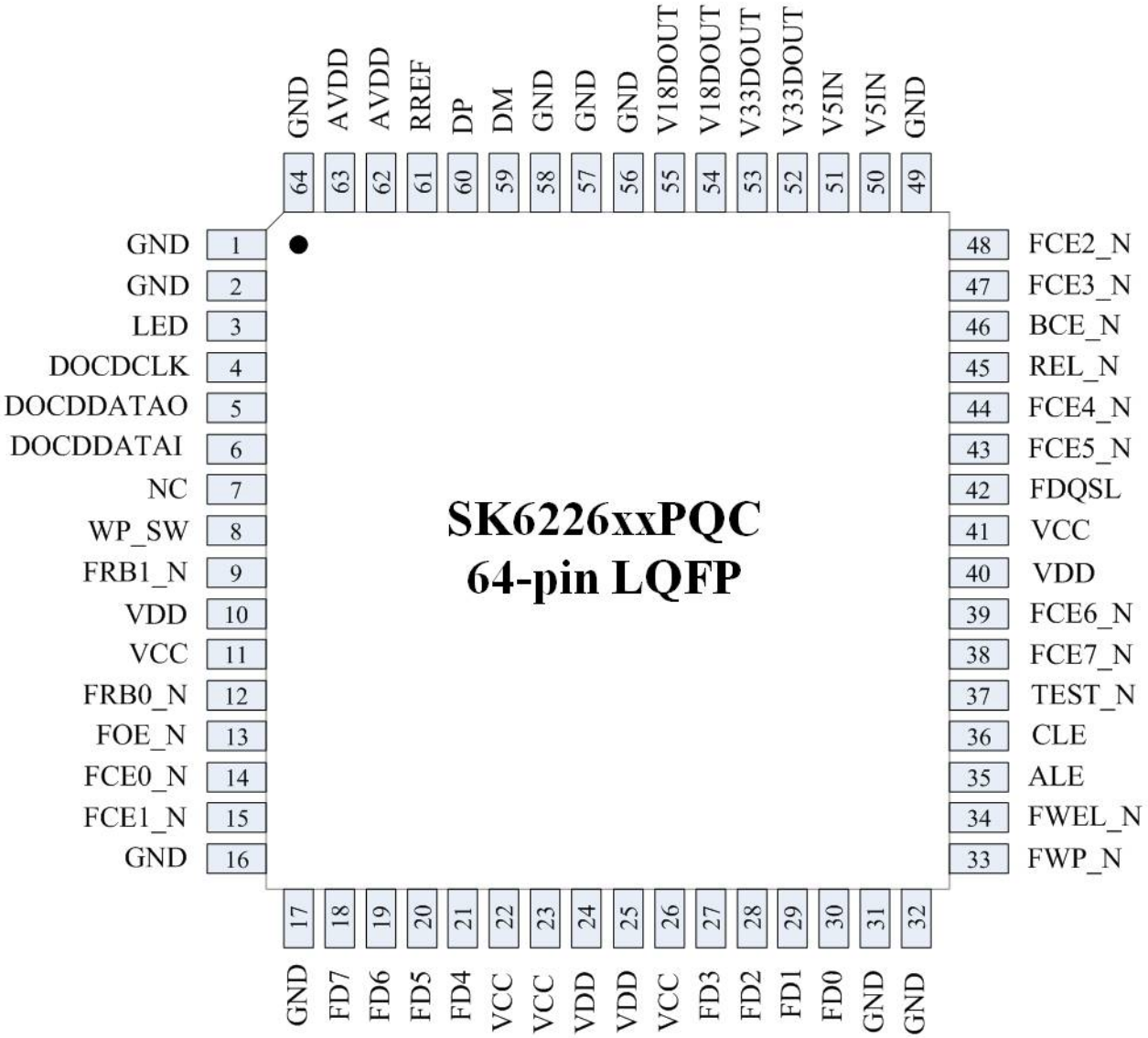
Pin #	Pin Name	Type	Description
30	VCC	Power In	I/O power.
31	FDQS	I/O	Flash DQS pin for DDR flash.
32	NC	------	No connection for normal use. The pin had a default pull-up resistor.
33	NC	------	No connection for normal use. The pin had a default pull-up resistor.
34	FCE3	O	Flash chip enable 3.
35	FCE2	O	Flash chip enable 2.
36	VSS	Power	Digital ground.
37	VCCA5V	Power In	Vbus 5V power input.
38	V33_OUT	Power Out	Regulated 3.3V power output.
39	V33_OUT	Power Out	Regulated 3.3V power output.
40	V18_OUT	Power out	Regulated 1.8V power output.
41	AGND	Power	Analog ground.
42	DM	I/O	USB D-.
43	DP	I/O	USB D+.
44	RREF	In	USB PHY reference resistor.
45	AVDD	Power In	Analog 3.3V input.
46	AGND	Power	Analog ground.
47	VSS	Power	Digital ground.
48	LED	O	LED output.



5.2 64-pin LQFP SK6226xxPQC

Pin #	Pin Name	Type	Description
1	VSS	Power	Digital ground.
2	VSS	Power	Digital ground.
3	LED	O	LED output.
4	NC	------	No connection for normal use.
5	NC	------	No connection for normal use.
6	NC	------	No connection for normal use.
7	NC	------	No connection for normal use.
8	WP_SW	In	Write protect switch.
9	R/B_1	In	Flash ready/busy 1.
10	VDD	Power In	Core power.
11	VCC	Power In	I/O power.
12	R/B_0	In	Flash ready/busy 0.
13	FNRE	O	Flash output enable.
14	FCE0	O	Flash chip enable 0.
15	FCE1	O	Flash chip enable 1.
16	VSS	Power	Digital ground.
17	VSS	Power	Digital ground.
18	FD7	I/O	Flash data bus bit7.
19	FD6	I/O	Flash data bus bit6.
20	FD5	I/O	Flash data bus bit5.
21	FD4	I/O	Flash data bus bit4.
22	VCC	Power In	I/O power.
23	VCC	Power In	I/O power.
24	VDD	Power In	Core power.
25	VDD	Power In	Core power.
26	VCC	Power In	I/O power.
27	FD3	I/O	Flash data bus bit3.
28	FD2	I/O	Flash data bus bit2.
29	FD1	I/O	Flash data bus bit1.
30	FD0	I/O	Flash data bus bit0.
31	VSS	Power	Digital ground.
32	VSS	Power	Digital ground.
33	FNWP	O	Flash write protect.
34	FNWE	O	Flash write enable for flash data.
35	FALE	O	Flash address latch enable.
36	FCLE	O	Flash command latch enable.
37	NC	------	No connection for normal use.
38	FCE7	O	Flash chip enable 7.
39	FCE6	O	Flash chip enable 6.
40	VDD	Power In	Core power.
41	VCC	Power In	I/O power.
42	FDQS	I/O	Flash DQS pin for DDR flash.
43	FCE5	O	Flash chip enable 5.
44	FCE4	O	Flash chip enable 4.
45	NC	------	No connection for normal use. The pin had a default pull-up resistor.
46	NC	------	No connection for normal use. The pin had a default pull-up resistor.
47	FCE3	O	Flash chip enable 3.
48	FCE2	O	Flash chip enable 2.
49	VSS	Power	Digital ground.
50	VCCA5V	Power In	Vbus 5V power input.
51	VCCA5V	Power In	Vbus 5V power input.
52	V33_OUT	Power Out	Regulated 3.3V power output.
53	V33_OUT	Power Out	Regulated 3.3V power output.
54	V18_OUT	Power out	Regulated 1.8V power output.

Pin #	Pin Name	Type	Description
55	V18_OUT	Power out	Regulated 1.8V power output.
56	VSSA	Power	Internal regulator analog ground.
57	AGND	Power	Analog ground.
58	AGND	Power	Analog ground.
59	DM	I/O	USB D-.
60	DP	I/O	USB D+.
61	RREF	In	USB PHY reference resistor.
62	AVDD	Power In	Analog 3.3V input.
63	AVDD	Power In	Analog 3.3V input.
64	AGND	Power	Analog ground.



6. Electrical Specifications

6.1 Absolute Maximum Ratings

Following table shows SK6226Bx stress ratings only. Extended exposure to the maximum ratings might degrade device reliability. Although has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

Symbol	Parameter	Min	Max	Unit
Tstorage	Storage Temperature	- 40	+125	°C
Ta	Ambient Operating Temperature, Commercial	0	70	°C
V_{AVDD}	Analog 3.3V Input Voltage	- 0.3	3.6	V
V_{VCC}, V_{VDD}	Digital 3.3V Input Voltage	- 0.3	3.6	V
V_{VCCA5V}	USB +5.0V Input Voltage	-----	5.25	V

6.2 DC Characteristics

Unless otherwise noted, all test conditions are as follows:

GND=0V, VCC, VDD =3.3V±10%, V18_OUT=1.8V±10%, Ta=25°C.

Symbol	Description	Min.	Typ.	Max.	Unit
V_{AVDD}	Analog 3.3V Input Voltage	3.0	3.3	3.6	V
V_{VCC}, V_{VDD}	Digital 3.3V Input Voltage	3.0	3.3	3.6	V
V_{VCCA5V}	USB +5.0V Input Voltage	4.40	5.0	5.25	V
V_{V33_out}	Regulated 3.3V Output Voltage		3.3		V
V_{V18_out}	Regulated 1.8V Output Voltage		1.8		V
V_{IH}	Input Voltage High	0.7VCC		VCC+0.3	V
V_{IL}	Input Voltage Low	GND-0.3		0.25VCC	V
V_{OH}	Output Voltage High	0.7VCC			V
V_{OL}	Output Voltage Low			0.125VCC	V
C_{in}	Input Pin Capacitance			10	pF
I_{REG}	5V => 3V regulator supply current @V_{V33_OUT}=3.15V		TBD		mA
I_{DD}	Operating Current		TBD		mA
I_{STD}	Standby Current		TBD		mA

6.3 AC Characteristics, ONFI 2.0 Synchronous Interface

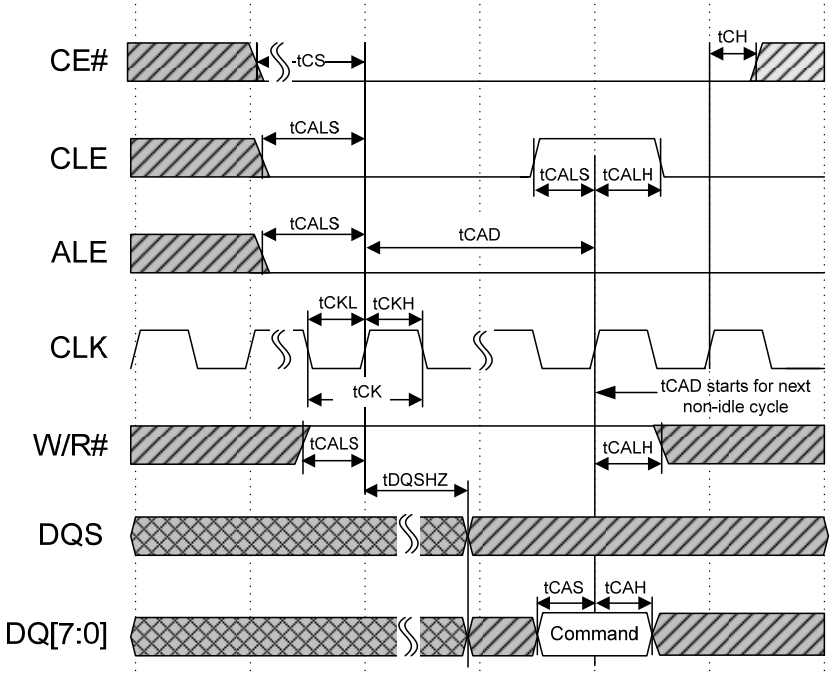
The specification of timing parameters of ONFI 2.0 Source Synchronous modes are listed below. The real AC timing is subjective to change due to FW revision.

Parameter	Mode 0		Mode 1		Mode 2		Unit
	50		30		20		ns
	~20		~33		~50		MHz
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
tAC	—	20	—	20	—	20	ns
tADL	100	—	100	—	70	—	ns
tCADf	25	—	25	—	25	—	ns
tCADs	45	—	45	—	45	—	ns
tCAH	10	—	5	—	4	—	ns
tCALH	10	—	5	—	4	—	ns
tCALS	10	—	5	—	4	—	ns
tCAS	10	—	5	—	4	—	ns
tCH	10	—	5	—	4	—	ns
tCK(avg) or tCK	50	—	30	—	20	—	ns
tCK(abs)	Minimum: tCK(avg) + tJIT(per) min Maximum: tCK(avg) + tJIT(per) max						ns
tCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK
tCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK
tCS	35	—	25	—	15	—	ns
tDH	5	—	2.5	—	1.7	—	ns
tDQSCK	—	20	—	20	—	20	ns
tDQSD	—	20	—	20	—	20	ns
tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tDQSHZ	—	20	—	20	—	20	ns
tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tDQSQ	—	5	—	2.5	—	1.7	ns
tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK
tDS	5	—	3	—	2	—	ns
tDSH	0.2	—	0.2	—	0.2	—	tCK
tDSS	0.2	—	0.2	—	0.2	—	tCK
tDVW	tDVW = tQH – tDQSQ						ns
tFEAT	—	1	—	1	—	1	µs
tHP	tHP = min(tCKL, tCKH)						ns
tITC	—	1	—	1	—	1	µs
tJIT(per)	0.7	0.7	0.7	0.7	0.7	0.7	ns
tQH	tQH = tHP – tQHS						ns
tQHS	—	6	—	3	—	2	ns
tRHW	100	—	100	—	100	—	ns
tRR	20	—	20	—	20	—	ns
tRST	—	5/10/500	—	5/10/500	—	5/10/500	µs

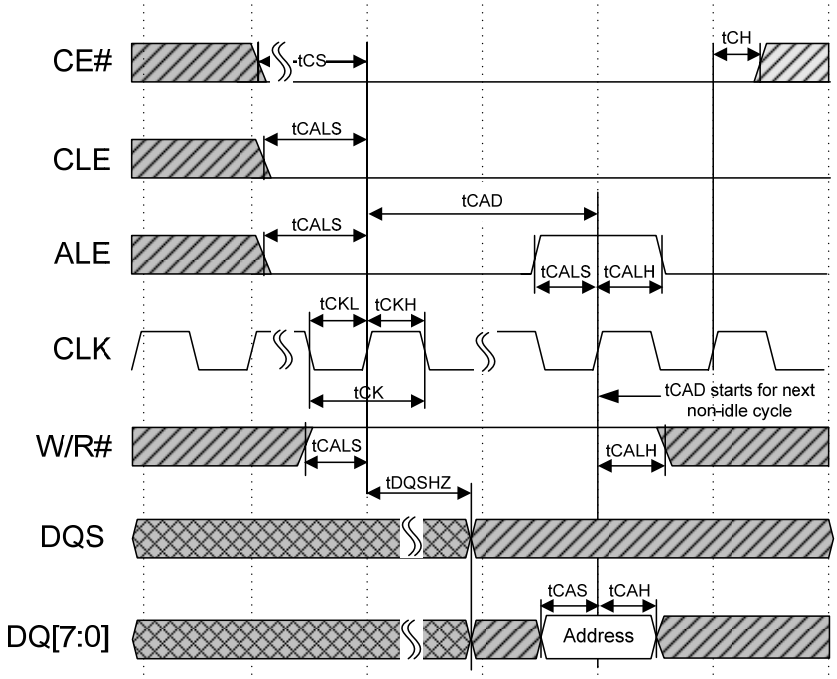
Parameter	Mode 0		Mode 1		Mode 2		Unit
tWB	—	100	—	100	—	100	ns
tWHR	80	—	60	—	60	—	ns
tWPRE	1.5	—	1.5	—	1.5	—	tCK
tWPST	1.5	—	1.5	—	1.5	—	tCK
tWRCK	20	—	20	—	20	—	ns
tWW	100	—	100	—	100	—	ns

NOTE:
tDQSHZ is not referenced to a specific voltage level, but specifies when the device output is no longer driving.
tCK(avg) is the average clock period over any consecutive 200 cycle window.
tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.

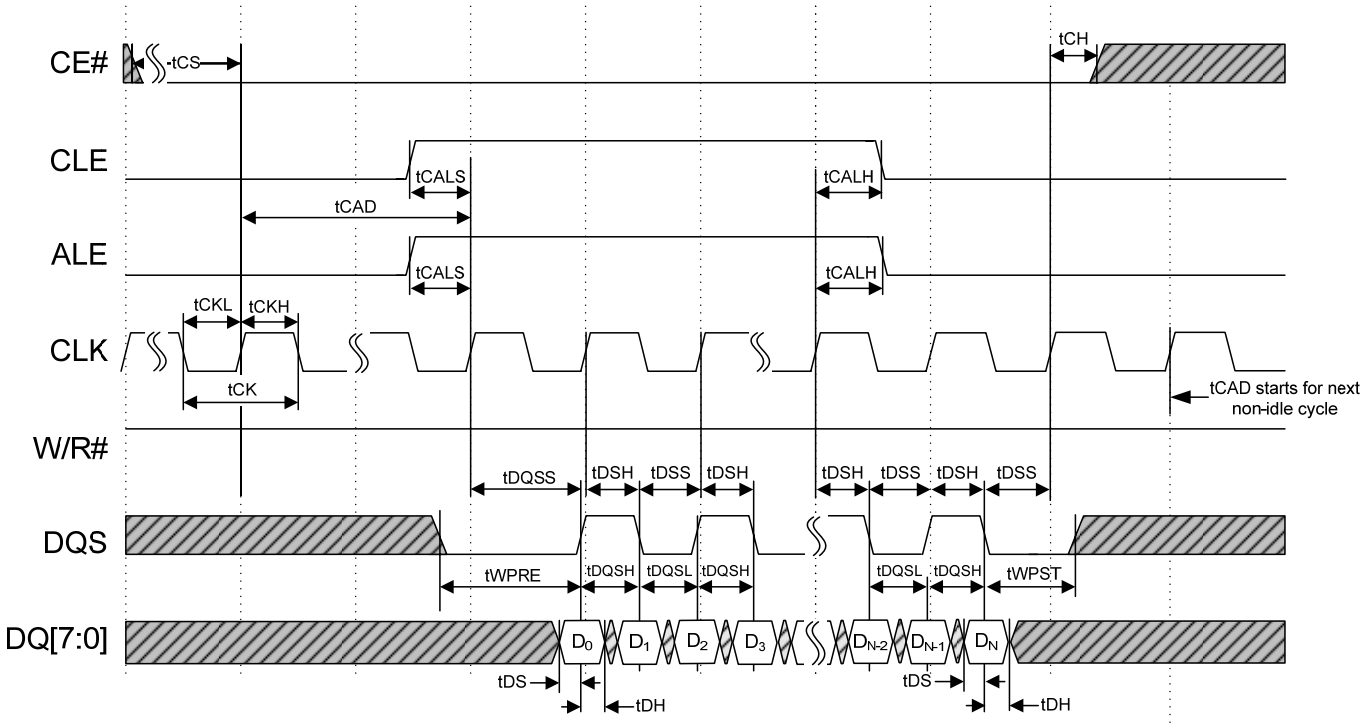
6.3.1 Command Cycle



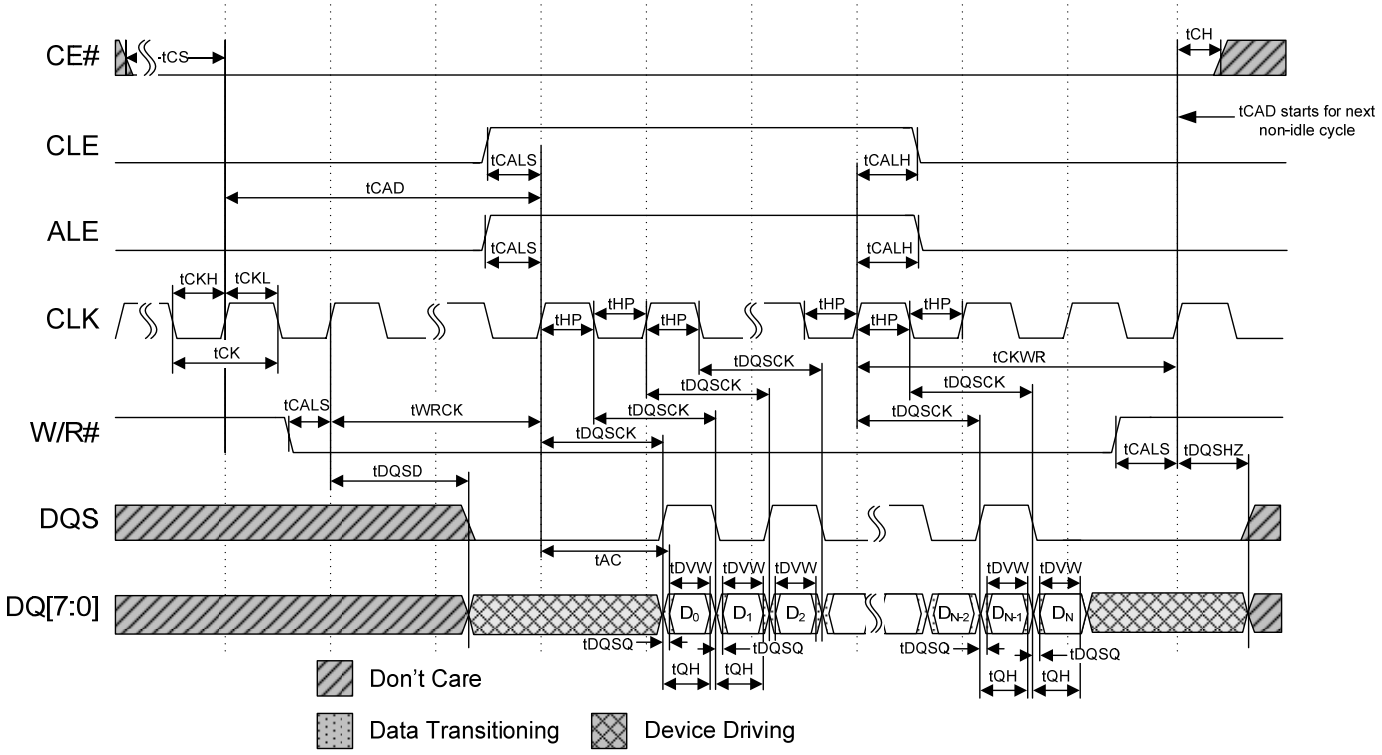
6.3.2 Address Cycle



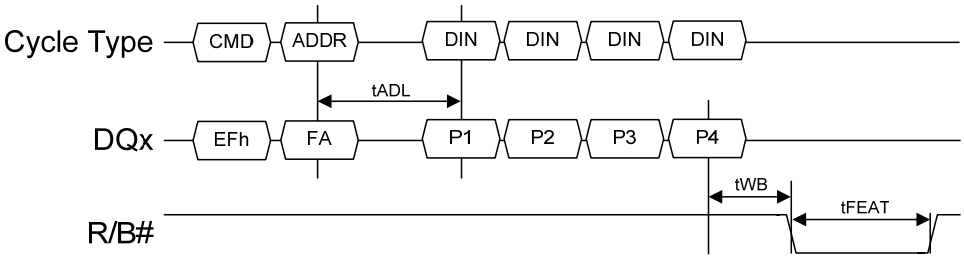
6.3.3 Data Input Cycle



6.3.4 Data Output Cycle



6.3.5 Set Feature Cycle



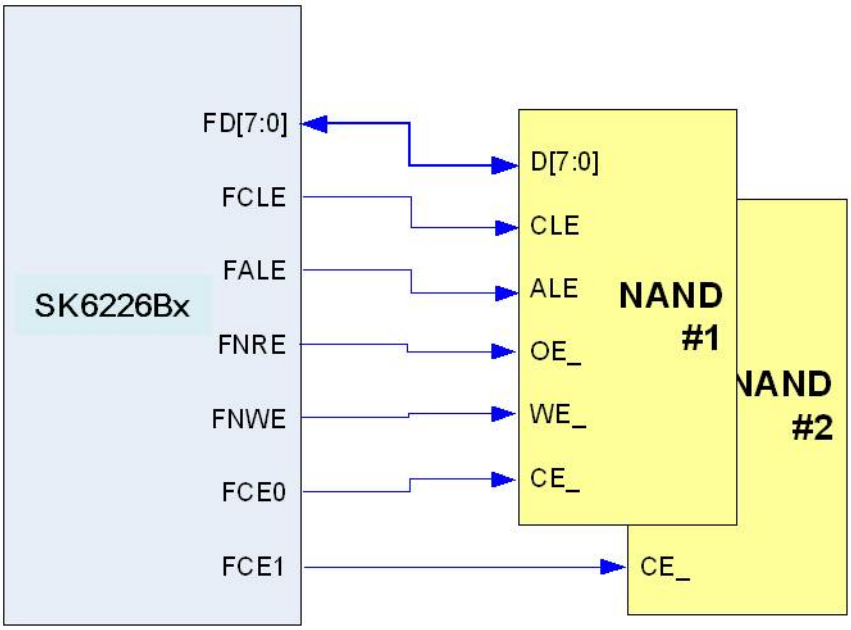
Sub Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)		Data Interface		Timing Mode Number			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							
Timing Mode Number	Set to the numerical value of the maximum timing mode in use by the host. Default power-on value is 0h.							

7. Application Examples

7.1 Controller Selection vs. NAND

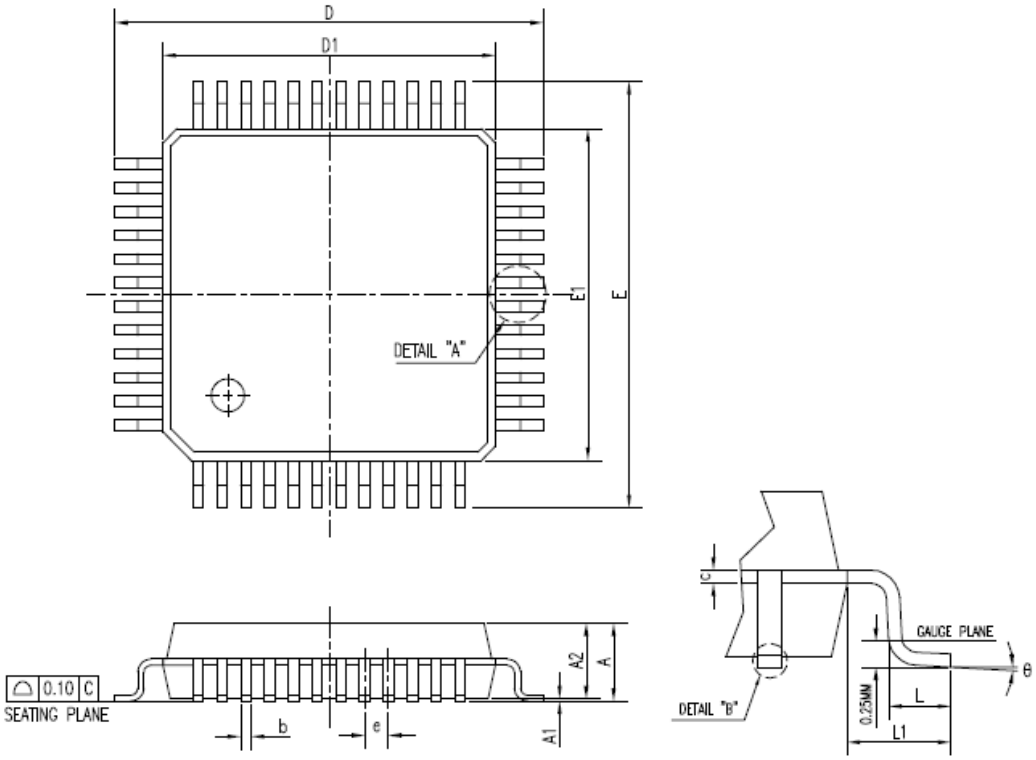
Part#	Async. NAND			DDR NAND		
	# of channel	# of CE	VCCq	# of channel	# of CE	VCCq
SK6226BAPQC	Single	8	3.3V	Single	8	1.8V 3.3V
SK6226BAPMC4	Single	4	3.3V	Single	4	1.8V 3.3V

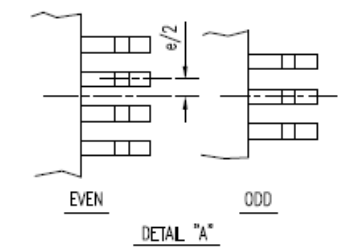
7.2 Single Channel (Byte mode)



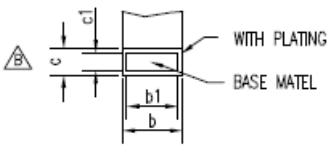
8. Package Dimension

8.1 48-pin LQFP



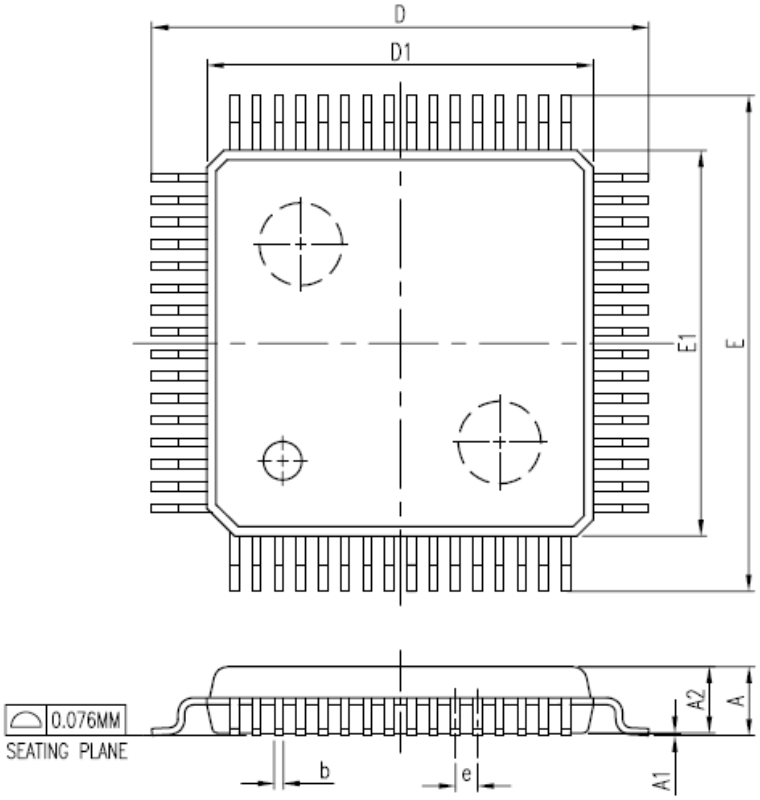


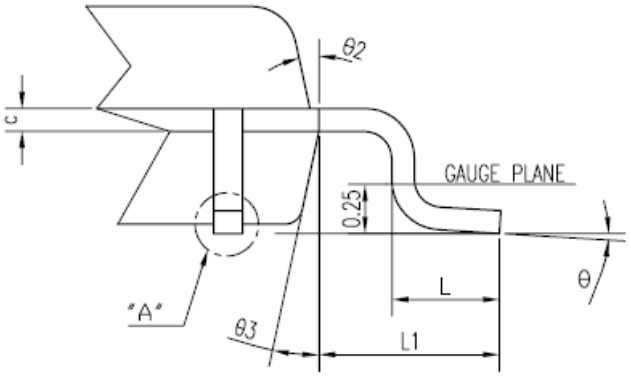
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						



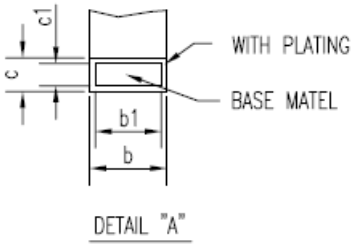
	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			
64L	0.13	0.16	0.19	0.13	0.16	0.19	0.40 BSC.			

8.2 64-pin LQFP





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.156			0.046
A1	0.05		0.15	0.002		0.006
A2	0.94	1.00	1.06	0.037	0.039	0.042
c	0.119		0.185	0.005		0.007
c1	0.127 TYP.			0.005 TYP.		
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.95	7.00	7.05	0.273	0.276	0.278
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.95	7.00	7.05	0.273	0.276	0.278
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	1.5	3.5	5.5	1.5	3.5	5.5
θ2	11	12	13	11	12	13
θ3	11	12	13	11	12	13



DETAIL "A"

	MIN.	NOM.	MAX.	NOM.	MIN.	MAX.	NOM.	MIN.	MAX.
b	0.34		0.45	0.15		0.26	0.15		0.26
b1	0.34	0.37	0.40	0.15	0.18	0.21	0.15	0.18	0.21
e	0.80BSC.			0.50BSC.			0.40BSC.		
N	32			48			64		
JEDEC	MS-026 ABA			MS-026 ABC			MS-026 ABD		