SK6238xx

Non-Crystal UFD Controller

for 1ynm MLC & TLC

Rev. 1.10

Sep. 12, 2013

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Revision History

Date	Rev	Description
Dec. 5, 2012	0.10	• Establishment.
Feb. 25, 2013	0.90	• Update some descriptions for customer reference • Remove 40QFN package due to lower customer request
Apr. 03, 2013	1.00	• Update Chap. 6 figures
Apr. 08, 2013	1.01	• Revise ECC to 65 bits/KB
Sep. 12, 2013	1.10	• Revise DC Characteristics • Update Chapter 5

Table of Contents

1. Description

The SK6238xx is a Non-Crystal USB2.0 Flash Disk controller that complies with USB version2.0 specification and USB Mass Storage Class version 1.0 specification. Besides full speed 12 Mbps complied with USB1.1 specification, SK6238xx can provide a 480 Mbps transfer rate. Designed with an enhanced power control circuit, the SK6238xx fully complies with USB power specifications for bus-powered devices, making it capable of bus-powered operation.

SK6238xx provides excellent performance in data transfer and a powerful ECC engine to ensure data integrity and reliability.

□ Reliable ECC for 1y nm MLC and TLC

SK6238xx provide 65-bit/1KB BCH ECC engine which can correct data error due to the Read/Write disturbance and enhance data detention for 1y/2x/3x nm MLC and TLC.

□ Advance Wear Leveling (AWL) to improve P/E cycle of NAND

□ Saving BOM Cost

Because SK6238 did not require an external crystal, it can save BOM cost a lot.

□ Performance & Low Power

SK6238xx provides high data transfer rate with single-channel mode. In order to meet Vista Premium logo program, SK6238xx also meet *ReadyBoost* requirement. Any UFD with SK6238xx can easily meet 5 MB/sec throughput for random 4KB reads and 3 MB/sec throughput for random 512KB writes and market the UFD with enhancement for Windows® *ReadyBoost* .

□ Support 256/384/512 pages and update to 16KB page size of NAND

With our superior designs, SK6238xx runs smoothly on all available host systems and supports MLC & TLC NAND Flash memories with 4KB, 8KB and 16KB page and either 128, 192, 256, 384 and 512 pages per block. The SK6238xx allows the direct connection of up to 8 NAND Flash chips in the configuration of single channel by 8 CE.

2. Order Information

Part #	Description	Package
SK6238ADPMC4	4 CE, 1 WE, 8-bit data width, Multi-Partition, 3.3V VCCq.	48-pin LQFP
SK6238ADWWC	8 CE, 1 WE, 8-bit data width, Multi-Partition, 3.3V VCCq.	wafer

3. Features

(1). Support 1y/2x/3x nm MLC and TLC NAND:

- □ Configurable 65-bit/1KB BCH error control coding (ECC) for MLC/TLC.
- □ Sufficient embedded buffer for 16K page NAND in single channel configuration.

(2). Advance Wear Leveling can improve P/E cycle of NAND.

(3). Saving BOM cost by removing external crystal.

(4). Outstanding R/W performance:

- □ Support high-speed DDR Toggle mode and ONFI NAND Flash
- □ *Support Windows Vista and Window-7 ReadyBoost* function

(5). USB Interface:

- □ Complied with high-speed USB 2.0 interface, backward compatible with USB 1.1.
- □ Complied with USB Mass Storage Class specification v1.0.
- □ Complied with USB bus-powered devices specification.
- □ Support HID interface for password entry in non-administrator mode.
- □ Integrated USB 2.0 Transceiver Macrocell Interface (UTMI) and Serial Interface Engine (SIE).

(6). Varieties of Supported NAND:

- □ Samsung 21nm 4-plane MLC & TLC, 27nm MLC & TLC, 32 nm TLC.
- □ IM 20nm 8KB/page MLC, 16KB/page MLC, 25 nm MLC & TLC.
- □ Hynix 16nm/20nm/26nm MLC, 32 nm TLC.
- □ Toshiba 19A/19nm/24nm 16KB/page MLC/TLC.
- □ SanDisk 19nm/24nm 16KB/page MLC/TLC.
- □ Kinds of page size: 8KB and 16KB.
- □ Kinds of page per block: 128 pages, 192 pages, 256 pages 384 pages and 512 pages.

(7). Async. NAND Interface with 3.3V VCCq:

- □ SK6238xxPMC4: single channel and 4 CE/channel.

(8). DDR NAND interface:

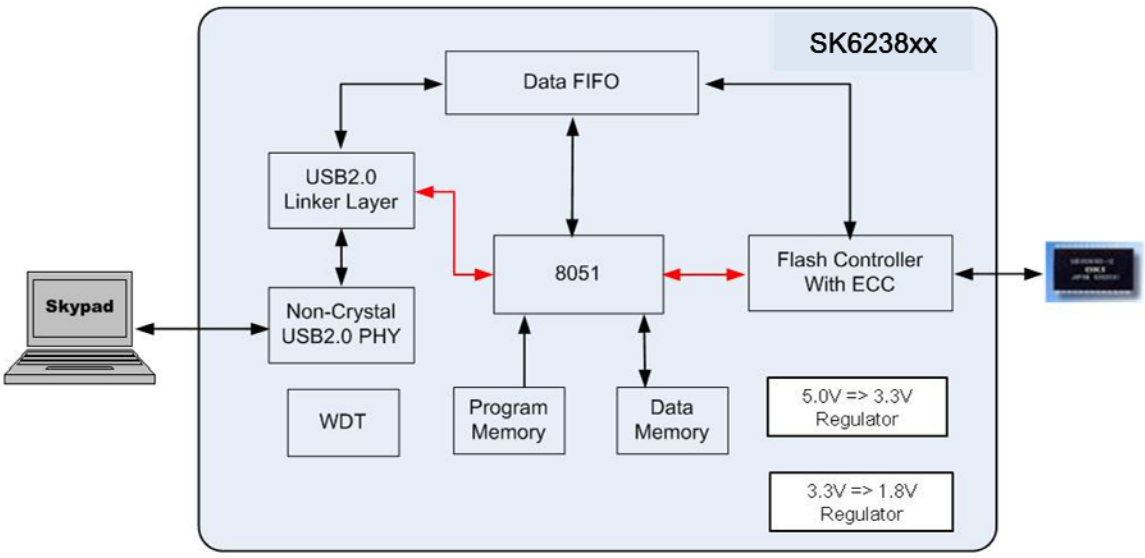
- □ 3.3V VCCq DDR NAND, either ONFI 2.x NAND or Toggle-mode NAND.
- □ SK6238xxPMC4: single channel and 4 CE/channel with 3.3V VCCq.

(9). Built-in Watch-Dog Timer (WDT)

(10). Enable Multi-Partition features:

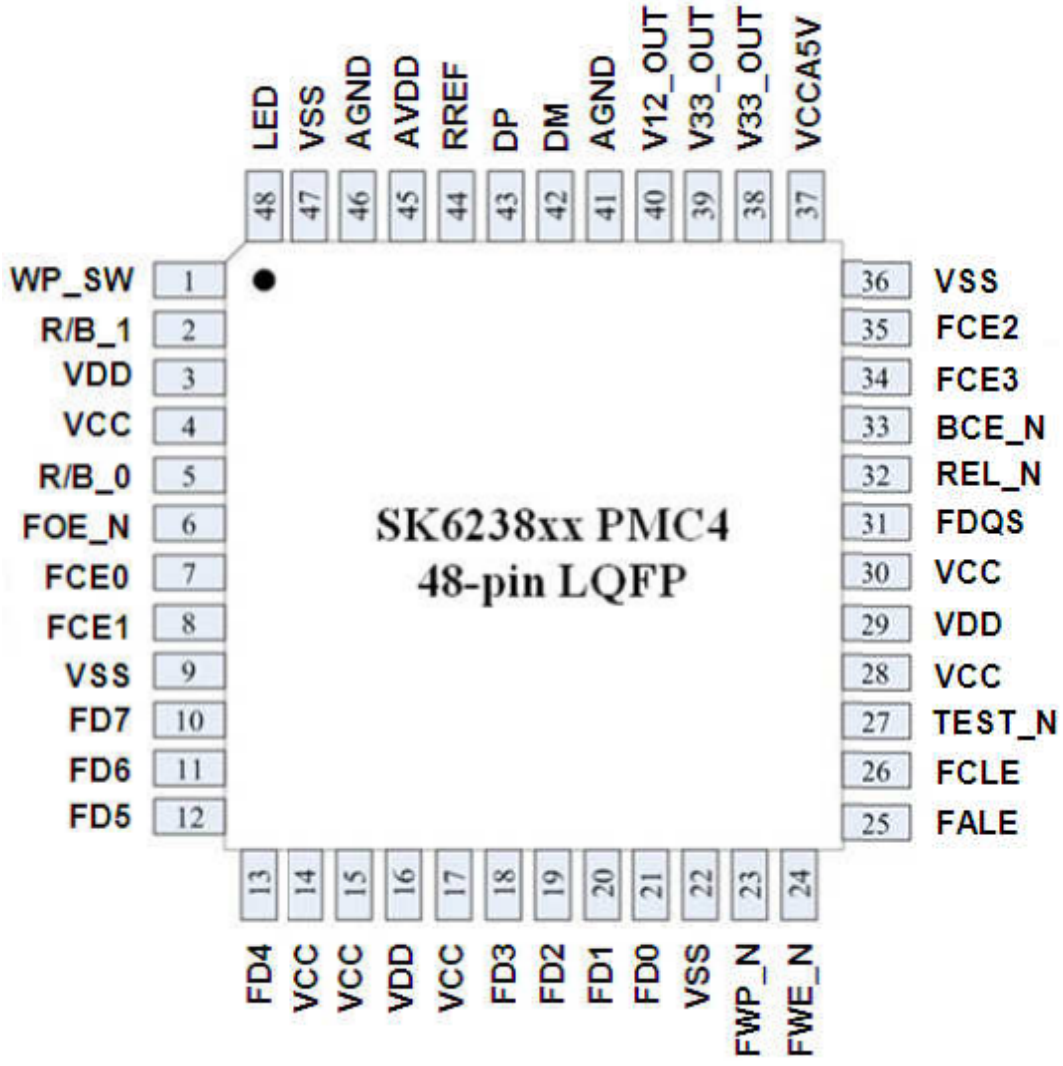
- □ One Read-only Partition, two Read-Write Partitions and one Hidden Partition.
- □ Read-only Partition is designated for AutoRun feature.
- □ UFD can have up to two LUNs because to two Read-Write Partitions.
- □ Each Read-Write Partition can be divided into Public Zone and Private Zone further.
- □ Private Zone can be protected by password.
- □ Capacity of each Partition and Zone can sizeable while factory initialization or by application program through vendor specific command.

4. Block Diagram



5. Pin Assignment

5.1 SK6238xxPMC4 48-pin LQFP Pin Assigment



5.2 Pin Definitions

Pin #	Pin Name	Type	Description
1	WP_SW	In	Write protect switch.
2	R/B_1	In	Flash ready/busy 1.
3	VDD	Power In	Core power.
4	VCC	Power In	I/O power.
5	R/B_0	In	Flash ready/busy 0.
6	FOE_N	O	Flash output enable.
7	FCE0	O	Flash chip enable 0.
8	FCE1	O	Flash chip enable 1.
9	VSS	Power	Digital ground.
10	FD7	I/O	Flash data bus bit7.
11	FD6	I/O	Flash data bus bit6.
12	FD5	I/O	Flash data bus bit5.
13	FD4	I/O	Flash data bus bit4.
14	VCC	Power In	I/O power.
15	VCC	Power In	I/O power.
16	VDD	Power In	Core power.
17	VCC	Power In	I/O power.
18	FD3	I/O	Flash data bus bit3.
19	FD2	I/O	Flash data bus bit2.
20	FD1	I/O	Flash data bus bit1.
21	FD0	I/O	Flash data bus bit0.
22	VSS	Power	Digital ground.
23	FWP_N	O	Flash write protect.
24	FEW_N	O	Flash write enable for flash data.
25	FALE	O	Flash address latch enable.
26	FCLE	O	Flash command latch enable.
27	TEST_N	I	Test pin. Low for test mode. The pin had a default pull-up resistor.
28	VCC	Power In	I/O power.
29	VDD	Power In	Core power.
30	VCC	Power In	I/O power.
31	FDQS	I/O	Flash DQS pin for DDR flash.
32	REL_N	I	No connection for normal use. The pin had a default pull-up resistor.
33	BCE_N	I	No connection for normal use. The pin had a default pull-up resistor.
34	FCE3	O	Flash chip enable 3.
35	FCE2	O	Flash chip enable 2.
36	VSS	Power	Digital ground.
37	VCCA5V	Power In	Vbus 5V power input.
38	V33_OUT	Power Out	Regulated 3.3V power output.
39	V33_OUT	Power Out	Regulated 3.3V power output.
40	V12_OUT	Power out	Regulated 1.2V power output.
41	AGND	Power	Analog ground.
42	DM	I/O	USB D-.
43	DP	I/O	USB D+.
44	RREF	In	USB PHY reference resistor.
45	AVDD	Power In	Analog 3.3V input.
46	AGND	Power	Analog ground.
47	VSS	Power	Digital ground.
48	LED	O	LED output.

6. Electrical Specifications

6.1 Absolute Maximum Ratings

Following table shows SK6238xx stress ratings only. Extended exposure to the maximum ratings might degrade device reliability. Although has protective circuitry to resist damage from electrostatic discharge (ESD), precautions should always be taken to avoid high voltage or electric field.

Symbol	Parameter	Min	Max	Unit
Tstg	Storage Temperature	- 55	+150	°C
Ta	Ambient Operating Temperature, Commercial	-45	+85	°C
V_{AVDD}	Analog 3.3V Input Voltage	3.0	3.6	V
V_{VCC}, V_{VDD}	Core and I/O supply Voltage	3.0	3.6	V
V_{VCCA5V}	USB +5.0V Input Voltage	-0.3	5.25	V

Note, this table contains preliminary data and may be updated in a later version.

6.2 DC Characteristics

Symbol	Description	Min.	Typ.	Max.	Unit
V_{AVDD}	Analog 3.3V Input Voltage	3.0	3.3	3.6	V
V_{VCC}, V_{VDD}	Digital 3.3V Input Voltage	3.0	3.3	3.6	V
V_{VCCA5V}	USB +5.0V Input Voltage	4.40	5.0	5.25	V
V_{V33_out}	Regulated 3.3V Output Voltage (at 350mA current loading)	3.0	3.3	3.6	V
V_{V12_out}	Regulated 1.2V Output Voltage	1.08	1.2	1.32	V
V_{IH}	Input Voltage High	0.625*VCC			V
V_{IL}	Input Voltage Low			0.25*VCC	V
V_{OH}	Output Voltage High	0.8*VCC			V
V_{OL}	Output Voltage Low			0.2*VCC	V
C_{in}	Input Pin Capacitance			10	pF

Note, this table contains preliminary data and may be updated in a later version.

6.3 AC Characteristics, ONFI 2.0 Synchronous Interface

The specification of timing parameters of ONFI 2.0 Source Synchronous modes are listed below. The real AC timing is subjective to change due to FW revision.

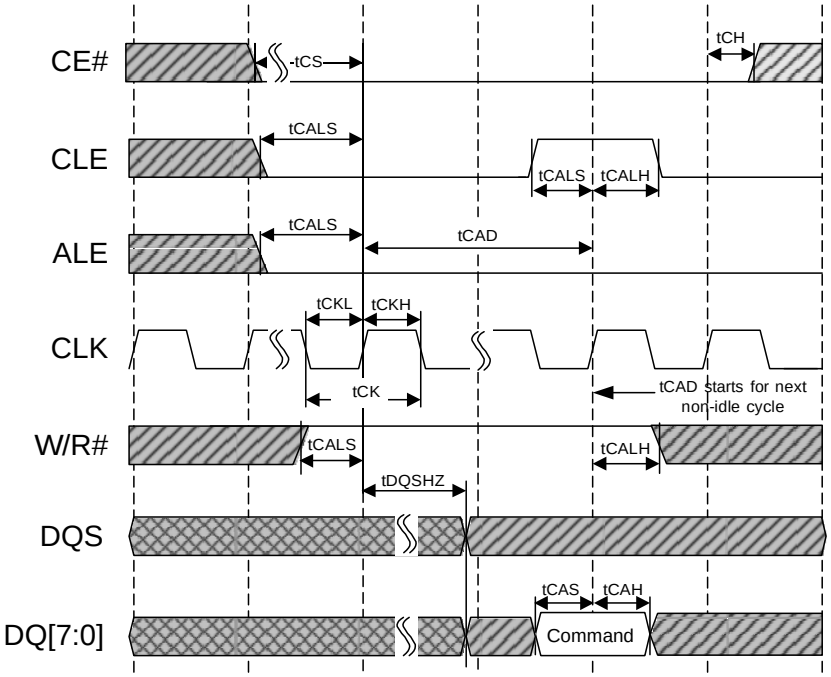
Parameter	Mode 0		Mode 1		Mode 2		Unit
	50		30		20		ns
	~20		~33		~50		MHz
	Min	**Max**	**Min**	**Max**	**Min**	**Max**	
tAC	—	20	—	20	—	20	ns
tADL	100	—	100	—	70	—	ns
tCADf	25	—	25	—	25	—	ns
tCADs	45	—	45	—	45	—	ns
tCAH	10	—	5	—	4	—	ns
tCALH	10	—	5	—	4	—	ns
tCALS	10	—	5	—	4	—	ns
tCAS	10	—	5	—	4	—	ns
tCH	10	—	5	—	4	—	ns
tCK(avg) or tCK	50	—	30	—	20	—	ns
tCK(abs)	Minimum: tCK(avg) + tJIT(per) min Maximum: tCK(avg) + tJIT(per) max						ns
tCKH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK
tCKL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK
tCS	35	—	25	—	15	—	ns
tDH	5	—	2.5	—	1.7	—	ns
tDQSCK	—	20	—	20	—	20	ns
tDQSD	—	20	—	20	—	20	ns
tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tDQSHZ	—	20	—	20	—	20	ns
tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK
tDQSQ	—	5	—	2.5	—	1.7	ns
tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK
tDS	5	—	3	—	2	—	ns
tDSH	0.2	—	0.2	—	0.2	—	tCK
tDSS	0.2	—	0.2	—	0.2	—	tCK
tDVW	tDVW = tQH – tDQSQ						ns
tFEAT	—	1	—	1	—	1	µs
tHP	tHP = min(tCKL, tCKH)						ns
tITC	—	1	—	1	—	1	µs
tJIT(per)	0.7	0.7	0.7	0.7	0.7	0.7	ns
tQH	tQH = tHP – tQHS						ns
tQHS	—	6	—	3	—	2	ns
tRHW	100	—	100	—	100	—	ns
tRR	20	—	20	—	20	—	ns
tRST	—	5/10/500	—	5/10/500	—	5/10/500	µs

Parameter	Mode 0		Mode 1		Mode 2		Unit
tWB	—	100	—	100	—	100	ns
tWHR	80	—	60	—	60	—	ns
tWPRE	1.5	—	1.5	—	1.5	—	tCK
tWPST	1.5	—	1.5	—	1.5	—	tCK
tWRCK	20	—	20	—	20	—	ns
tWW	100	—	100	—	100	—	ns

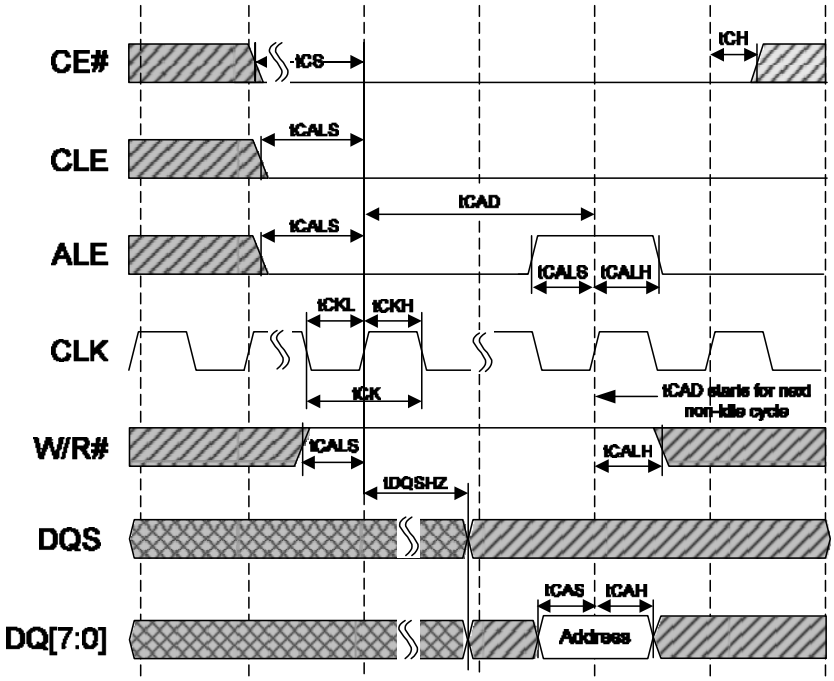
NOTE:

1. tDQSHZ is not referenced to a specific voltage level, but specifies when the device output is no longer driving.
2. tCK(avg) is the average clock period over any consecutive 200 cycle window.
3. tCKH(abs) and tCKL(abs) include static offset and duty cycle jitter.
4. This table contains preliminary data and may be updated in a later version

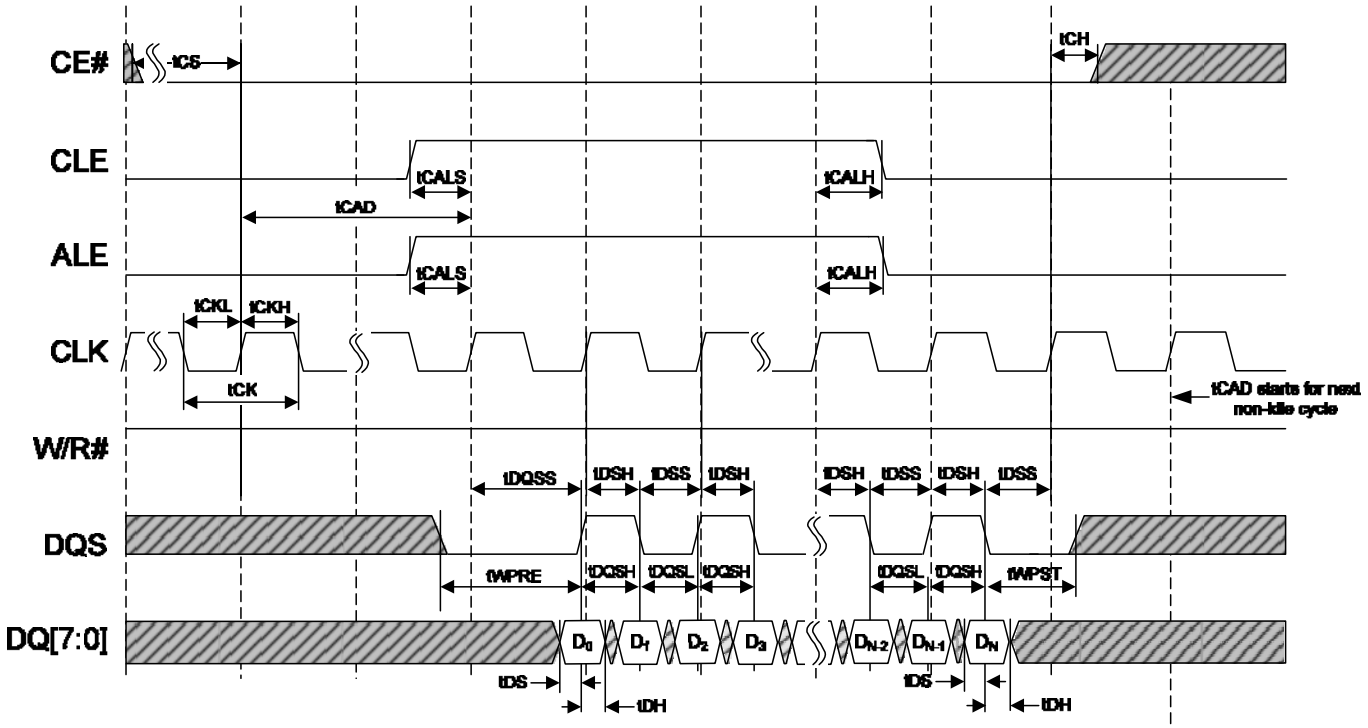
6.3.1 Command Cycle



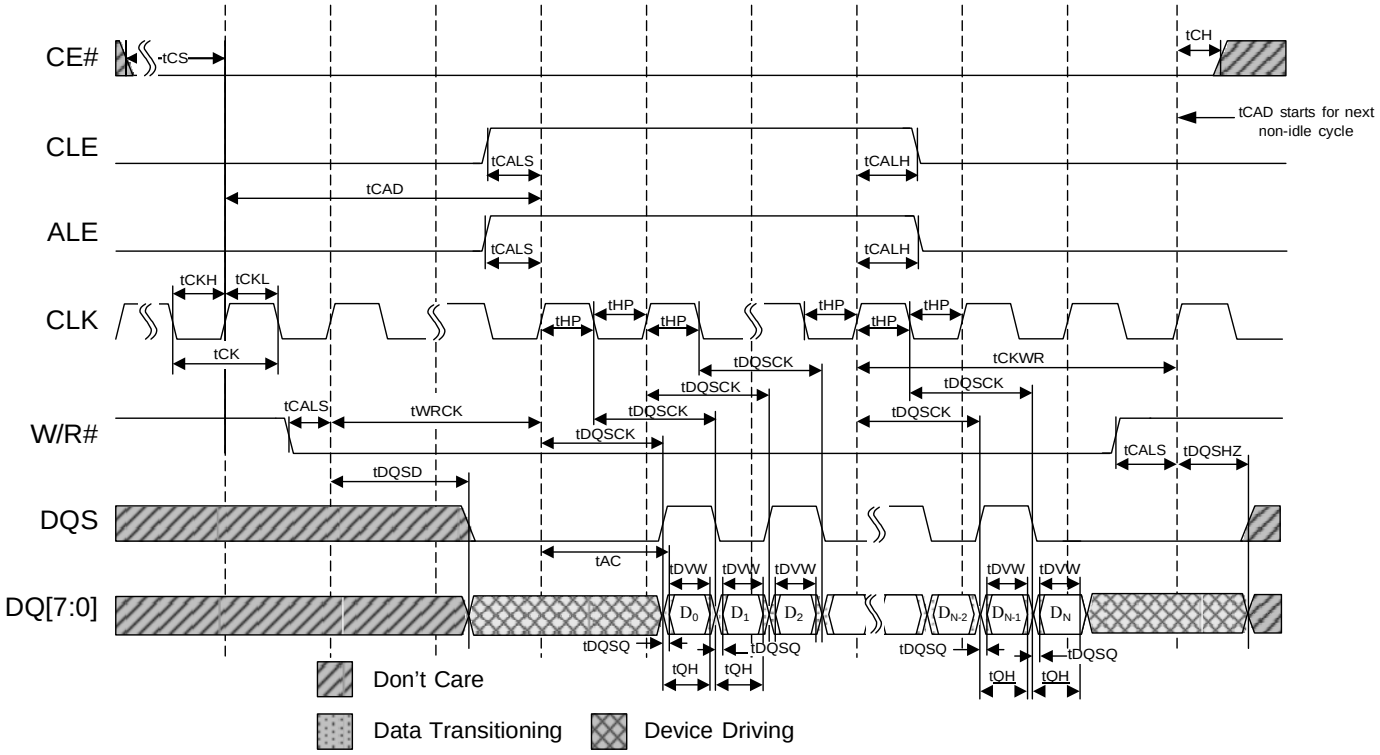
6.3.2 Address Cycle



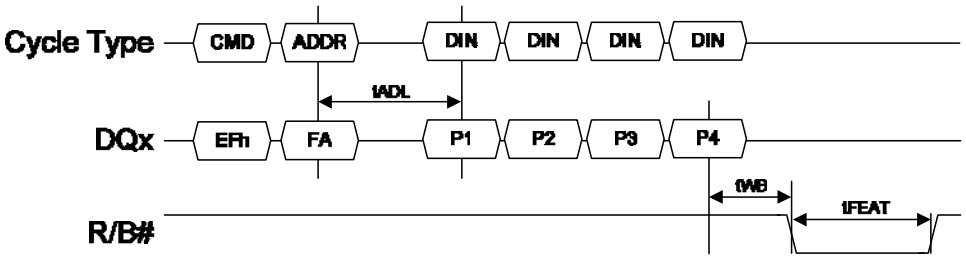
6.3.3 Data Input Cycle



6.3.4 Data Output Cycle



6.3.5 Set Feature Cycle



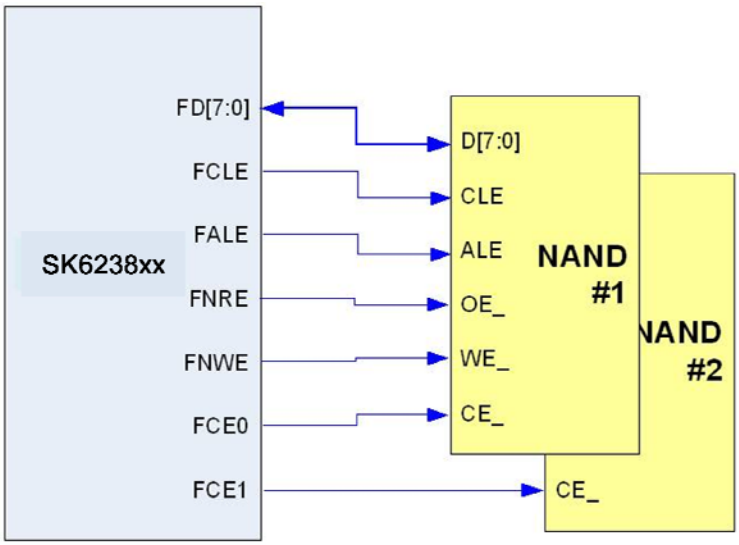
Feature Parameter	7	6	5	4	3	2	1	0
P1	Reserved (0)		Data Interface		Timing Mode Number			
P2	Reserved (0)							
P3	Reserved (0)							
P4	Reserved (0)							
Timing Mode Number	Set to the numerical value of the maximum timing mode in use by the host. Default power-on value is 0h.							

7. Application Examples

7.1 Controller Selection vs. NAND

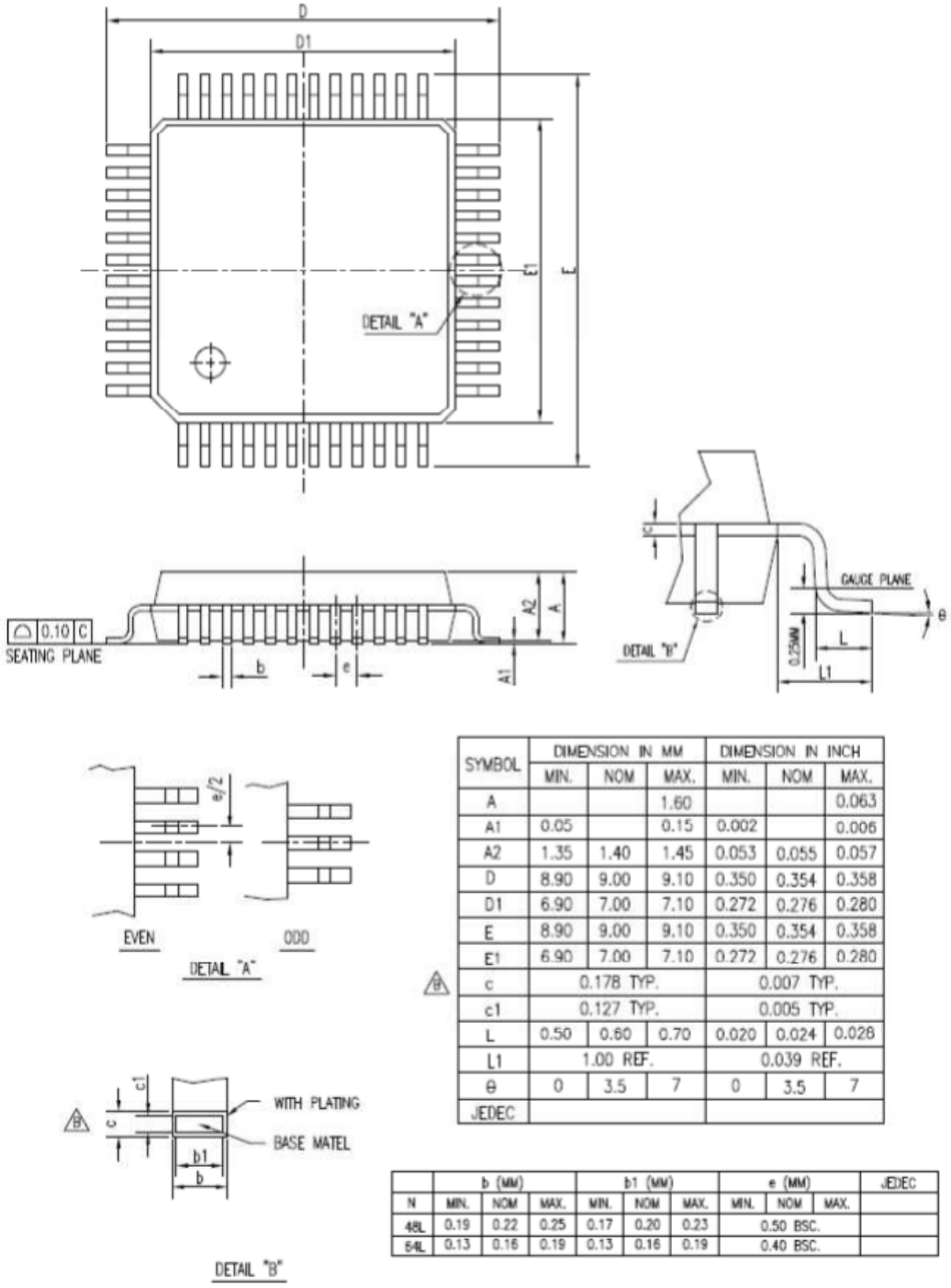
Part#	Async. NAND			D R NAND		
	# of channel	# of CE	VCCq	# of channel	# of CE	VCCq
SK6238ADPMC4	Single	4	3.3V	Single	4	3.3V
SK6238xxNUC	Single	4	3.3V	Single	4	3.3V

7.2 Single Channel (Byte mode)



8. Package Dimension

8.1 48-pin LQFP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.19	0.22	0.25	0.17	0.20	0.23	0.50 BSC.			
64L	0.13	0.16	0.19	0.13	0.16	0.19	0.40 BSC.			