SK70725A/SK70721

Enhanced Multi-Rate DSL Data Pump Chip Set

Datasheet

The Enhanced Multi-Rate DSL Data Pump (EMDP) is a variable-rate transceiver that provides symmetric full-duplex communication on one twisted wire pair using a 2B1Q line code with echo-cancellation. The EMDP operates in either framed or Transparent modes and supports channelized, cell and packet applications. Symmetrical line rates may be at any speed between 272 and 1,168 kbps. Performance is specified at 272, 400, 528 784 and 1,168 kbps for payloads of 4, 6, 8, 12 or 18 channels at 64 kbps and 16 kbps of overhead. The EMDP chip set consists of two devices:

- SK70725A - Enhanced Digital Signal Processor (EDSP)
- SK70721- Integrated Analog Front-End (IAFE)

The IAFE is a fully integrated CMOS analog front-end which includes D/A converter, filters, and transmit line drivers. Receiver functions include analog echo canceller, AGC, A/D converter modulator and VCXO functions. The EDSP incorporates all digital signal processing required for A/D conversion, echo-cancellation, data scrambling and adaptive equalization as well as transceiver activation state machine control

Applications

- High speed symmetrical Internet access
- Extended range fractional T1/E1 transport
- Digital pairgain systems from 4 to 18 channels
- Wireless base station access
- WAN access for 10BaseT and ATM LANs
- Video Conferencing Systems

As of January 15, 2001, this document replaces the Level One document *SK70725A/SK70721 — Enhanced Multi-Rate DSL Data Pump Chip Set*.

Order Number: 249210-001
January 2001

Datasheet

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Revision History

Revision	Date	Description

1.0 Features

- Fully integrated, 2-chip transceiver. Compliant with the following standards:
  - — ITU G.991.1
  - — ANSI Committee T1E1.4-TR28 (T1E1.4/96-006)
  - — ETSI ETR-152
- Integrated line drivers, filters and hybrid circuits reduce the number of external components required
- Multiple framing modes: Transparent, T1 standard, E1 standard
- Independent transmit and receive clocks for minimum delay
- Tolerance for extended signal interruptions
- Single +5V supply
- Supports processor directed rate selection driven by receive signal level and noise margin
- Continuously adaptive echo canceller and equalizers maintain excellent transmission performance with changing noise and line characteristics
- Typical noise-free transmission range:
- 272 kbps
  25.3 kft (7.7 km) on 24 AWG (0.5 mm) wire
  17.1 kft (5.2 km) on 26 AWG (0.4 mm) wire
- 784 kbps
  19.8 kft (6.0 km) on 24 AWG (0.5 mm) wire
  13.7 kft (4.2 km) on 26 AWG (0.4 mm) wire
- 1,168 kbps
  17.1 kft (5.2 km) on 24 AWG (0.5 mm) wire
  12.3 kft (3.7 km) on 26 AWG (0.4 mm) wire

Figure 1. SK70725A/SK20221 Block Diagram

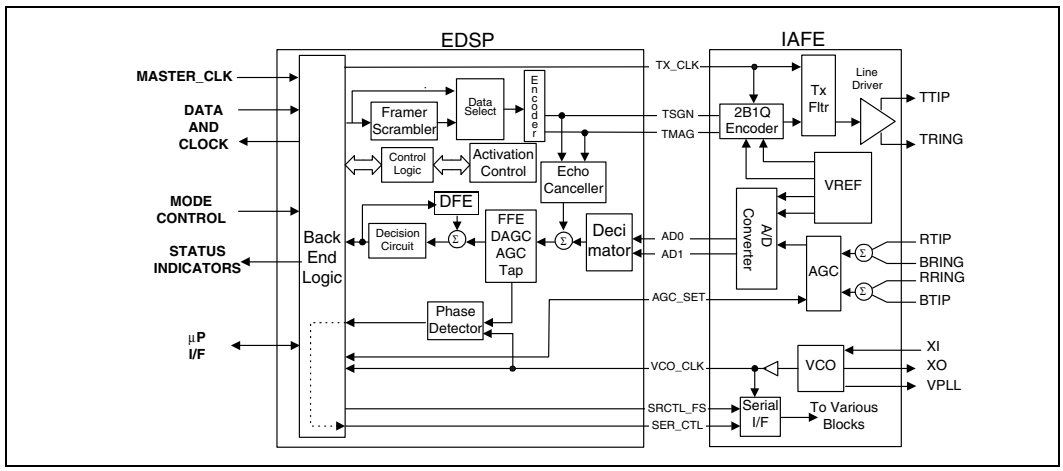
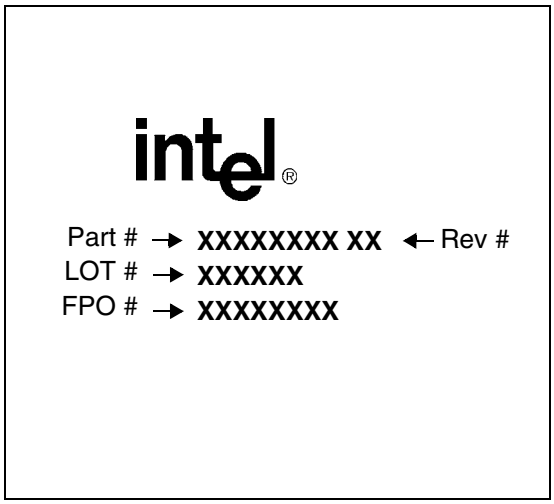


Figure 2. Package Markings



Package Topside Markings

Marking	Definition
Part #	Unique identifier for this product family.
Rev #	Identifies the particular silicon “stepping” — refer to the specification update for additional stepping information.
Lot #	Identifies the batch.
FPO #	Identifies the Finish Process Order.

2.0 Pin Assignments and Signal Descriptions

The IAFE is packaged in a 28 pin PLCC. Figure 3 shows the IAFE pin locations. Table 1 provides signal descriptions.

The EDSP device is packaged in a 44 pin PLCC. Figure 4 shows EDSP pin designations. Table 2 provides signal descriptions.

Figure 3. IAFE Pin Locations

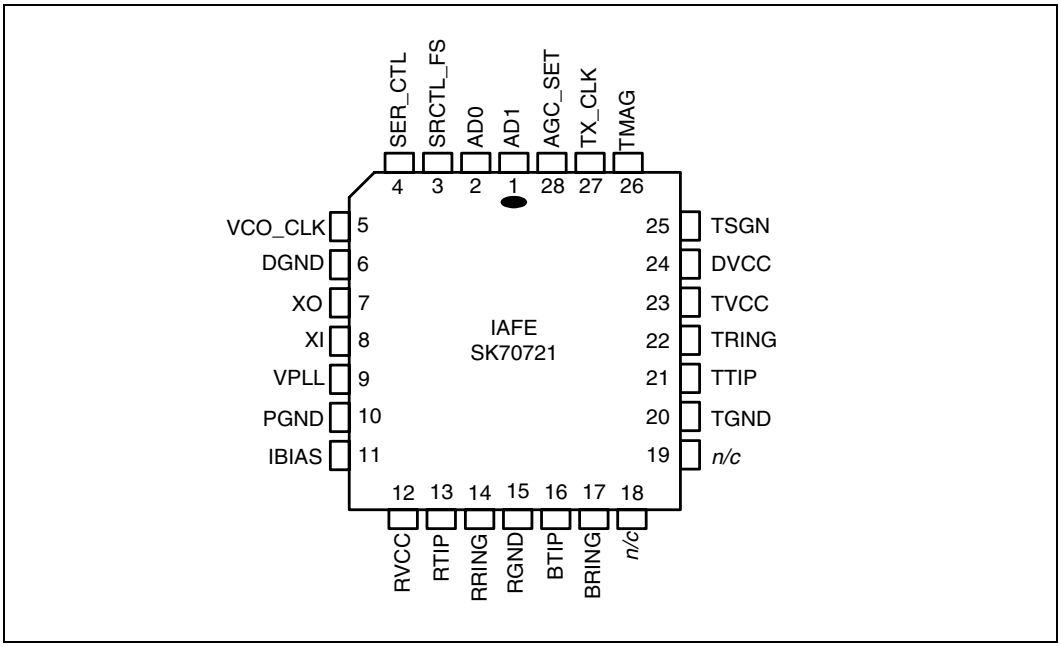


Table 1. IAFE Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[1]	Description
Power	12	RVCC	S	**Receive Power Supply.** +5 V
	23	TVCC	S	**Transmit Power Supply.** +5 V
	24	DVCC	S	**Digital Power Supply.** +5 V
	6	DGND	S	**DVCC Ground.**
	10	PGND	S	**PLL Ground.**
	15	RGND	S	**RVCC Ground.**
	20	TGND	S	**TVCC Ground.**

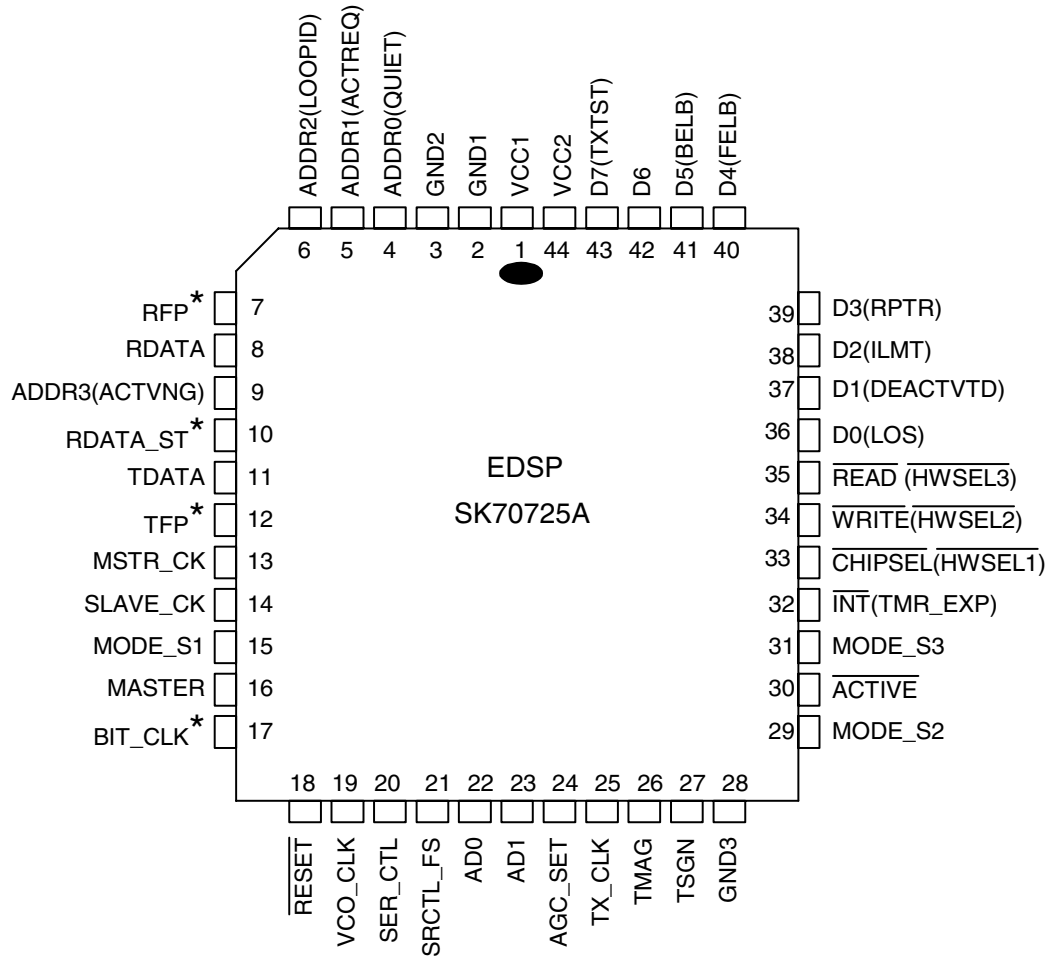
1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 1. IAFE Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[1]	Description
MDSL I/F	13	RTIP	AI	**Receive Tip and Ring.** Receiver differential inputs.
	14	RRING	AI	
	16	BTIP	AI	**Balance Tip and Ring.** Echo canceller balance network differential inputs.
	17	BRING	AI	
	21	TTIP	AO	**Transmit Tip and Ring.** Balanced line driver outputs.
	22	TRING	AO	
PLL	7	XO	AO	**Crystal Oscillator.** Connect a pullable crystal whose frequency is 32 times the bit rate between these two pins. Refer to the Applications Section for crystal specifications.
	8	XI	AI	
	9	VPLL	AO	**PLL Control Voltage.** Control signal for the VCXO.
EDSP Interface	1	AD1	DO	**A/D Converter Data Line 1.**
	2	AD0	DO	**A/D Converter Data Line 0.**
	3	SRCTL_FS	DI	**Serial Control Frame Strobe**. Equal to Receive Baud Rate.
	4	SER_CTL	DI	Serial Control.
	5	VCO_CLK	DO	**IAFE Reference Clock Output.** Provides the receive timing reference for the EDSP.
	25	TSGN	DI	**Transmit Quat Sign Bit.**
	26	TMAG	DI	**Transmit Quat Magnitude Bit.**
	27	TX_CLK	DI	**Transmit Symbol Clock. Four times the Bit-rate.**
	28	AGC_SET	DO	AGC Adjust.
Analog Input	11	IBIAS	AI	**Input Bias.** Sets internal bias currents.

1. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Figure 4. EDSP Pin Assignments



NOTES:
1. Pin Names in Hardware Control mode are shown in parentheses.
2. Pin Names indicated with an * apply to data modes 6 and 7. See Table 2 and Table 5 for signal names and functions in other modes.

Table 2. EDSP Pin Assignments/Signal Descriptions

Group	Pin #	Symbol	I/O[5]	Description
Power	1	VCC1	S	**Logic Power Supply.** +5V
	44	VCC2	S	**I/O Power Supply.** +5 V.
	2	GND1	S	**Ground 1.**
	3	GND2	S	**Ground 2.**
	28	GND3	S	**Ground 3.**
Misc	18	RESET	DI[1]	**Reset.** Pulse Low to initialize internal circuits.
Mode Select	16	MASTER	DI[3]	**Master.** When High, the Data Pump operates in Master mode and is the link timing source. When Low, the Data Pump operates in Slave mode. The EDSP must be reset after the state of MASTER is changed.
	15	MODE_S1	DI[3]	**Mode Selects.** Determine the framing and data interface mode of the EMDP. See Table 5 for details.
	29	MODE_S2	DI[3]	
	31	MODE_S3	DI[3]	
Status Indication	30	$\overline{\text{ACTIVE}}$	DO	**Link Active Indicator.** In operating modes 0, 1, 2, 4, and 5, $\overline{\text{ACTIVE}}$ is asserted whenever the EMDP completes the Activation process. In operating modes 6 and 7, $\overline{\text{ACTIVE}}$ is asserted upon detection of two consecutive frame synchronization words. $\overline{\text{ACTIVE}}$ goes High if the signal is lost, or if the frame synchronization word is not detected in six consecutive frames.
Clock and Control	14	SLAVE_CLK	DI[1]	**Slave Mode Reference Clock.** Master clock for Slave Mode, at 16 times the line rate. This clock is used as a reference clock until the clock is recovered from the received signal. Tie High or Low in Master Mode.
	13	MSTR_CLK	DI DO	**MDSL Reference Clock.** In Master Mode, this input clock, at 16 times the line rate, generates transmit and receive timing. In Slave Mode, this output is designed to drive the MSTR_CLK input of another Data Pump configured as a repeater.
IAFE Interface	19	VCO_CLK	DI	**Receive Clock Input.** Clock provided by the IAFE VCXO. VCO_CLK is 32 times the line rate.
	20	SER_CTL	DO	**Serial Control Output.**
	21	SRCTL_FS	DO	**Serial Control Frame Strobe.** Equal to Receive Baud Rate and derived from VCO_CLK.
	22	AD0	DI[4]	**Analog to Digital Converter Data Line 0.**
	23	AD1	DI[4]	**Analog to Digital Converter Data Line 1.**
	24	AGC_SET	DI[4]	**AGC Adjust Input.**
	25	TX_CLK	DO	**Transmit Symbol Clock.** Four times the line rate.
	26	TMAG	DO	**Transmit Quat Magnitude Bit.**
	27	TSGN	DO	**Transmit Quat Sign Bit.**

1. Input is a Schmidt triggered circuit and includes an internal pull-up device.
2. Input is a Schmidt triggered circuit and includes an internal pull-down device.
3. Input includes an internal pull-up device.
4. Input includes an internal pull-down device.
5. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2. EDSP Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[5]	Description
Data Interface, Transparent Modes (0, 1, and 2)	7	UNUSED	DO	**This pin is unused in Transparent Mode.**
	8	RDATA	DO	**Receive Data.** When $\overline{\text{ACTIVE}}$ is Low, the received data is output on RDATA. RDATA is High during the inactive and deactivated states. RDATA is aligned with the rising edge of the BIT_CLK.
	10	UNUSED	DO	This pin is unused in Transparent Mode.
	11	TDATA	DI[1]	**Transmit Data.** When $\overline{\text{ACTIVE}}$ is Low, the Data Pump samples TDATA on every falling edge of BIT_CLK. In Transparent mode the user may either send the data and allow the Data Pump to scramble the data or disable the scrambler and independently control the sign and magnitude bits.
	12	QUAT_CLK	DO	**Quat Clock.** One QUAT_CLK cycle occurs for each baud transmitted. The same clock is used for both transmit and receive data.
	17	BIT_CLK	DO	**Bit Clock.** One BIT_CLK cycle occurs for each data bit. The same clock is used for both transmit and receive data.
Data Interface, Independent Modes (4 and 5)	7	RQUAT_CLK	DO	**Receive Quat Clock.** Baud rate clock aligned with received data.
	8	RDATA	DO	**Receive Data.** When $\overline{\text{ACTIVE}}$ is Low, the received data is output on RDATA. RDATA is High during the inactive and deactivated states. RDATA is aligned with the rising edge of the BIT_CLK.
	10	RBIT_CLK	DO	**Receive Data Clock.** One RBIT_CLK cycle occurs for each received data bit.
	11	TDATA	DI[1]	**Transmit Data.** When $\overline{\text{ACTIVE}}$ is Low, the Data Pump samples TDATA on every falling edge of TBIT_CLK. In Independent mode the user may either send the data and allow the Data Pump to scramble the data or disable the scrambler and independently control the sign and magnitude bits.
	12	TQUAT_CLK	DO	**Transmit Quat Clock.** Baud rate clock for alignment of transmit data.
	17	TBIT_CLK	DO	**Transmit Data Clock.** One TBIT_CLK cycle occurs for each data bit transmitted.
Data Interface, Framed Modes (6 and 7)	7	RFP	DO	**Receive Frame Pulse.** Low for one BIT_CLK cycle during the last bit of the current MDSL receive frame. RFP is valid only when $\overline{\text{ACTIVE}}$ is Low.
	8	RDATA	DO	**Receive Data Output.** When $\overline{\text{ACTIVE}}$ is Low, the receive data including frame sync and stuff bits are output on RDATA. RDATA is High during the inactive and deactivated states. RDATA is aligned with the falling edge of BIT-CLK.
	10	RDATA_ST	DO	**Receive Data Strobe.** RDATA_ST goes High during receipt of stuffing and framing bits.
	11	TDATA	DI[1]	**Transmit Data.** When $\overline{\text{ACTIVE}}$ is Low, the Data Pump samples TDATA at the rising edge of BIT_CLK, except during frame sync and stuff bits.
	12	TFP	DI[1]	**Transmit Frame Pulse.** TFP must be Low during the last BIT_CLK cycle of each transmitted MDSL frame. *If TFP is pulled Low and is Low again three BIT_CLK cycles later, RDATA, RFP, RDATA_ST, BIT_CLK, and $\overline{\text{ACTIVE}}$ will tristate until the TFP is set High again.*
	17	BIT_CLK	DO	**Bit Rate Clock.** This clock is used to transfer data into and out of the EMDP.

1. Input is a Schmidt triggered circuit and includes an internal pull-up device.
2. Input is a Schmidt triggered circuit and includes an internal pull-down device.
3. Input includes an internal pull-up device.
4. Input includes an internal pull-down device.
5. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2. EDSP Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[5]	Description
Hardware Interface (Hardware Control Mode only)	4	QUIET	DI[2]	**Quiet Mode Enable.** Set High to force the EDSP into the Deactivated state. Set Low to enable activation requests (see ACTREQ).
	5	ACTREQ	DI[2]	**Activation Request (Master mode only - not used in Slave mode).** When QUIET is Low, a rising edge on this pin initiates activation. The signal is ignored after activation. In Slave mode this pin may be held Low or left open.
	6	LOOPID	DI[2]/O	**Loop Number Control (Master mode) or Loop Number Indicator (Slave mode).** This indicator is transmitted from the Master to the Slave and can be used for loop identification in systems that multiplex data onto two MDSL lines. In Slave mode LOOPID is valid only when in the ACTIVE state. LOOPID=0 identifies MDSL loop 1 in accordance with the ETSI standard. LOOPID must be set before the Master is activated. LOOPID may be originated in the EMDP only when operating in modes 6 or 7.
	9	ACTVNG	DO	**Activating State Indication.** ACTVNG is High when the EMDP is in the Activating state.

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4. Input includes an internal pull-down device.
5. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2. EDSP Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[5]	Description
Hardware Interface (Hardware Control Mode only)	32	TMR_EXP	DO	**Timer Expiration Indicator.** TMR_EXP goes High when the Master Activation Timer (MAT) expires.
	33	HWSEL1	DI[2]	**Hardware Selects.** Each of these three pins must be Low to enable Hardware Control Mode. When any are High, the EDSP reverts immediately to Software Control Mode.
	34	HWSEL2	DI[2]	
	35	HWSEL3	DI[2]	
	36	LOS	DO	**Loss of Signal Indicator.** Goes High when the EMDP is in the Inactive state.
	37	DEACTVTD	DO	**Deactivation Indicator.** Goes High when the Data Pump is in the Deactivated state.
	38	ILMT	DI[1]	**Insertion Loss Measurement Test.** Set High to transmit a scrambled all 1's signal. In operating mode 6 and 7 the signals transmitted are framed with valid sync word, whereas in the rest of the operating modes signals transmitted are unframed without any sync word. If the loop is connected to a Slave Data Pump then it may begin activating. Must be asserted only from the Inactive state of the Data Pump.
	39	RPTR	DI[1]	**Repeater Mode Enable. (operating mode 6 & 7 only).** When in Master mode, setting RPTR High configures the Data Pump to derive timing from the MSTR_CLK output of an adjacent device for transparent repeater applications. The BIT_CLK output phase is aligned to the TFP input pulse. RPTR is ignored in Slave mode.
	40	FELB	DI[1]	**Front-End Loopback (Master only).** In the Inactive state, set High to cause the IAFE to loopback. The RTIP/RRING inputs are disconnected and only the signals on the BTIP/BRING inputs are processed.
	41	BELB	DI[1]	**Back-End Loopback.** Set BELB High in Active1 or Active2 state to force an internal loopback with RDATA connected to TDATA and RFP connected to TFP.
	43	TXTST	DI[1]	**Transmit Test.** Set High to enable isolated transmit pulse generation. TDATA controls the sign and TFP controls the magnitude of the transmitted pulses according to the 2B1Q encoding rules described in Table 3. The TXTST function is available only in framed modes 6 and 7. In framed mode 6 the pulses are transmitted every 7006/7010 BIT_CLK cycles, corresponding to the ETSI framing sequence. In framed mode 7 the pulses are transmitted every 4702/4706 BIT_CLK cycles. TXTST is available only when the Data Pumps are Inactive.

1. Input is a Schmidt triggered circuit and includes an internal pull-up device.
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3. Input includes an internal pull-up device.
4. Input includes an internal pull-down device.
5. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

Table 2. EDSP Pin Assignments/Signal Descriptions (Continued)

Group	Pin #	Symbol	I/O[5]	Description
Processor Interface (Software Control Mode)	4 5 6 9	ADDR0 ADDR1 ADDR2 ADDR3	DI[2]	**Address Bits.** Four-bit address, selects read or write register.
	32	INT	DO	**Interrupt Output.** Open drain output. Requires an external 10 kΩ pull up resistor. Goes Low on interrupt.
	33	CHIPSEL	DI[2]	**Chip Select.** Pull Low to read or write to registers.
	34	WRITE	DI[2]	**Write.** Pull Low to write to registers.
	35	READ	DI[2]	**Read.** Pull Low to read from registers.
	36 37 38 39 40 41 42 43	D0 D1 D2 D3 D4 D5 D6 D7	DI[1]/O	**Data Bits.** Eight-bit, parallel data bus.

1. Input is a Schmidt triggered circuit and includes an internal pull-up device.
2. Input is a Schmidt triggered circuit and includes an internal pull-down device.
3. Input includes an internal pull-up device.
4. Input includes an internal pull-down device.
5. DI = Digital Input; DO = Digital Output; DI/O = Digital Input/Output; AI = Analog Input; AO = Analog Output; AI/O = Analog Input/Output; S = Supply.

3.0 Functional Description

The Enhanced MDSL Data Pump (EMDP) chip set provides synchronous, full duplex data transport on a single twisted wire pair using 2B1Q line coding and echo cancellation. The EMDP provides symmetrical data transport at any line rate from 272 to 1,168 kbps. This document specifies performance at a few typical line rates, but all line rates between 272 and 1168 kbps are allowed. The EMDP includes an internal state machine and can activate and operate without a processor. The EMDP can transport data which is synchronous, asynchronous, or near-synchronous (pleisiochronous) to the line rate of the Data Pump. Several new features have been added in the EDSP chip as compared to previous MDSP and HDX - SK70720, SK70706, SK70708, and SK70707.

The EMDP chip set consists of the IAFE chip and EDSP chip. The following paragraphs describe the chip set components with reference to internal functions and their interfaces.

3.1 Integrated Analog Front End (IAFE)

The IAFE incorporates the following analog functions:

- Transmit driver
- Transmit and receive filters
- Phase-Locked Loop (PLL)
- Analog-to-digital converter

The IAFE provides the complete analog front end for the EMDP. It includes: transmit pulse shaping, line driver, receive A/D converter, and the VCO portion of the receiver PLL function. Transmit and receive control signals are exchanged between IAFE and EDSP through a serial port. The IAFE line interface uses a single twisted pair line for both transmit and receive.

3.1.1 IAFE Transmitter

The IAFE transmitter performs 2B1Q coding, pulse shaping and driving functions. It generates a shaped output pulse at the baud rate and has one of four levels determined by TMAG and TSGN. Refer to Test Specifications for frequency and voltage of the pulse templates.

3.1.1.1 2B1Q Line Code

The 2B1Q line code utilized in the EMDP is same as that selected by ANSI and ETSI as the preferred line code for ISDN BRA and HDSL applications. This line code provides good performance at minimum complexity. The line code utilizes pulse amplitude modulation to encode two data bits (2B) into a single amplitude modulated pulse. The pulse amplitude is restricted to one of four (quaternary) levels. This pulse is familiarly known as a “quat” and gives the second part of the line code its name (1Q). Table 3 shows the encoding scheme used in the 2B1Q system to assign pulse amplitudes to bit pairs. Note that one bit of the pair is used to set the sign (the sign bit), while the second bit (the magnitude bit) controls the magnitude of the pulse. The pulse shape is independent of sign and magnitude and is described in Figure 28.

Table 3. 2B1Q Pulse Coding Rule

Sign Bit	Magnitude Bit	Output Symbol (quat)
1	0	+3
1	1	+1
0	1	-1
0	0	-3

3.1.2 IAFE Receiver

The IAFE receiver is a sophisticated sigma-delta A/D converter. It subtracts the differential signal at the balance input (BTIP/BRING) from the received signal (RTIP/RRING). The output is generated in two stages. The first stage of A/D converter generates AD0 at 32 times the symbol rate. The second stage of the A/D converter samples the noise generated by the first stage and provides the AD1 bit stream at 32 times the symbol rate.

Receiver gain is controlled by the EDSP via the AGC0-2 bits in the Serial Control (SER_CTL) stream. The AGC_SET output from the IAFE is normally Low. It goes High when the signal level in the sigma-delta A/D converter approaches its clipping level thus signaling the EDSP to lower the gain.

The VCO is part of a PLL locked to the received data. The VCO frequency is varied by changing the capacitive load of an external crystal with the help of Tuning Diodes that are biased by the VPLL output. The VPLL output is, in turn, controlled by the EDSP through PLL bits of SER_CTL.

3.2 Enhanced MDSL Digital Signal Processor

The Enhanced MDSL Digital Signal Processor (EDSP) incorporates the following digital functions:

- activation/start-up control, mode selection and the microprocessor interface
- adaptive Echo-Cancelling (EC)
- adaptive Decision Feedback Equalization (DFE), and Feed Forward Equalizer (FFE) using the receive quat stream and the internal error signal
- fixed and adaptive digital-filtering functions
- bit-rate transmit and receive signal-processing including optional scrambling and descrambling

A simple, parallel 8-bit microprocessor interface on the EDSP provides high-speed access to status, control and filter coefficient words. The microprocessor interface provides bit flags for signal presence, synchronization, activation completion. Single-byte words representing receive signal level and the noise margin of the transceiver are also available on the microprocessor interface. One control bit allows the user to start the Data Pump activation sequence. The EDSP controls the complete activation/start-up sequence.

Table 2 lists the EDSP pin descriptions. Refer to Test Specifications for EDSP electrical and timing specifications.

3.2.1 Scrambling

The transmitted 2B1Q symbol must change value frequently to maintain appropriate power spectral density, to limit low frequency content of the transmitted signal and to ensure that adequate signal transitions are available for the receiver to recover clock phase information from the received signal. A standardized mechanism has been adopted to ensure that adequate symbol changes take place. This process is called scrambling, and generates a unique, self-synchronizing pseudorandom data stream. The EMDP includes a data scrambler which complies with industry standard scrambling and unscrambling rules. A 23rd-order polynomial is used to scramble and descramble the data. The scrambler and descrambler polynomial used in the direction of Master to Slave is $X^{-23}+X^{-5}+1$. The scrambler and descrambler polynomial used in the direction of Slave to Master is $X^{-23}+X^{-18}+1$. Here '+' symbol represents 'Exclusive OR' operation. For further details of scrambler and descrambler refer to the following standards:

- ITU G.991.1
- ANSI Committee T1E1.4-TR28 (T1E1.4/96-006)
- ETSI ETR-152

In some applications it may be necessary to bypass the scrambler. An example would be a framing protocol which requires transmission of symbols with alternating +3 and -3 amplitudes. Direct access to the 2B1Q encoder/decoder or the 2B1Q pulse generator is provided in some EMDP operating modes (as described in subsequent sections) in which both bit clocks and quat clocks are provided. Aligning the input data with both these clocks allows the desired quat to be transmitted. When using these operating modes, the user application must ensure that the symbols transmitted have been scrambled in a manner equivalent to that specified in the reference documents.

3.3 EDSP/IAFE Interface

TSGN, TMAG, and TX_CLK provide data interface from EDSP to IAFE. VCO_CLK, AD0 and AD1 provide data interface from IAFE to EDSP. SER_CTL, SRCTL_FS, and AGC_SET provide serial control interface between IAFE and EDSP.

Transmit data, represented by TSGN and TMAG, is clocked from the EDSP using the falling edge of TX_CLK, the transmit clock. The IAFE uses the rising edge of TX_CLK to sample TSGN and TMAG. TX_CLK is eight times the baud rate (equal to 4xBIT_CLK. e.g. for line rate of 784 kbps, TX_CLK is 3.136 MHz). TSGN and TMAG change state at the baud rate, or every 8 cycles of TX_CLK.

The IAFE provides the VCO_CLK to the EDSP which is generated by the IAFE's internal VCO. The A/D converter provides AD0 and AD1 outputs and coincides with the rising edge of VCO_CLK/2. IAFE and EDSP both generate an internal VCO_CLK/2 from the same VCO_CLK. The EDSP samples AD0 and AD1 with the falling edge of its internal VCO_CLK/2.

The serial control stream SER_CTL is provided by EDSP at the rate of VCO_CLK/2 and coincides with its falling edge. A serial control frame strobe signal is also provided by the EDSP with its edge transition occurring at every 16th of the VCO_CLK/2 period and coincides with the falling edge of the VCO_CLK/2. The serial control stream SER_CTL and the framing signal SRCTL_FS is sampled inside the IAFE at the rising edge of VCO_CLK/2.

Figure 5 shows relative timing for the EDSP/IAFE interface.

3.3.1 Serial Control Port

The EDSP continually writes to the serial control port via SER_CTL signal stream. This serial control stream consists of two 16-bit words as shown in Table 4. The data flows from the EDSP to the IAFE at a rate of VCO_CLK/2. TXOFF, TXDIS, and TXTST control the transmit modes. AGC0-AGC2 bits control the Receiver gain. PLL0-PLL7 bits control the VPLL output which is used to control the frequency of VCO. Refer to the Test Specifications section for serial port timing relationships and electrical parameters.

Table 4. EDSP/IAFE Serial Control Port Word Bit Definitions

Bit	Word A (on SER_CTL)	Word B (on SER_CTL)
15	INIT	*n/a*
14	*n/a*	*n/a*
13	*n/a*	*n/a*
12	TXOFF	*n/a*
11	TXDIS	*n/a*
10	TXTST	*n/a*
9	AGC2	*n/a*
8	AGC1	*n/a*
7	AGC0	PLL7
6	FELB	PLL6
5	*n/a*	PLL5
4	*n/a*	PLL4
3	*n/a*	PLL3
2	*n/a*	PLL2
1	*n/a*	PLL1
0	*n/a*	PLL0

3.4 Line Interface

The Data Pump line interface consists of three differential pairs. The transmit outputs TTIP and TRING, receive inputs RTIP and RRING, and the balance inputs BTIP and BRING, all connect through a common transformer to a single twisted-pair line (Figure 26 and Figure 27). The transmit outputs require resistors in series with the transformer. A passive pre-filter is required for the receive inputs. The balance inputs feed the transmit signals back to the Data Pump providing passive echo cancellation. Protection circuitry could be used if required. Refer to application note AN79 for further details of line protection circuits.

3.5 Data Interface

The EMDP data interface provides three distinct operating modes: Transparent, Independent and Framed. The operating modes can be configured using the MODE_S3, MODE_S2, and MODE_S1 pins of the EDSP. Table 5 lists various operating modes along with their key features.

Figure 6 illustrates generic data transport using the MDSL system. Data is clocked into a transmitter, encoded as a 2B1Q signal, sent over the line, and clocked out of the receiver of the far-end transceiver. Data is transmitted simultaneously in both directions.

Figure 5. EDSP/IAFE Interface – Relative Timing

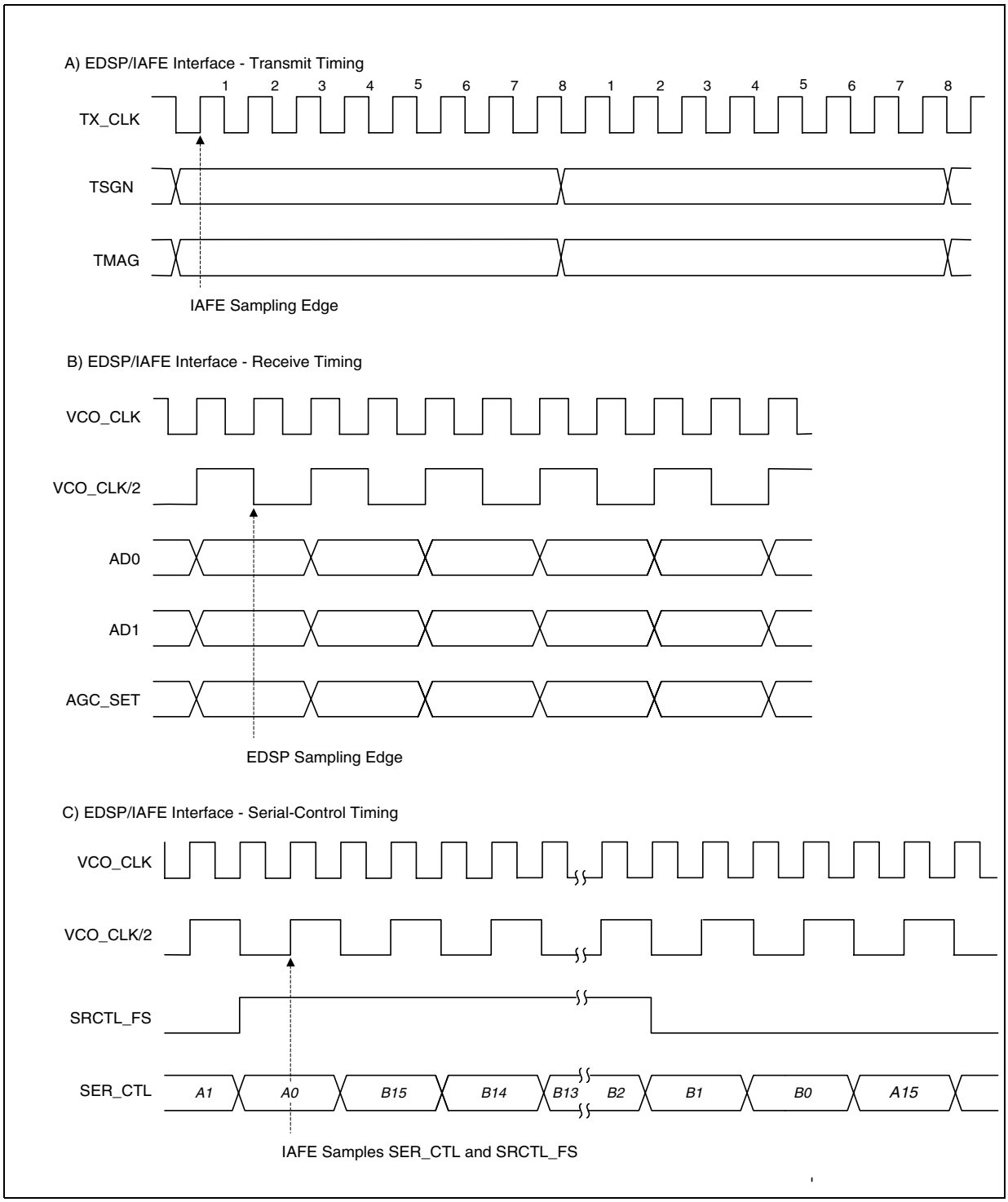
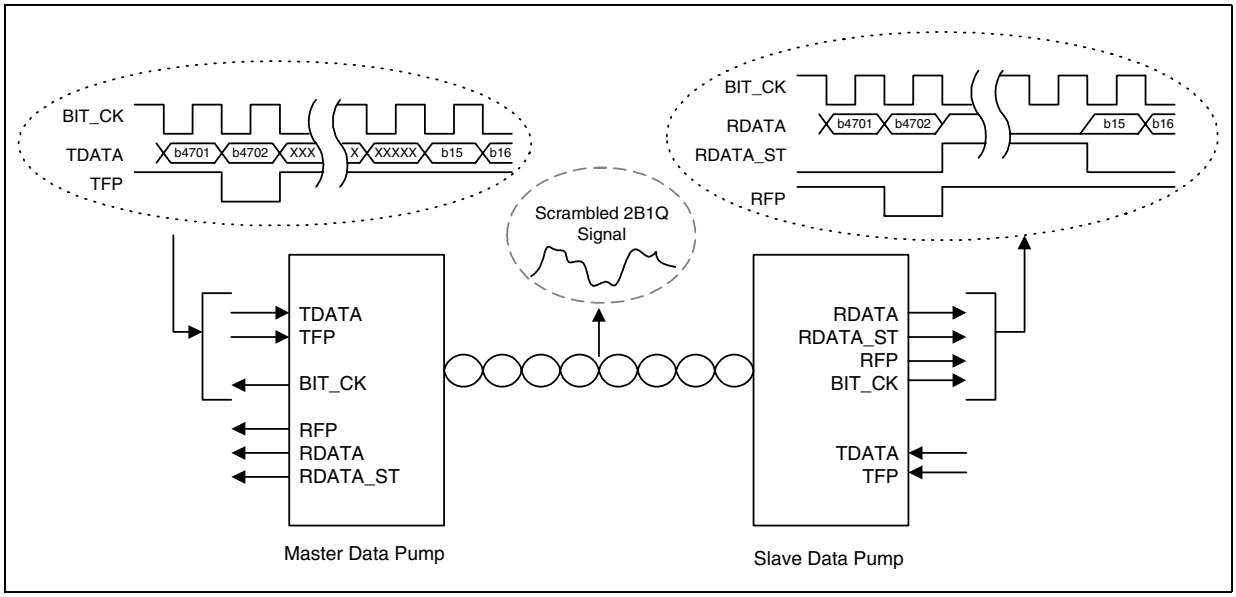


Table 5. EMDP Data Mode Selection

Mode Select Pin (MODE_Sn)			Scrambler Enabled while Active	Sign bit First	Independent Transmit and Receive Timing	Framed	Frame Length (bits)	Mode	
3	2	1						Name	#
0	0	0	No	Yes	No	No	*n/a*	Transparent Operation	0
0	0	1	No	No	No	No	*n/a*	Transparent Operation	1
0	1	0	Yes	*n/a*	No	No	*n/a*	Transparent Operation	2
0	1	1	*n/a*	*n/a*	*n/a*	*n/a*	*n/a*	Reserved	3
1	0	0	No	Yes	Yes	No	*n/a*	Independent	4
1	0	1	Yes	*n/a*	Y	No	*n/a*	Independent	5
1	1	0	Yes	*n/a*	No	Yes	7006/7010	Framed ETSI	6
1	1	1	Yes	*n/a*	No	Yes	4702/4706	Framed ANSI	7

Figure 6. MDSL System Data Transport (Framed Mode Shown)



3.5.1 Transparent Mode

Transparent operating modes are used for the transport of asynchronous data or fully synchronous data (which may have been framed by an external device). All Transparent modes have common transmit and receive clocks and provide an optional internal scrambler/descrambler. If the scrambler is bypassed, the application must align the data appropriately to ensure that the correct 2B1Q symbol is transmitted. Data may be input with either the sign or magnitude bit first.

The appropriate selection of mode enables operation compatible with other vendor's framers. In this mode the use of a single clock for transmit and receive data results in small, but uncontrolled, data delays.

3.5.2 Independent Mode

In Independent timing mode the EMDP provides separate transmit and receive clocks at the data interface. Both clocks are at the same rate, but the clock phases are independent. In this mode, minimum delay of the data is assured. In addition, delay is constant for subsequent activations on the same loop. Constant delay is necessary for applications such as alignment of transmitted signals from radio base stations where data delay must be precisely measured and controlled. An optional internal scrambler is available in Independent mode.

3.5.3 Framed Mode

Framed mode is provided for compatibility with previous MDSPs and HDXs - SK70720, SK70706, SK70707, and SK70708. Framed mode is useful for applications in which pleisiochronous data must be transmitted while maintaining accurate timing information.

The EMDP can embed a 14-bit Frame Synchronization Word (FSW) and optional stuffing bits in the data stream that divides the data into MDSL frames with average length of 4704 or 7008 bits as shown in Figure 7. The Framed mode, with associated stuffing, provides two primary functions:

- Transports plesiochronous data, where data rate is not precisely related to the line rate and the data rate in each direction of transmission is different while retaining frame alignment.
- Provides an MDSL frame position indicator that may be used in time-division-multiplexed systems to relate time slots in the MDSL frame to those in an application frame.

Note: The EMDP frame sync word format and frame length are fully compatible with those defined for 784 and 1,168 kbps HDSL applications in the ITU G.991.1, ANSI Committee T1E1.4-TR28 (T1E1.4/96-006), and ETSI ETR-152 standards. The EMDP is fully transparent to all data except the frame sync word. It does not provide other framing functions defined for HDSL.

Each frame contains either a 4,688 or 6,992 payload data bits. There are no restrictions on the data patterns which can be transmitted in the payload data. The application synchronizes data to the EMDP framing by generating a pulse on the transmit frame pulse input, TFP. The transmitter sends the FSW in the first 14 bits following the rising edge of TFP. Application data is not transmitted or buffered during the transmission of the FSW.

The EMDP receiver detects the incoming FSW and provides a blanking signal (RDATA_ST) at its output to indicate that payload data is not present during the FSW. The RDATA_ST signal can also be used to gate the receiver clock signal (BIT_CLK) so that clock transitions are present only when payload data is available.

3.5.3.1 Bit Stuffing

Some applications require that data be transported at a rate which is externally controlled and varies slightly from a nominal payload data rate. The EMDP framed mode allows the application to modify the payload data rate slightly without changing the line rate so that each of the payload bits contains a valid data bit. To operate in this mode, the EMDP uses a mechanism known as bit stuffing. By properly choosing the line rate of the MDSL system and using the stuffing mechanism, the application can transmit data at slightly different rates in both directions simultaneously while using a common, fixed MDSL line rate.

When stuffing is employed, the application inserts an additional four bits not carrying payload data in the data stream between the end of the 4,688 (or 6,992) payload bits and the beginning of the next FSW as shown in Figure 8. This is accomplished by delaying the TFP pulse by four BIT_CLK periods from its normal position. The EMDP receiver detects this four bit change in the location of the FSW and adjusts its payload data strobe indicator (RDATA_ST) to indicate that the four additional bits do not contain payload data and should be suppressed along with the FSW which follows them. This mode of operation is frequently used in the transport of T1 or E1 signals where the upstream and downstream data rates are not the same and are not exactly at the nominal rate.

Table 6 provides the minimum and maximum data rates and frame times for several line rates. Although the EMDP can only transport data at either of these two instantaneous rates, it can support any average data rate between them by adjusting the ratio of frames with stuffing to those without stuffing. When alternate frame stuffing is used the EMDP will transport data at the nominal rate shown in Table 6. If necessary, a PLL tracking the Receive Frame Pulse (RFP) output or a gapped clock produced by combining RDATA_ST and BIT_CLK can be used to create a continuous (i.e., not gapped) clock whose frequency is at the average receive data rate. The PLL characteristics depend on the jitter and wander requirements for the output clock.

Figure 7. MDSL Frame Example (4,702 bits per frame)

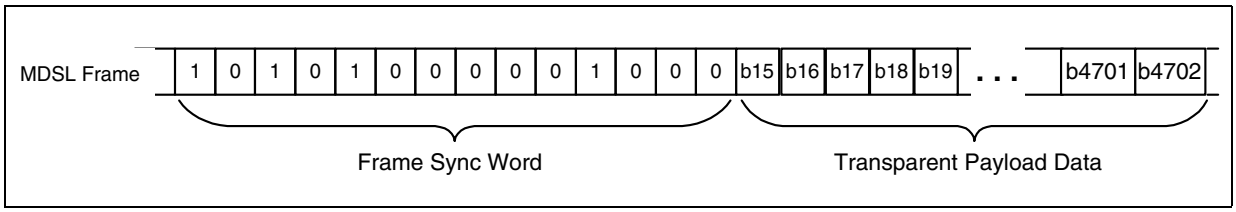


Figure 8. Example of Framing With and Without Stuff Bits(4,702 bits per frame)

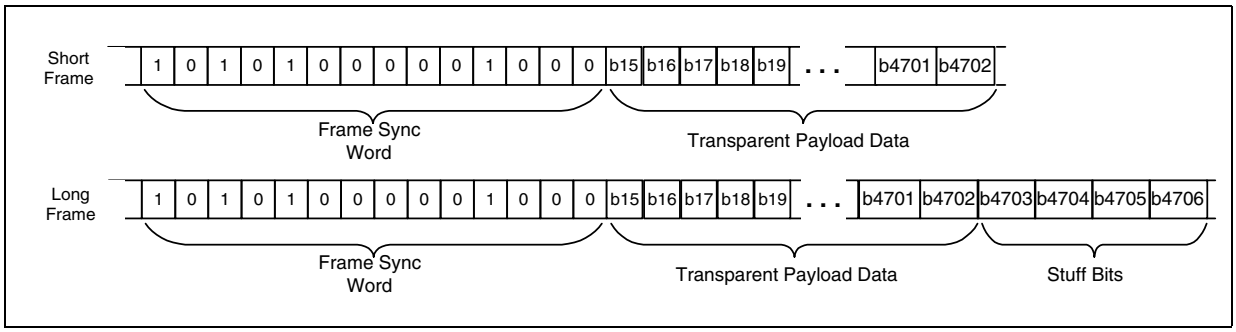


Table 6. Min, Max and Alternate Bit Stuffed Frame Timing and Payload Data Rate

Line Rate (kbps)	4702 bit Frame		4706 bit Frame		Alternate bit stuffed frame	
	Frame Length (ms)	Payload data rate (kbps)	Frame Length (ms)	Payload data rate (kbps)	Frame Length (ms)	Payload data rate (kbps)
272	17.287	271.190	17.302	270.96	17.294	271.075
400	11.755	398.809	11.765	398.47	11.76	398.64

1. 7,006 bit Frame.
2. 7,010 bit Frame.

Table 6. Min, Max and Alternate Bit Stuffed Frame Timing and Payload Data Rate (Continued)

Line Rate (kbps)	4702 bit Frame		4706 bit Frame		Alternate bit stuffed frame	
	Frame Length (ms)	Payload data rate (kbps)	Frame Length (ms)	Payload data rate (kbps)	Frame Length (ms)	Payload data rate (kbps)
528	8.905	526.428	8.913	525.981	8.909	526.204
784	5.997	781.666	6.003	781.001	6.000	781.333
1,168	5.998[1]	1,165.666[1]	6.002[2]	1,165.001[2]	6.000	1,165.333

1. 7,006 bit Frame.
2. 7,010 bit Frame.

4.0 Operation

This following paragraphs provide details of the operation of the EMDP including:

- operating modes
- timing and data synchronization
- control modes
- register access
- activation
- frame synchronization
- deactivation

4.1 Operating Modes

As listed in Table 5, EMDP supports the following operating modes:

- Transparent operating mode
- Independent operating mode
- Framed mode

Some of these operating modes have a number of options as described below. Selection of the modes and the options is controlled with three mode select signals: MODE_S1, MODE_S2 and MODE_S3.

4.1.1 Transparent Operating Modes (0:2)

Transparent operating Mode transmits data supplied at the TDATA input completely transparent without changing it. Within Transparent operating Mode three options are available:

- The internal scrambler disabled, sign bit transmitted first (mode #0).
- The internal scrambler disabled, magnitude bit transmitted first (mode #1).
- The internal scrambler enabled, sign bit transmitted first (mode #2).

When the internal scrambler is disabled, the incoming data must be aligned with the quat clock. The data may be aligned with either the sign bit or the magnitude bit first. If the scrambler is disabled the user must assure that the 2B1Q pulses are properly scrambled to meet the system PSD and performance requirements. In Transparent operating Mode with the scrambler disabled the EMDP could be compatible with other vendor framers while transporting data. In addition, the EDSP uses internal signals during the activation process to ensure easy and reliable activation. The transmit and receive data signals share common bit clocks and baud clocks in Transparent operating Mode. Figure 9, Figure 10 and Figure 11 show the data and clock relationships available in Transparent operating Mode.

Figure 9. Clock/Data Timing: Transparent Mode #0, Sign First, Not Scrambled

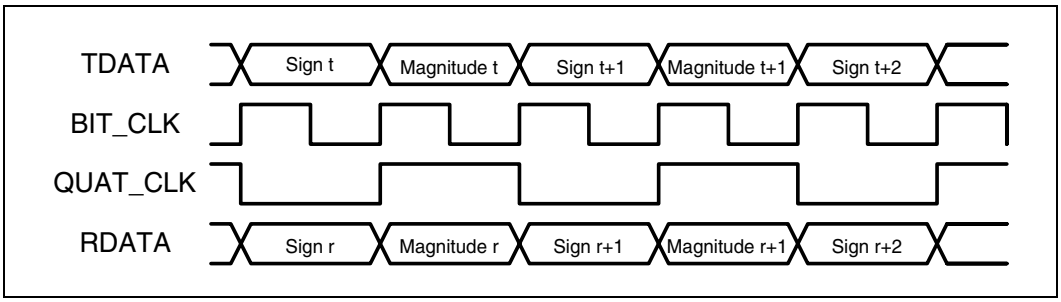
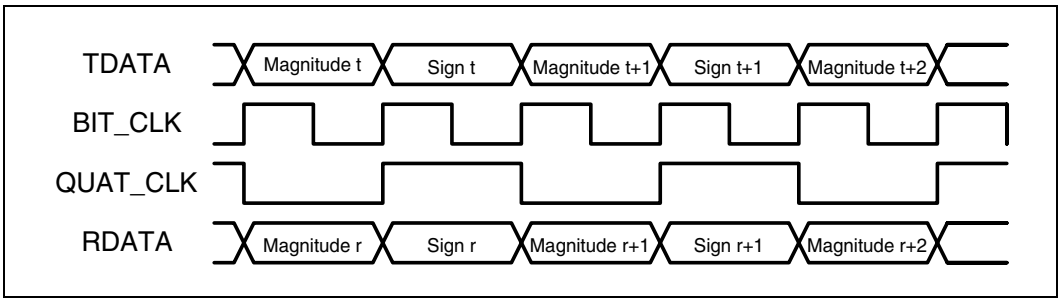


Figure 10. Clock/Data Timing: Transparent Mode #1, Magnitude First, Not Scrambled



4.1.2 Independent Operating Modes (4:5)

The Independent operating modes provided by the EMDP use separate transmit and receive clocks to minimize data transport delay (latency) and to provide constant data delay within the EMDP. In a transmission system delay occurs in the transmitter, the transport media and the receiver. The EMDP has small and constant delay in the transmitter and receiver by design. The medium dependent delay changes linearly with the length of the twisted pair wire. In Transparent operating mode there is an additional receiver delay required to align the received signal with the BIT_CLK at the data I/F. The magnitude of this delay is variable, ranging from 0 to a full baud period. Independent mode removes this delay by providing separate transmit and receive clocks so that the received data can be output as soon as it is available.

Independent mode has another option, to enable or disable the internal scrambler. If the scrambler is bypassed, the user must assure that the 2B1Q pulses are properly scrambled to meet the system PSD and performance requirements. The data must be presented with the sign bit first. Figure 12 and Figure 13 show the data and clock relationships available in Independent Mode.

Figure 11. Clock/Data Timing: Transparent Mode #2, Scrambled

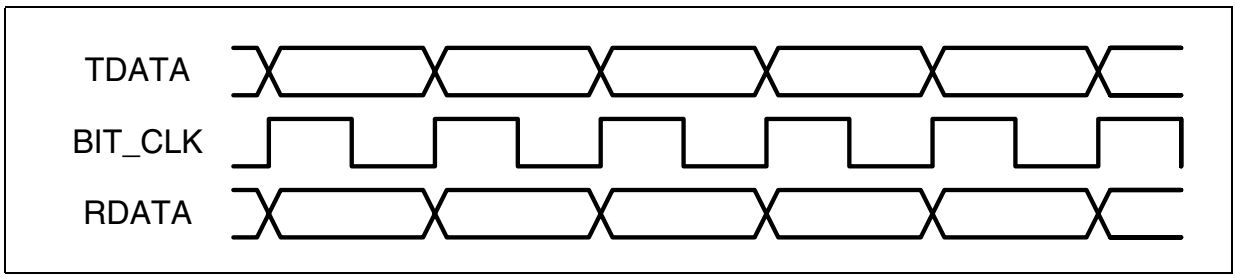


Figure 12. Clock/Data Timing: Independent Mode #4, Sign First, Scrambler Disabled

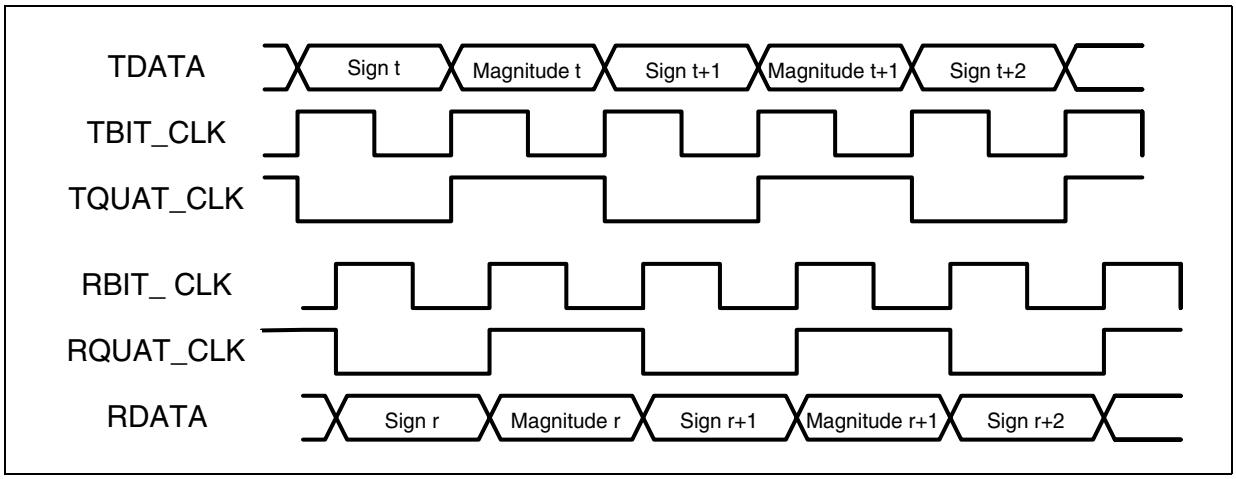
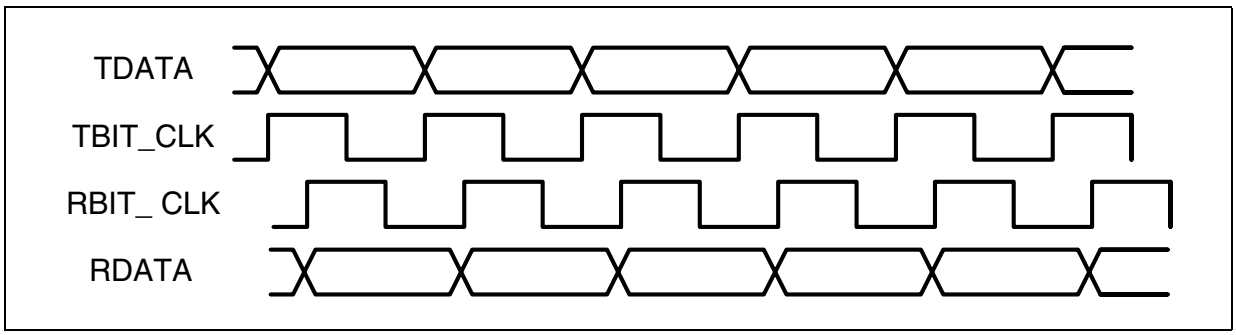


Figure 13. Clock/Data Timing: Independent Mode #5, Scrambled



4.1.3 Framed Operating Modes (6:7)

The EMDP has two Framed operating modes and can be used in a number of different applications. The basic framing functions provide ETSI and ANSI compatible framing sequences when operated at the appropriate line rate. In mode 6 the frame length is either 7006 or 7010 bits long. When operated at a nominal line rate of 1168 kbps this framing structure is compatible with the ETSI framing structure specified for two pair HDSL systems. In mode 7 the frame length is either 4702 or 4706 bits long. When operated at a nominal line rate of 784 kbps this framing structure is compatible with the ANSI framing structure specified for two pair HDSL systems and the ETSI structure for three pair HDSL systems. Both framing modes provide bit stuffing capability so that pleisiochronous data streams may be transported without error and with acceptable jitter and wander. The scrambler is always enabled when either mode 6 or mode 7 is selected.

4.1.3.1 Data Interface Timing

This section provides guide lines for operating the EMDP in framed mode. Detailed information on operation is contained in the MDSL data sheets for the standard MDSL chip set (SK70720/70721).

The EMDP data interface provides for the transfer of binary data to and from the transceiver using the 272 to 1,168 kHz clock, BIT_CLK, generated by Data Pump. Figure 14 and Figure 15 show the data interface timing for modes 6 and 7. Since the only difference between these modes is the number of bits per frame, the convention used in this section will be to write appropriate bit numbers consequently for modes 6 and 7, separated by a slash (for instance, 4702/7006).

In the transmit direction, payload data is sampled from TDATA during bits b15-b4702/7006 of each frame. Frame sync word bits (b1-b14) are internally generated in the EDSP. The state of TDATA during b1-b14 is ignored. For fixed line rate applications an external counter must drive the TFP input Low for one complete BIT_CLK cycle. This signal on TFP establishes the start of an MDSL frame - bit 1 of the frame begins immediately after the end of this signal on TFP. The external data source must suppress data for 14 bit periods during the internally generated frame synchronization word, bits 1-15. In variable line rate applications, bit stuffing logic adjusts the time between TFP pulses to match the average line rate of the Data Pump and the data rate of the external source. In both the cases - fixed and variable line rate, the TFP signal should be valid prior to an activation request to the Master Data Pump. A valid TFP signal should be generated after power-up, before or immediately after LOS goes Low for the Slave Data Pump. During initialization and anytime thereafter TFP must not be held Low for more than 2 BIT_CLK cycles or the data interface output signals will be disabled. If the TFP signal is inactive (always High or unconnected) when activation starts, the Data Pump may activate but will inject synchronization bits in every frame and stuff bits into every other frame. Since the Data Pump will not be synchronized to the data source these internally generated bits will overwrite payload data. If the position of TFP changes, the Data Pump will immediately reset the transmit frame alignment, typically causing a temporary loss of frame alignment at the other end.

In the receive direction, the binary data output on RDATA contains the 14-bit frame synchronization word (b1-b14), the transparent payload data (b15-b4702/7006) and optional stuff bits (b4703-b4706/b7007-b7010). The data strobe signal RDATA_ST is High during the frame synchronization word and stuff bits and Low during payload data. RDATA_ST can be used to create a gapped receive payload data clock by suppressing BIT_CLK cycles when RDATA_ST is High. RFP is the receive frame synchronization output that goes Low during the first bit of every MDSL frame. In variable data rate applications the original data timing can be recovered from RFP using a PLL.

During the activation process, no data are transmitted until the Noise Margin is greater than -5 dB and the frame synchronization word has been detected in 6 consecutive frames. The output data line, RDATA, is held High until $\overline{\text{ACTIVE}}$ goes Low to indicate link activation has been completed.

Figure 14. Clock/Data Relationships: Framed Mode (#6), Scrambled (7006/7010 bits per frame)

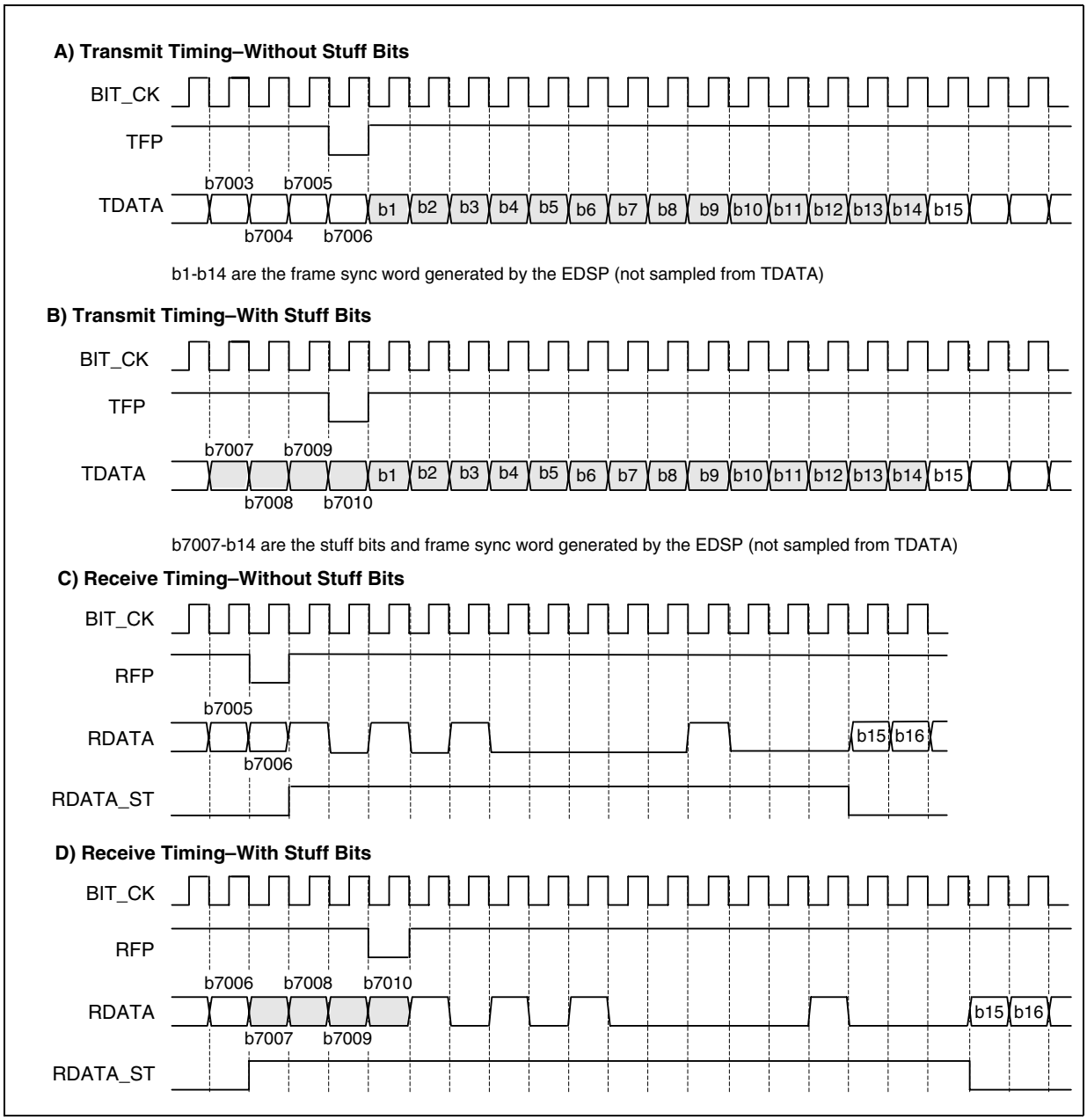
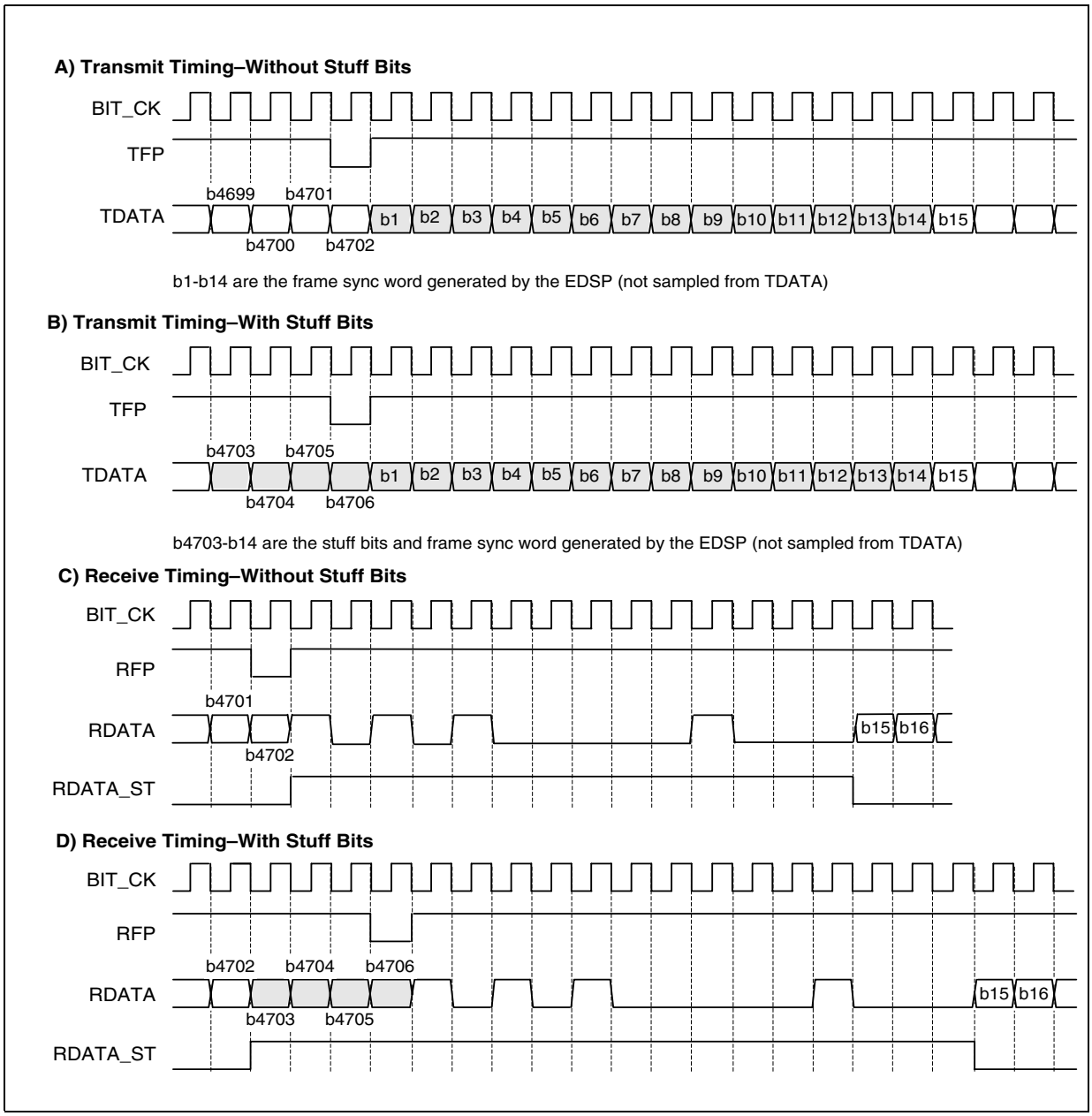


Figure 15. Clock/Data Relationships: Framed Mode (#7), Scrambled (4702/4706 bits per frame)



4.2 Timing and Data Synchronization

The EMDP implements a synchronous, echo-cancelled communications system. For such a system to work properly, both Data Pumps must share a common clock. This common system clock is generated at the Master and sent over the data link to the Slave Data Pump. Figure 16 shows an MDSL link between a Master and Slave transceiver. This figure illustrates the clock/timing

architecture of the Data Pump in both modes. Link activation is initiated by the Master mode device which also operates as the MDSL timing source. The Slave mode device recovers the MDSL clock from the received data and uses this clock to transmit data towards the Master.

A Master Data Pump derives its line transmit clock and data interface clocks from MSTR_CLK by dividing it by 16. MSTR_CLK also provides a ±32 ppm accurate local training reference for the receiver clock recovery VCXO before activation. When active, the Master Data Pump uses the VCXO, as part of PLL, for clock recovery from the line. Since the Slave clock is synchronous with the Master clock after activation, the result is that the transmit and receive signals and clocks all operate at the same frequency. There is, however, an unknown phase difference between the two clocks at the Master. All received clocks are subject, in addition, to degradation due to jitter and wander.

At the Slave transceiver, SLAVE_CLK is used only to train the VCXO frequency within ±32 ppm before activation. After activation, the Slave Data Pump derives the transmit clock, receiver internal clock and data interface bit clock from the PLL locked to the received clock.

An internal FIFO is provided so that the receive data at the Master can be aligned with the bit clock derived from the MSTR_CLK. This FIFO is disabled in Independent mode.

To select the clock and crystal frequencies required for a specific application, the required line rate must first be calculated from the specified payload data rate. In the case of transparent and Independent operating modes, the line rate would be equal to the payload data rate. In the case of framed operating modes, line rate would be calculated as follows:

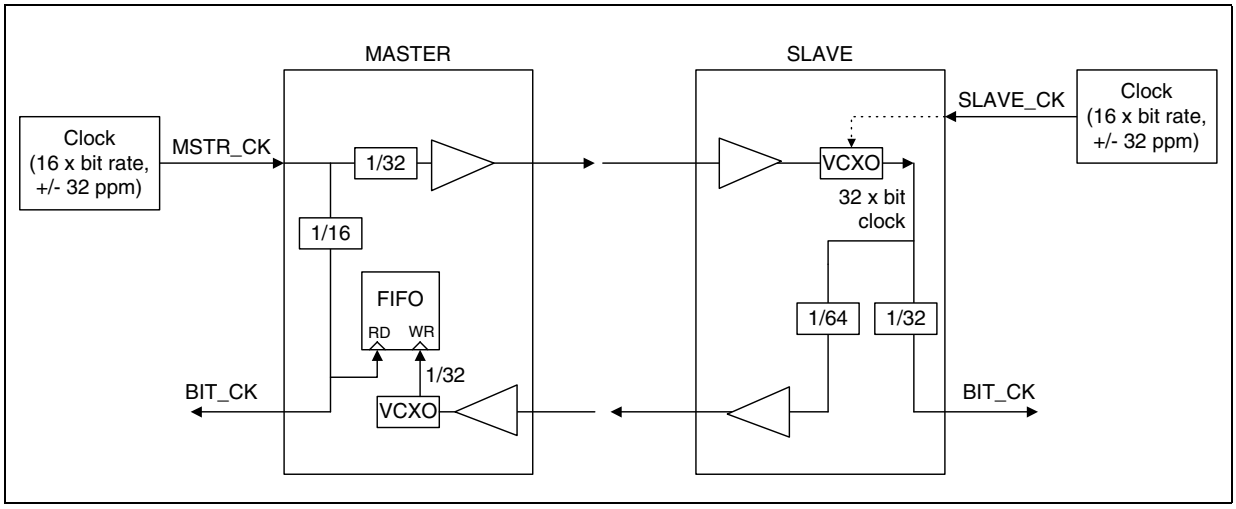
Operating mode 6, no bit stuffing: line rate = (7006/6992)*payload data rate.

Operating mode 6, with bit stuffing: line rate = (7010/6992)*payload data rate.

Operating mode 7, no bit stuffing: line rate = (4702/4688)*payload data rate.

Operating mode 7, with bit stuffing: line rate = (4706/4688)*payload data rate.

Figure 16. EMDP Clock Distribution In Master and Slave Modes



4.3 Control Modes

The EMDP includes an integrated, hardware controlled state machine unique to Intel DSL Data Pumps. The hardware control mode allows the design of low cost, low power MDSL systems which do not require the support of a microprocessor. Thus, in the hardware control mode no programming is required. Where it is desirable to use the full capabilities of the EDSP, a microprocessor interface provides access to the internal registers of the EDSP. The next two sections describe both control modes.

4.3.1 Hardware (Stand-alone) Control

In hardware control mode the EMDP utilizes I/O pins to provide simple activation control and status indication. These I/O pins are multiplexed with the pins used for the microprocessor interface. Figure 17 shows the pin functions in hardware control mode. Note that the hardware mode select pins ($\overline{\text{HWSEL1}}$, $\overline{\text{HWSEL2}}$, and $\overline{\text{HWSEL3}}$) are used for the $\overline{\text{CHIPSEL}}$, $\overline{\text{READ}}$, and $\overline{\text{WRITE}}$ signals when in microprocessor mode. Holding these three pins Low causes the EDSP to enter in the Hardware Control Mode.

4.3.1.1 ACTREQ

Setting ACTREQ pin High initiates the activation state machine. ACTREQ is a level sensitive signal. ACTVNG signal goes High and stays High until the Data Pump activates. Upon activation, LOS pin goes Low. TMR_EXP pin goes High after activation timer expires. If link is disconnected due to any reason, DEACTVTD pin goes High and stays High until the Data Pump reaches inactive state.

4.3.1.2 ILMT

Setting ILMT pin High enables Data Pump to send all 1's scrambled pattern on the loop. This is mainly useful in measuring power spectral density of the transmitted signal. In the case of framed operating modes, the signals transmitted are framed, with unscrambled synchronization word and without stuffing bits. In case of Transparent and Independent operating modes, the signals transmitted are scrambled and unframed.

4.3.1.3 TXTST

Setting TXTST pin High enables the Data Pump to transmit isolated pulses. Amplitude of the pulses depends upon the TDATA and TFP pin status. TDATA controls the sign and TFP controls the magnitude of the transmitted pulses according to the 2B1Q encoding rules described in Table 3. The TXTST function is available only in framed operating modes 6 and 7. In framed operating mode 6, the pulses are transmitted every 7008 BIT_CLK cycles, corresponding to the ETSI framing sequence. In framed operating mode 7, the pulses are transmitted every 4704 BIT_CLK cycles. TXTST is available only in the Inactive state of the Data Pump.

4.3.1.4 Repeater Mode (RPTR)

Setting the RPTR pin High enables Data Pump in Master mode to configure in repeater mode. This ensures that the phase of the BIT_CLK in Master mode is aligned with the TFP pulse. Note that to configure two Data Pumps to operate as a repeater, MASTER_CLK output from Slave Data Pump is connected to MASTER_CLK input of adjacent Master Data Pump. RFP of the Slave Data Pump is connected to TFP input of Master Data Pump. In Slave mode, RPTR pin has no function and can be pulled Low or High.

4.3.1.5 Front -End Loopback Mode (FELB)

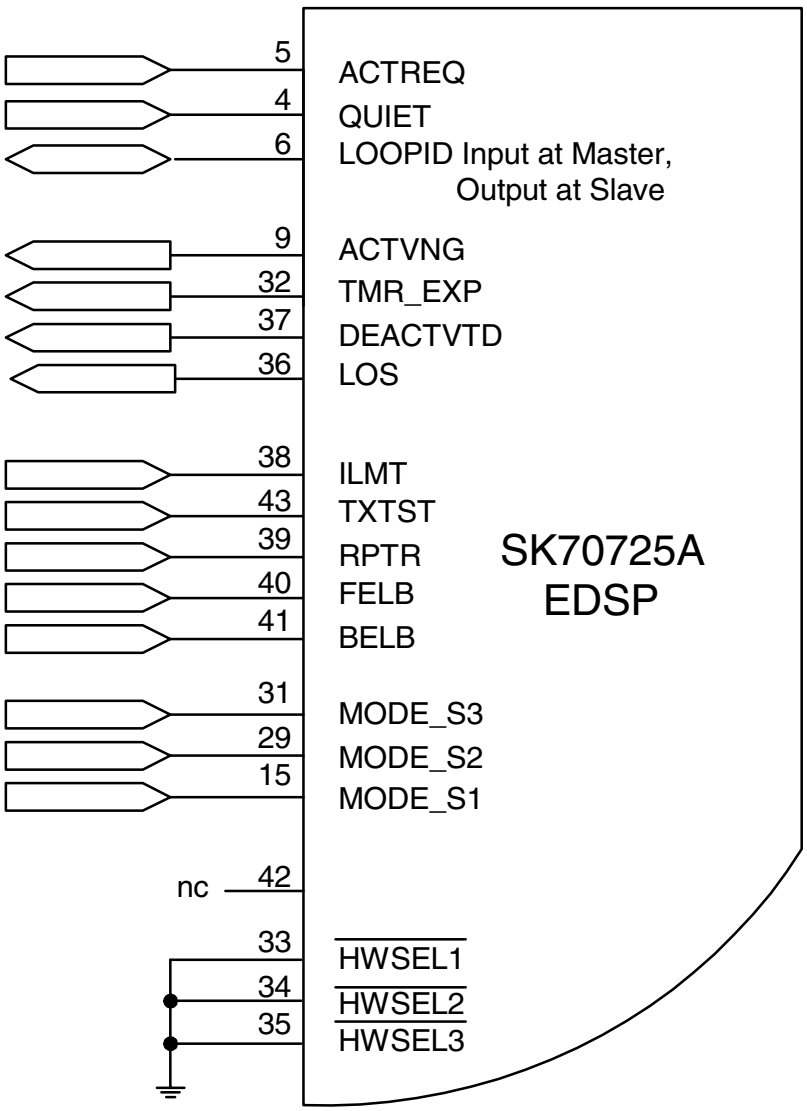
Setting the FELB pin High enables the Data Pump to configure in front end loop back. The Data Pump must be in Master mode. Upon setting ACTREQ pin to High, the Data Pump will begin activation using its own signals received at the BTIP and BRING inputs. Proper operation in this mode is dependent on the configuration of external line interface circuit components.

4.3.1.6 Back-End Loopback Mode (BELB)

Setting the BELB pin High enables Data Pump to configure in back end loop back. The Data Pump must be in active state. RDATA and RFP outputs are used in place of the TDATA and TFP inputs, respectively. TDATA and TFP signals from the external interface are ignored.

Note: BELB is only available in Framed modes (i.e. modes 6 and 7).

Figure 17. EDSP Control and Status Signals (Stand-Alone Mode)



NOTE: This figure illustrates the EDSP control and status signals in stand-alone mode. All other EDSP and IAFE signals are connected as shown in Figure 26 and Figure 27.

4.3.2 Microprocessor (Software) Control

Three primary control pins, $\overline{\text{CHIPSEL}}$, $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$, select the Software Mode which also uses an interrupt output pin to report status changes. Four additional pins are used for the parallel bus addressing and eight pins for data I/O. See Figure 34 on page 83 and Figure 35 on page 84 for microprocessor interface timing in Software Control Mode.

There are ten write only registers and seven read only registers available in the EDSP. Refer to Table 14 on page 57 for the list of registers.

Note: $\overline{\text{CS}}$ should be asserted Low before asserting $\overline{\text{RD}}$ Low for a minimum of 50 ns. Refer to Figure 35 on page 84 for timing.

4.3.2.1 Chip Select

The Chip Select ($\overline{\text{CHIPSEL}}$) pin requires an active Low signal to enable Data Pump read or write operations.

4.3.2.2 Read Pin

Data is placed on the data bus when the Data Read pin ($\overline{\text{READ}}$) goes Low. When $\overline{\text{READ}}$ is asserted, the EDSP data bus lines go from tristate to active and place the data from the register addressed by ADDR0-ADDR3 on to the data bus D0-D7.

4.3.2.3 Write Pin

The Data Write pin ($\overline{\text{WRITE}}$) requires an active Low pulse to enable a write transfer on the data bus. Data transfer is triggered by the rising edge of the $\overline{\text{WRITE}}$ pulse. To ensure data is written to the register addressed by ADDR0-ADDR3, valid data must be present on the EDSP data bus lines before $\overline{\text{WRITE}}$ goes High.

4.3.2.4 Interrupt Pin

The Interrupt pin ($\overline{\text{INT}}$) is an open drain output requiring an external pull-up resistor. The $\overline{\text{INT}}$ output is pulled Low when an internal interrupt condition occurs. $\overline{\text{INT}}$ is latched and held until Main Status Register RD0 is read. An internal interruption results from a Low-to-High transition in any of the four status indicators: ACTIVE, $\overline{\text{ACTIVE}}$, DEACTVTD or TMR_EXP. Any transition of the LOS indicator will also cause an interrupt. The interrupts associated with transitions of the above mentioned status bits may be masked by setting the appropriate bits in register WR2 as shown in Table 16.

4.3.2.5 Writing Registers

To write to an EDSP register, proceed as follows:

1. Drive $\overline{\text{CHIPSEL}}$ Low.
2. Set the register address on ADDR0-ADDR3.
3. Observe address setup time requirements.
4. Set 8-bit input data word on D0-D7.
5. Pull $\overline{\text{WRITE}}$ Low, observing minimum pulse width.

6. Pull $\overline{\text{WRITE}}$ High, observing hold time requirements for data and address lines.

4.3.2.6 Reading Registers

Procedures for reading the EDSP registers vary by register. Registers RD0, RD1, RD2, RD5 and RD6 are easily accessed. The process for reading registers RD3 and RD4 is more complex. Both processes are described below.

To read registers RD0, RD1, RD2, RD5 or RD6:

1. Pull $\overline{\text{CHIPSEL}}$ Low.
2. Place the desired address onto ADDR0-ADDR3.
3. Pull $\overline{\text{READ}}$ Low.
4. After observing minimum pulse width make $\overline{\text{READ}}$ High to complete the read cycle. (Figure 35)

Registers RD3 and RD4 hold the coefficient values from the DFE, EC, FFE and AGC as shown in Table 18. Register RD3 holds the lower byte value and register RD4 holds the upper byte value. To reconstruct the complete 16-bit word, concatenate the least significant and most significant bytes.

To read registers RD3 and RD4:

1. Select the desired coefficient by writing the appropriate code from Table 18 to register WR3.
2. Enable the Coefficient Read Register by writing a 1 to bit b0 (CRD1) in register WR2.
3. Perform standard register read procedure listed in steps 1 through 6 above to read the lower byte from RD3 and the upper byte from RD4.
4. Concatenate the contents of RD3 and RD4 to obtain the complete 16-bit word.

4.4 Activation

The EMDP integrates all logic required to manage DSL line activation, operation, and deactivation. Figure 18 illustrates the Activation State Machine for unframed modes (0,1,2,4, and 5). Figure 19 illustrates the Activation State Machine for framed modes (6 and 7). In addition to the major states shown in Figure 18 and Figure 19, two of the EDSP states (Activating and Pending Deactivation) have significant sub-states which can be managed for optimum performance. The Activating substates are described in the following: Table 8 and Table 9, Figure 20 and Figure 21.

Note that Activation can be initiated only at the Master Data Pump.

Earlier MDSL Data Pumps operated only in Framed mode. These Data Pumps used FSW, for activation state timing. These Data Pumps also relied on detection of the FSW for changes from one state to another. The EMDP uses the FSW in the activation sequence only in framed modes 6 and 7.

4.4.1 Activation Sequence

When the Master Data Pump is reset, the EMDP goes to the Inactive state. The EMDP remains in the Inactive state until the ACTREQ command is asserted. In the hardware mode when the Master Data Pump is in the Inactive state and the QUIET pin is Low, a Low-to-High transition on the ACTREQ pin initiates activation of the link. In the software mode when the Data Pump is in the Inactive state and the QUIET bit is set to 0, setting the ACTREQ bit to 1 initiates activation of the link. Because the ACTREQ control bit is level sensing, to generate a single request, ACTREQ should be set to 1 and then reset to 0 before the MAT expires.

The activation state machines for Slave and Master EMDP are similar. The primary difference is that the Master activates from and external activation command (ACTREQ) while the Slave device begins activation when signal energy is detected on the loop. Thus, only the Master device can bring up the link. Once the Master begins transmitting, the Slave device will automatically activate and attempt synchronization.

Starting from the Inactive state, the device normally progresses through the Activating, Active1, and Active2 states. In software mode, the ST*n* bits in register RD6 shows the current status of the state machine (Table 27).

During the Activating state, the AGCs, echo canceller, equalizers and timing recovery circuits adapt to the characteristics of a particular transmission line using training signals. Two types of training signals are used by the Data Pump:

- Training Signal S0
  S0 is a two level signal comprised of +3 and -3 only.
- Training Signal S1
  S1 is a four level signal comprised of +3,-3,+1, -1.

The EMDP provides great flexibility in selecting the source of both S0 and S1 signals. See details in Table 7.

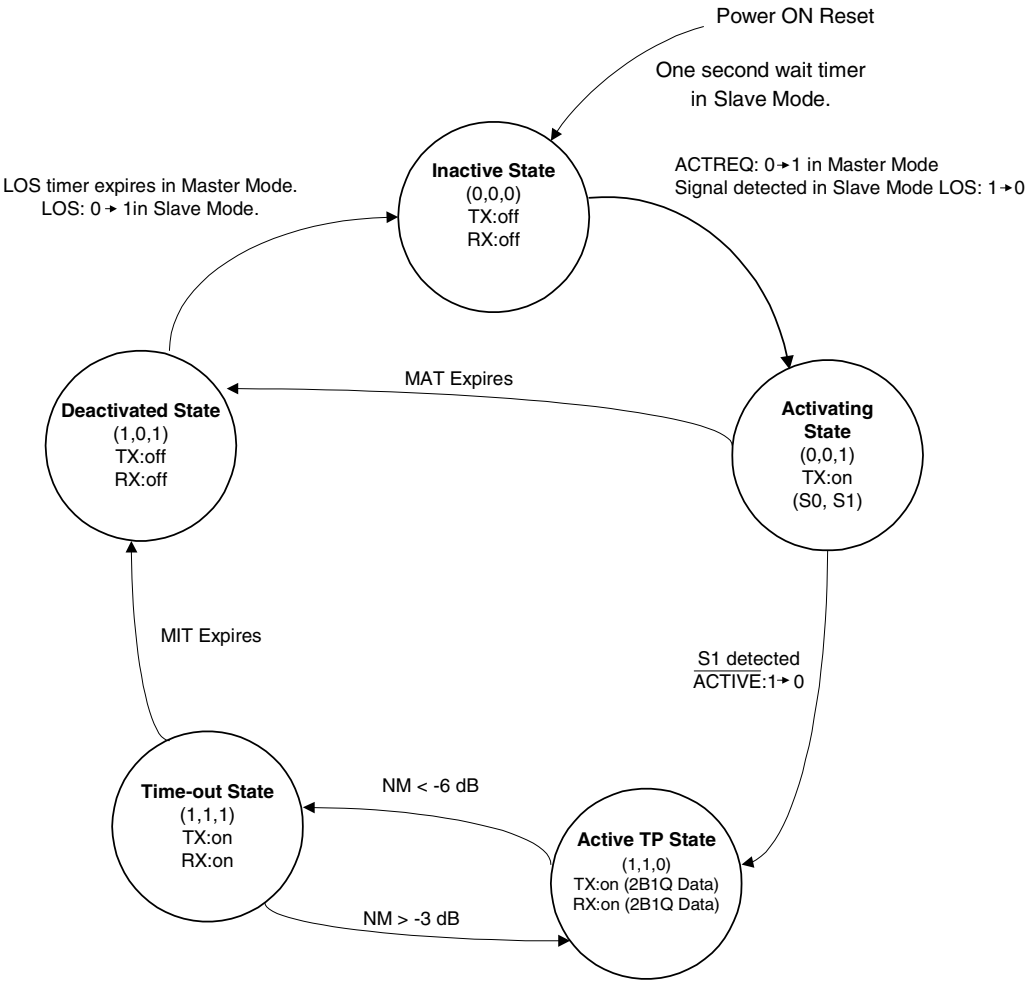
The received data line from the EMDP is held High until the Active1 state is reached because the receiver is not fully trained. Since low error rates cannot be achieved until training is completed, data output is suppressed until the Active1 state is entered in accordance with industry standards. The EMDP, like all Intel DSL Data Pumps, continuously adapts all receiver elements except the AGC in the Active states. This allows the EMDP to perform well in the presence of significant changes in line conditions.

In Independent and Transparent modes (0, 1, 2, 4, and 5) the presence of a FSW cannot be guaranteed. In these modes the EMDP relies only on signal level and signal to noise ratio to move to the Active state. In framed modes, modes 6 and 7, the EMDP searches for the FSW after completing the 4 level detection process. When the FSW is detected in two consecutive frames the device moves to the Active1 state.

The activating state is subdivided into a number of substates. In general the two Data Pumps act as a synchronous machine, providing appropriate signals to the other end of the system during each phase of the activation. Because reliable communications between the Data Pumps is not achieved until the end of the activation process, it is not possible for the Data Pumps to signal each other that a particular process has been completed. The absence of communications between the two Data Pumps led to development of a means of synchronizing the operations of the two Data Pumps which does not require communications between them.

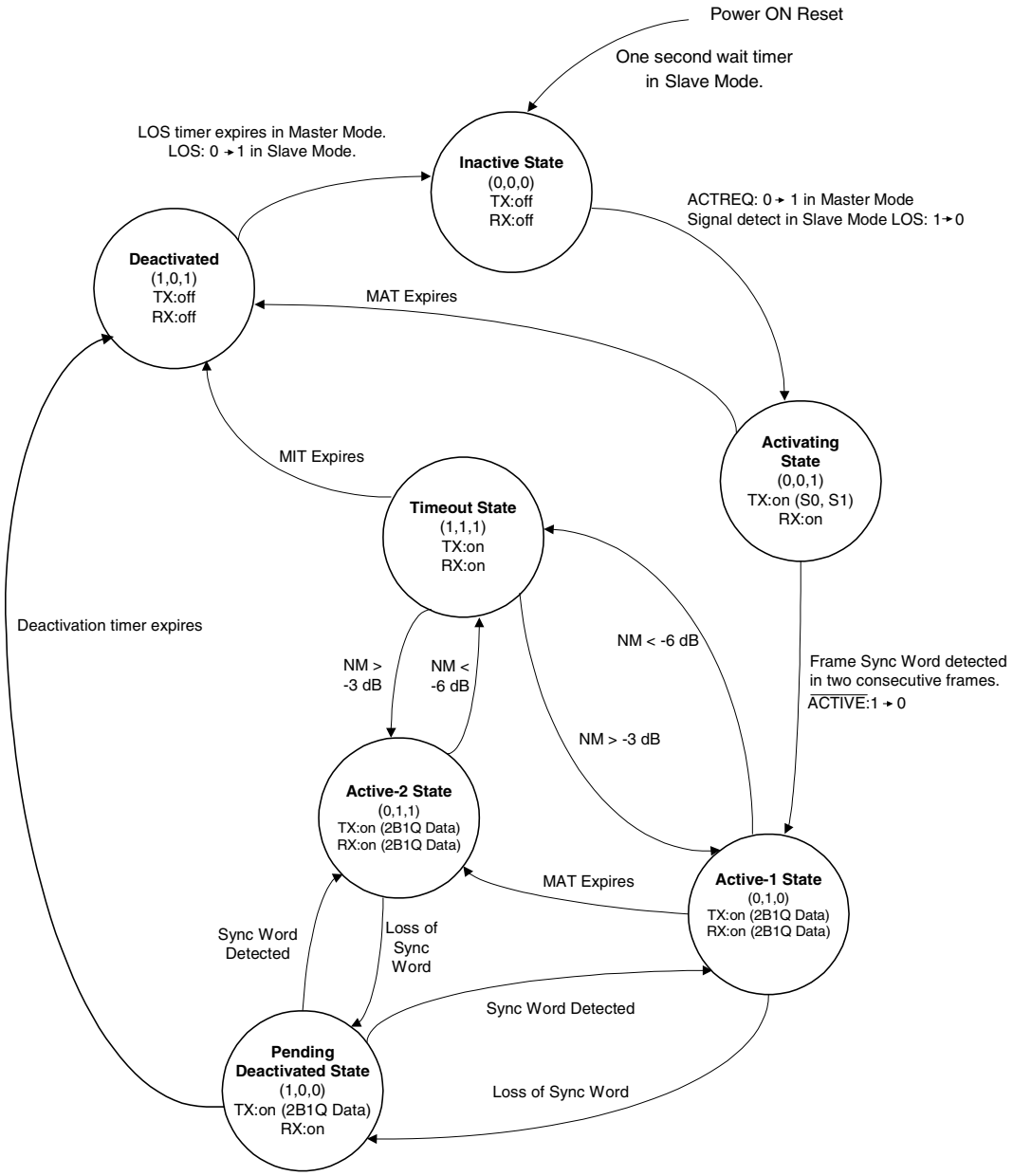
The status of the Activating substates of the EMDP may be determined by reading the Activating Status Register RD5 as shown in Table 8. The contents of the register RD5 may be used to monitor the progress of the training and activation sequence in each of the EMDPs.

Figure 18. Activation State Machine for Modes 0,1,2,4 & 5



Notes:
1. (n,n,n) in each state indicates the status of bits ST2, ST1, and ST0 respectively.
2. MAT: Master Activation Timer.
3. MIT: Micro Interruption Timer.
4. S0 is a two level signal. Signal is scrambled.
5. S1 is a four level scrambled signal. Scrambler is driven by all 1's signal.
6. NM: Noise Margin.
7. Active TP: Active state in mode 0,1,2,4, and 5.

Figure 19. Activation State Machine for Modes 6 & 7



Notes:
1. (n,n,n) in each state indicates the status of bits ST2, ST1, and ST0 respectively.
2. MAT: Master Activation Timer.
3. MIT: Micro Interruption Timer.
4. S0 is a two level signal including Sync Word and Stuff symbols that can be user controlled. Signal is scrambled except Sync Word and Stuffing bits.
5. S1 is a framed four level scrambled signal. Scrambler is driven by all 1's signal and is disabled during sync words and stuffing bits.
6. NM: Noise Margin.

Table 7. EMDP Mode Dependent Activation Signal State

Mode			Xmit Signal	Scrambler Input		D/A Input		Internal Sync Word	Internal Stuffing	Mode	
3	2	1		Sign	Mag	Sign	Mag			Name	#
0	0	0	S0	1	1	S	0	Off	Off	Transparent Operation, Sign First, Not Scrambled	0
			S1	T	T	S	S	Off	Off		
			Active	T	T	T	T	Off	Off		
0	0	1	S0	1	1	S	0	Off	Off	Transparent Operation, Mag First, Not Scrambled	1
			S1	T	T	S	S	Off	Off		
			Active	T	T	T	T	Off	Off		
0	1	0	S0	1	1	S	0	Off	Off	Transparent Operation, Sign First, Scrambled	2
			S1	T	T	S	S	Off	Off		
			Active	T	T	S	S	Off	Off		
0	1	1	Reserved								3
1	0	0	S0	1	1	S	0	Off	Off	Independent, Sign First, Not Scrambled	4
			S1	T	T	S	S	Off	Off		
			Active	T	T	T	T	Off	Off		
1	0	1	S0	1	1	S	0	Off	Off	Independent, Sign First, Scrambled	5
			S1	T	T	S	S	Off	Off		
			Active	T	T	S	S	Off	Off		
1	1	0	S0	1	1	S	0	On	On	E1 Framed Mode	6
			S1	T	T	S	S	On	On		
			Active	T	T	S	S	On	On		
1	1	1	S0	1	1	S	0	On	On	T1 Framed Mode	7
			S1	T	T	S	S	On	On		
			Active	T	T	S	S	On	On		

1. Note: T - Transparent signals, S - Scrambled signals.

Table 8. Details of Activating State

ACT Bits RD5 [3:0]	EMDP Master States				EMDP Slave States			
	Receiver State	State Description	Ends at	Xmit Signal	Receiver State	State Description	Ends at	Xmit Signal
0000	Inactive	Remains until ACTREQ is asserted	ACTREQ	None	Inactive	Remains until S0 signal is detected	LOS=0	None
0001	Pre-AGC	Presets AGC with only local signal present	SMT1	S0	Wait	Trains analog AGC	SMT2	None
0010	Pre-EC	Pre-trains echo canceler with only local signal present	SMT2	S0	AAGC	Continues to train analog AGC	SMT1	S0
0011	SIGDET	Waits for receipt of signal from Slave	LOS=0	S0	EC	Trains echo canceler and digital AGC	SMT3	S0
0100	AAGC	Trains analog AGC	SMT3 + TDELTA	S0	PLL1	Trains PLL to frequency of received signal	SMT5	S0
0101	EC	Trains echo canceler and digital AGC	SMT4 + TDELTA	S0	PLL2	Trains PLL to phase of received signal. Train DFE and FFE	SMT4	S0
0110	PLL	Trains PLL to phase of received signal.Train DFE and FFE.	SMT5 + TDELTA	S0	4LVLDET	Detects S1.	Data Driven	S0
0111	4LVLDET	Detects S1	Data Driven	S1	Not present in modes 0 - 5			
0000	Active	Fully Active		S1	Active	Fully Active		S1
The following states are present only in framed modes 6 and 7								
0111					FRMDET	Waits for receipt of 2 consecutive Frame Synch Words	Data Driven	S1
1000	FRMDET	Waits for receipt of 2 consecutive Frame Synch Words	Data Driven		Not present in Slave Mode			
0000	Active	Fully Active		S1	Active	Fully Active		S1

1. S0 = Two level (±3) signal
2. S1 = Four level (±3, ±1) signal
3. See Table 7 for the source of the S0 and S1 signals. The source of the signals is mode dependent.

4.4.2 Normal Operation

Both Data Pumps should be in the IDLE state prior to the start of an activation sequence. Activation always begins at the Master with the assertion of ACTREQ. The Master sends the S0 signal, and presets its AGC (pre-AGC sub-state) and Echo-Canceler (EC) (pre-EC sub-state)

circuits based on its own transmitted signal. The Master moves between states based on its MAT. When the Master timer has passed SMT2, it enters the SIGDET sub-state where it remains until detection of an S0 signal from the Slave.

If Master and Slave are connected and the Slave is in the Inactive state, the Slave detects the S0 signal from the Master, and starts its MAT. The Slave enters the Wait sub-state, and begins training its AGC. The Slave does not transmit any signal until MAT exceeds SMT2. At that time, the Slave transmits an S0 signal and enters the EC sub-state where the Echo canceler and the Digital AGC are trained.

The Master detects the S0 signal from the Slave, and resets the MAT to SMT2+1. This re-synchronization process assures that Master and Slave state machines will be synchronized for the remainder of the activation process. In most activation, attempts where the Slave is connected to the line and is in the Inactive state at the beginning of the activation attempt, the Slave will begin to transmit S0 just as the Master gets to the SIGDET state and the change in the Master MAT will be minimal. If the Slave is reset or connected to the line sometime after the activation sequence has begun at the Master, the Master will remain in the SIGDET state until S0 is received or the MAT expires. If S0 is received after the Master has been in SIGDET for some time, the change in the setting of the MAT at the Master may be significant. This change in the Master reference timer, which is referred to as TDELTA in Figure 20 and Figure 21, allows the substates of the Master and Slave Data Pumps to be synchronized for the remainder of the activation sequence.

The Master and Slave Data Pumps continue through the activation process as shown in Figure 20 and Figure 21. Both Data Pumps complete training of all the receiver components which can be trained with a two-level (S0) signal relying on system timers SMT2, SMT3, SMT4, and SMT5 to maintain synchronization between the Master and Slave.

After the SMT5 timers have expired, progression through the remainder of the activation states is data driven, that is, it relies on receipt of a particular signal from the other end to move to the next sub-state. The Slave enters the 4LVLDET sub-state and waits for receipt of a four level (S1) signal from the Master. On receipt of this signal the Slave completes training of the DFE and 4 level slicer then begins to transmit an S1 signal. The Master detects the S1 signal from the Slave and then completes training of the DFE and 4 level slicer.

The EDSP also allows the designer to specify the length of time the Data Pump spends in each of the activating substates. The default times have been optimized for best performance at either 784 kbps or 1168 kbps in the framed modes (modes 7 and 6). Reliable operation has been demonstrated using the default values at all data rates between 272 kbps and 1168 kbps in unframed modes using the default timing. Overall activation time can be reduced for certain applications by reducing the activation times of the individual states. Table 9 gives the information required to select timer values for each of the activating substates. After settings for each of the individual sub-state timers has been optimized, the Master Activation Timer may be optimized to minimize the time required between sequential activation attempts.

4.4.3 Transition to the Active State

The actions following detection of the S1 signal vary depending on the operating mode of the system. The following sections describe the operation in both modes.

Unframed Signal (Modes 0,1,2,4,5)

Both Master and Slave move directly to the Active state on completion of the 4LVLDET training functions. The devices remain in the Active state even after MAT expires. Received data are available, and the $\overline{\text{ACTIVE}}$ indicator is asserted Active state.

Framed Signal (Modes 6,7)

Both Master and Slave move directly to the FRAMEDET sub-state on completion of the 4LVLDET training functions. The devices begin executing their internal algorithm to search for the FSW. As soon as the FSW is detected in the appropriate place in two consecutive frames, the device moves to the Active1 state. The devices remain in the Active1 state until the MAT expires, then move to the Active2 state. Received data are available, and the $\overline{\text{ACTIVE}}$ indicator is asserted in both the Active1 and Active2 states. The only difference between the Active1 and Active2 states is the status of the MAT.

The EMDP provides a mean for abnormal termination of the activation process. Expiration of the MAT will cause immediate termination of the activation process. When MAT expires, the EMDP moves directly to the Deactivated state.

Table 10 illustrates the management of the MAT. WR3[5:6] is used to program the MATC. The programmed value of MATC, as described in Table 17 is used to calculate the MAT as follows:

MAT = MATC*FL*T

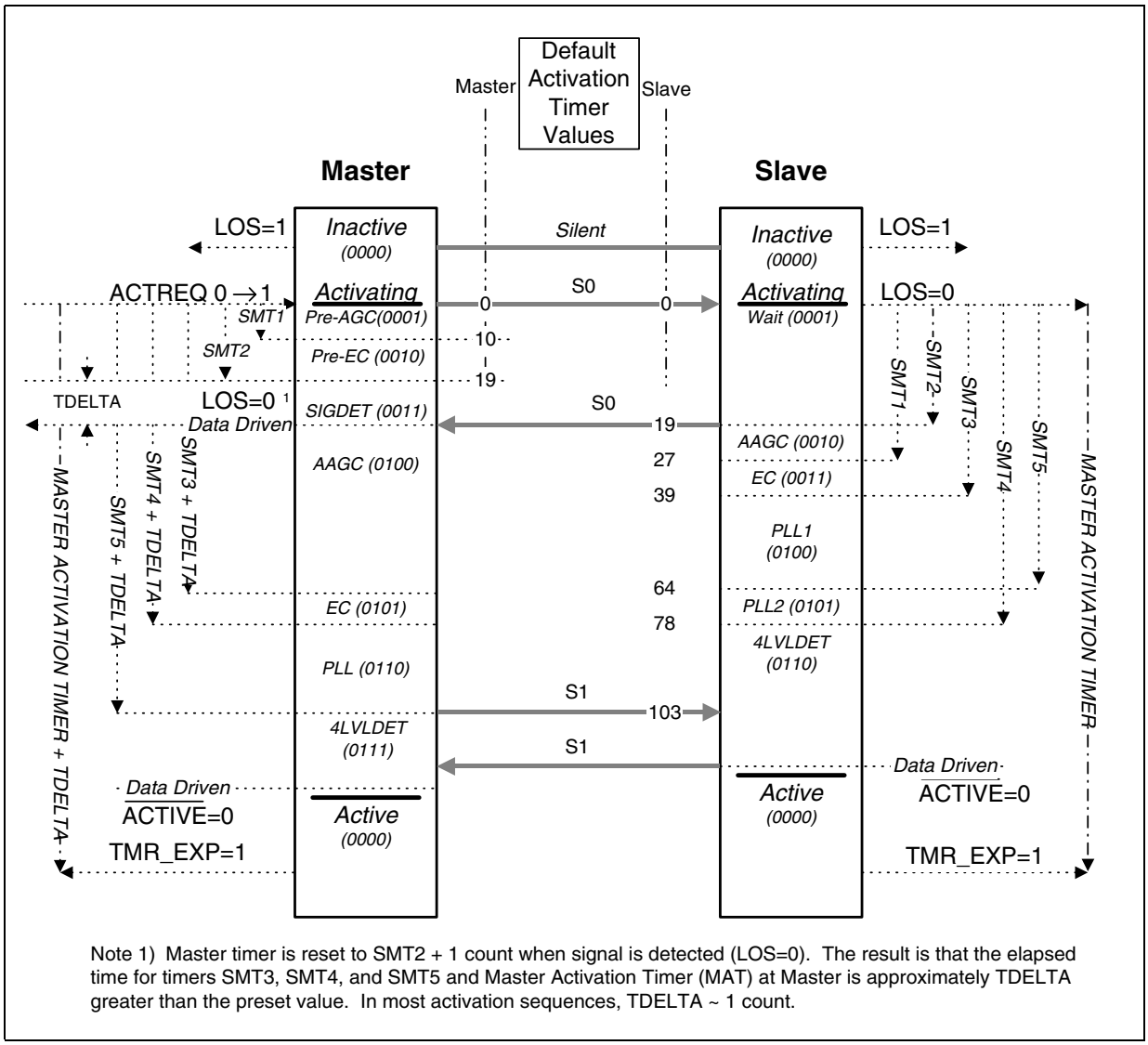
Where:

MATC = Number from Table 17
FL = 4704 bits for operating modes 0, 1, 2, 4, 5,& 7; 7008 for operating mode 6.
T = Length of the period of the bit clock

If MAT expires, or signal is lost before the Active1 state is reached, the EMDP moves directly to the Deactivated state and ceases transmission. The Master remains in the Deactivated state until the LOS timer has expired (Table 11). The Slave transitions to the Inactive state as soon as the presence of signal on the line is no longer detected.

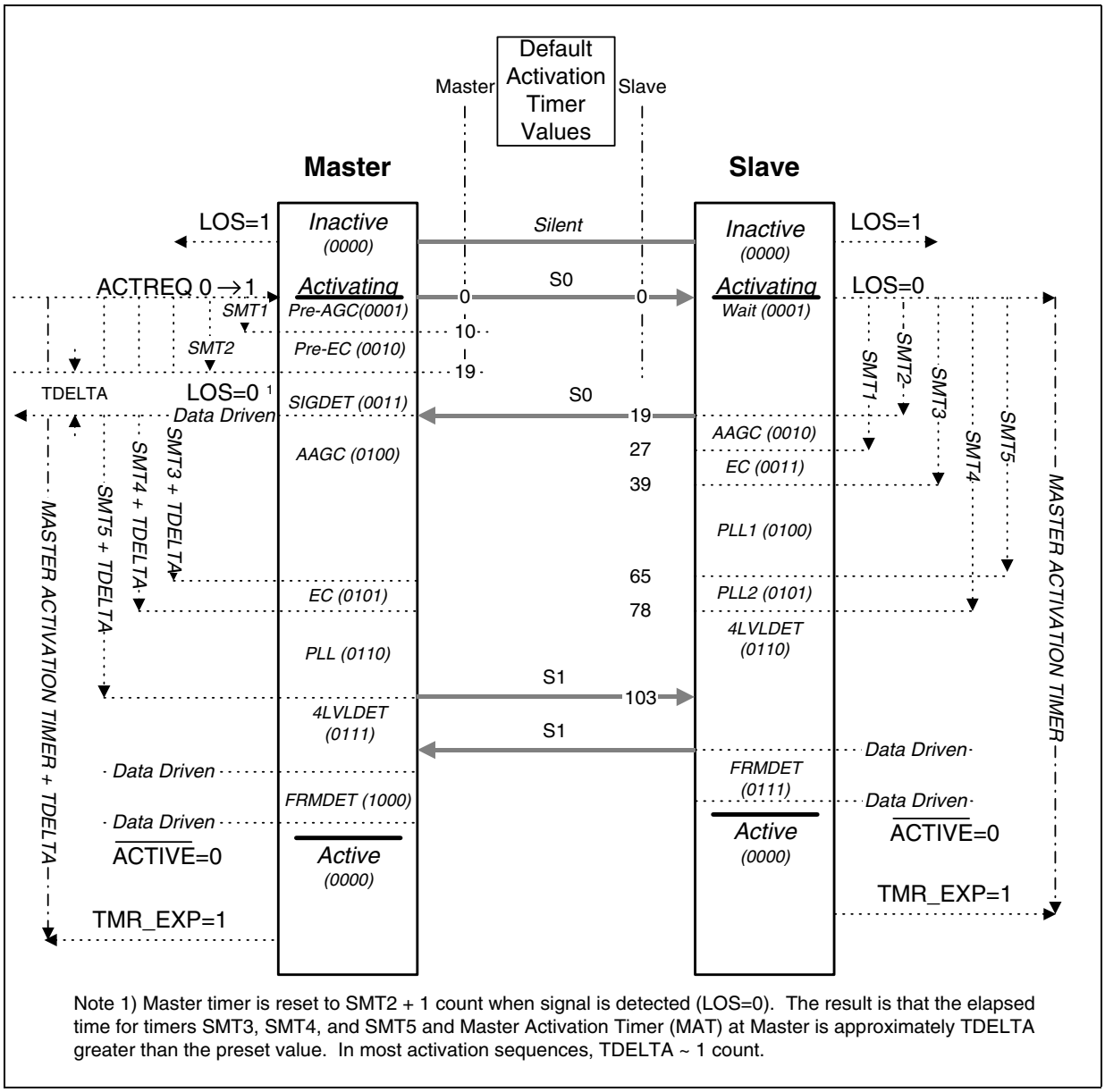
In framed modes frame synchronization may be lost during a signal interruption. If this occurs, the EDSP will begin the frame re-synchronization process, as described in the next section.

Figure 20. MDSL Activating State Detail - Unframed Modes 0,1,2,4, and 5



Note 1) Master timer is reset to SMT2 + 1 count when signal is detected (LOS=0). The result is that the elapsed time for timers SMT3, SMT4, and SMT5 and Master Activation Timer (MAT) at Master is approximately TDELTA greater than the preset value. In most activation sequences, TDELTA ~ 1 count.

Figure 21. MDSL Activating State Detail - Framed Modes 6 and 7



Note 1) Master timer is reset to SMT2 + 1 count when signal is detected (LOS=0). The result is that the elapsed time for timers SMT3, SMT4, and SMT5 and Master Activation Timer (MAT) at Master is approximately TDELTA greater than the preset value. In most activation sequences, TDELTA ~ 1 count.

Table 9. Activating Sub-state Timers

Timer	Default Count (Decimal)	Default Timer Values (seconds) vs. Data Rate Operating Modes 0 through 5 and 7						Mode 6 Only
	Data Rate	272	400	520	656	784	1168	1168
Master								
SMT1	10	2.8	1.9	1.5	1.1	1.0	0.6	1.0
SMT2	19	5.3	3.6	2.8	2.2	1.8	1.2	1.8
SMT3	65	18.0	12.2	9.6	7.5	6.2	4.2	6.2
SMT4	78	21.6	14.7	11.5	8.9	7.5	5.0	7.5
SMT5	103	28.5	19.4	15.1	11.8	9.9	6.6	9.9
Slave								
SMT1	27	7.5	5.1	4.0	3.1	2.6	1.7	2.6
SMT2	19	5.3	3.6	2.8	2.2	1.8	1.2	1.8
SMT3	39	10.8	7.3	5.7	4.5	3.7	2.5	3.7
SMT4	78	21.6	14.7	11.5	8.9	7.5	5.0	7.5
SMT5	64	17.7	12.0	9.4	7.3	6.1	4.1	6.1
Increment	1	0.28	0.19	0.15	0.11	0.10	0.06	0.10

Table 10. Master Activation Timer Examples

Bits WR3 [6:5]	Data Mode	MATC	Frame Length	Line Rate (kbps)	Bit Clock Period	MAT (Seconds)
00	0:5,7	5000	4704	784	1.275 us	30
01	0:5,7	2500	4704	784	1.275 us	15
10	0:5,7	1667	4704	784	1.275 us	10
reserved	-	-	-	-	-	-
00	0:5,7	5000	4704	1168	0.856 us	20
00	6	5000	7008	1168	0.856 us	30
00	0:5,7	5000	4704	272	3.676 us	86.5
reserved	-	-	-	-	-	-

Table 11. State Machine Default Timer Durations (Figure 18 and Figure 19)

Timer	Default[1] Timer Duration (seconds)						Description
	272 kbps	400 kbps	528 kbps	784 kbps	1168 kbps (framed)	1168 kbps (unframed)	
MAT[2]	86.5	59.0	44.5	30.0	30.0	20.0	**Master Mode**: Starts with an activation request. Reset for synchronization when a signal from the Slave is detected. **Slave Mode**: Starts when a signal from the Master is detected.
Deactivation Timer[3,4]	6.0	4.0	3.0	2.0	2.0	1.3	Starts when the EDSP enters the Pending Deactivation state due to Loss of Synchronization Word for 6 consecutive frames. Occurs only in framed modes 6 and 7.
LOS Timer[5]	3.0	2.0	1.5	1.0	1.0	0.7	**Master Mode Only**: Starts in Deactivated state when signal from the Slave is no longer detected. Set to 0 whenever signal from the Slave is detected. Restarts when signal is no longer detected.

1. See Table 10 and Table 17 for information on changing the MAT from its default values.
2. If time elapses and Data Pump has not moved to Active1 state, the Data Pump enters the Deactivated state.
3. Pending Deactivation can be reached from either Active1 or Active2 states in framed modes 6 and 7.
4. If synchronization word detection does not occur before time elapses, the Data Pump moves to the Deactivated state.
5. When the Data Pump fails to activate, there is no waiting period in the Deactivated state; the Data Pump immediately goes to the Inactive state.

4.4.4 Frame Synchronization

Figure 22 shows the EMDP Synchronization State Machine. Table 12 shows the correspondence between the Synchronization states and Activation states. The same Synchronization states are used in both the Master and Slave Data Pumps, but only when the EMDP is operating in the framed modes 6 and 7.

Starting at the initial Out-of-Sync condition (State 6), the device progresses through State 7 until two consecutive FSW are detected and then Synchronization is declared in State 0.

Table 12. Activation and Synchronization

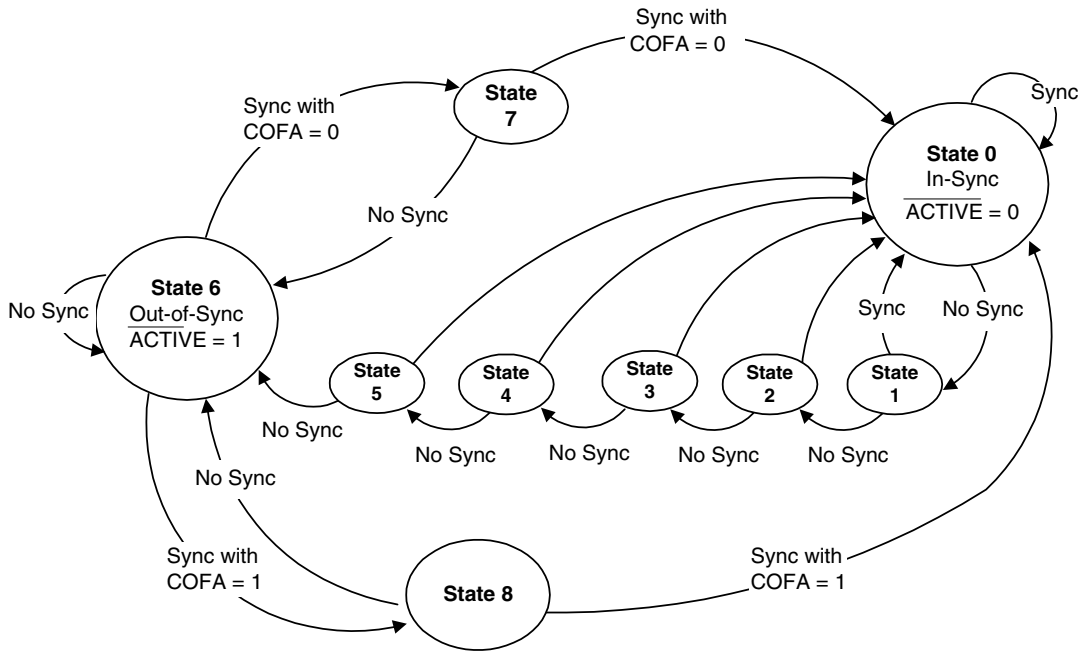
Activation State	Synchronization States
Active	States 0, 1, 2, 3, 4, and 5
Pending Deactivation	States 6

Once the In-Sync condition is achieved, failure to detect an FSW causes the EMDP to move to State 1. Each subsequent failure to detect an FSW at the appropriate time advances the state machine one step through States 1 to 5. If an FSW is detected at any time before State 6 is reached the EMDP goes directly back to State 0. An Out-of-Sync condition is declared in State 6, which is reached when no FSW is detected for six consecutive frames. As soon as State 6 of the synchronization state machine is reached the EMDP goes to the Pending Deactivation state of the Activation state machine and activates the Deactivation Timer described in Table 11.

If the deactivation timer expires without re-establishing frame synchronization, the Activation State Machine progresses to Deactivated state.
synchronization state returns to State 0.

If frame synchronization is re-established before the deactivation timer expires, the EDSP will return to the In-Sync condition (State 0) through State 7 if two consecutive frames are received without any change of frame alignment (COFA = 0). If a change of frame alignment does occur (COFA = 1), two consecutive matches are required to move through State 8 back to State 0.

Figure 22. MDSL Synchronization State Machine



NOTES:
1. "Sync" = Frame synchronization word match.
2. "No Sync" = Frame synchronization word mismatch.
3. Upon entering Stage 6, ACTIVE is set to 1 and Deactivation timer starts.
4. State 0 corresponds to Active-1 and Active-2 states as shown in Figure 19.
5. State 6 corresponds to Pending deactivated state as shown in Figure 19.
6. This state machine applies to 4-level signals in Framed modes 6 and 7 only.
7. COFA: Change of Frame Alignment.

4.5 Deactivation

The EDSP may be deactivated by using control signals to stop transmission on the loop or by the expiration of MAT. This section describes method of deactivation.

"Normal" Deactivation takes place when the QUIET control is asserted. QUIET may be asserted using an input signal in hardware control mode or by setting a register bit (WR0:B1) in Software control mode. Deactivation may be initiated at either the Master or the Slave Data Pump.

When QUIET is asserted the Data Pump moves from the present state directly to the Deactivated state. In this state no signal is transmitted. A Slave Data Pump stays in the deactivated state until there is no received signal (LOS=1). A Master Data Pump remains in the Deactivated state until it detects that no signal is being received from the Slave. The Master then starts its LOS timer (Table 11). When the LOS timer expires the Data Pump moves to the Inactive state. If a received signal is

detected while the LOS timer is active, the LOS timer is reset and starts from zero when absence of signal is again detected. The delay before moving to the Inactive state ensures that the line has been quiet at the Master for a reasonable length of time before a new activation attempt occurs.

4.6 Special Features

4.6.1 Micro-Interruption

The EMDP incorporates a transient interruption protection process that provides protection against short interruptions of the received signal.

The EDSP monitors the received SNR on every baud. Whenever the noise margin drops below -6 dB, the EDSP freezes all the adaptive coefficients, moves to the Time-out state and starts the Micro-interruption Timer (MIT). If the noise margin rises above -3 dB while in the Time-out state the EDSP returns to the state from which it entered Time-out. The EDSP then allows the coefficients to begin adapting again and begins to realign the phase of the local clock with the phase of the received signal. If the received SNR does not increase above the -3 dB threshold before MIT expires, the EDSP goes directly to the Deactivated state. Once in the Deactivated state, transition to the Inactive state occurs in the manner described above in the section on Deactivation.

ETSI ETR-152 and ITU G.991.1 specifies the micro-interruption feature (Figure 23). This test is specifically intended to simulate momentary open circuits caused by problems with splices in twisted pair wires. In practice, DSL system problems are often due to other causes such as momentary shorts on the line or nearby lightning strikes which may last much longer than the ETSI specified line interruptions. Systems manufactured using the EDSP will meet the ETSI requirement. Since the signal may be lost for many reasons and since the line conditions may change after an interruption it is not possible to guarantee restoration of service when the cause of the problem is removed. In addition, the phase relationship of the Master and Slave clocks will drift during the interruption, so it is necessary to reacquire the phase of the received signal at the end of the interruption.

The EMDP stays in the Time-out state until the MIT expires. The MIT functions by counting baud periods until the maximum value of 255 is exceeded.

For example: When operating at 784 kbps, the length of one baud is 2.55 µsec for 2048 periods. Therefore the time of interruption at 784 kbps is 2.55 x 2048 x 255 = approximately 1.33 seconds. It is important to note that this does not ensure that the EMDP will be able to recover timing and resume operation after an interruption of that duration.

Figure 23. Micro-interruption as Defined in ETR-152

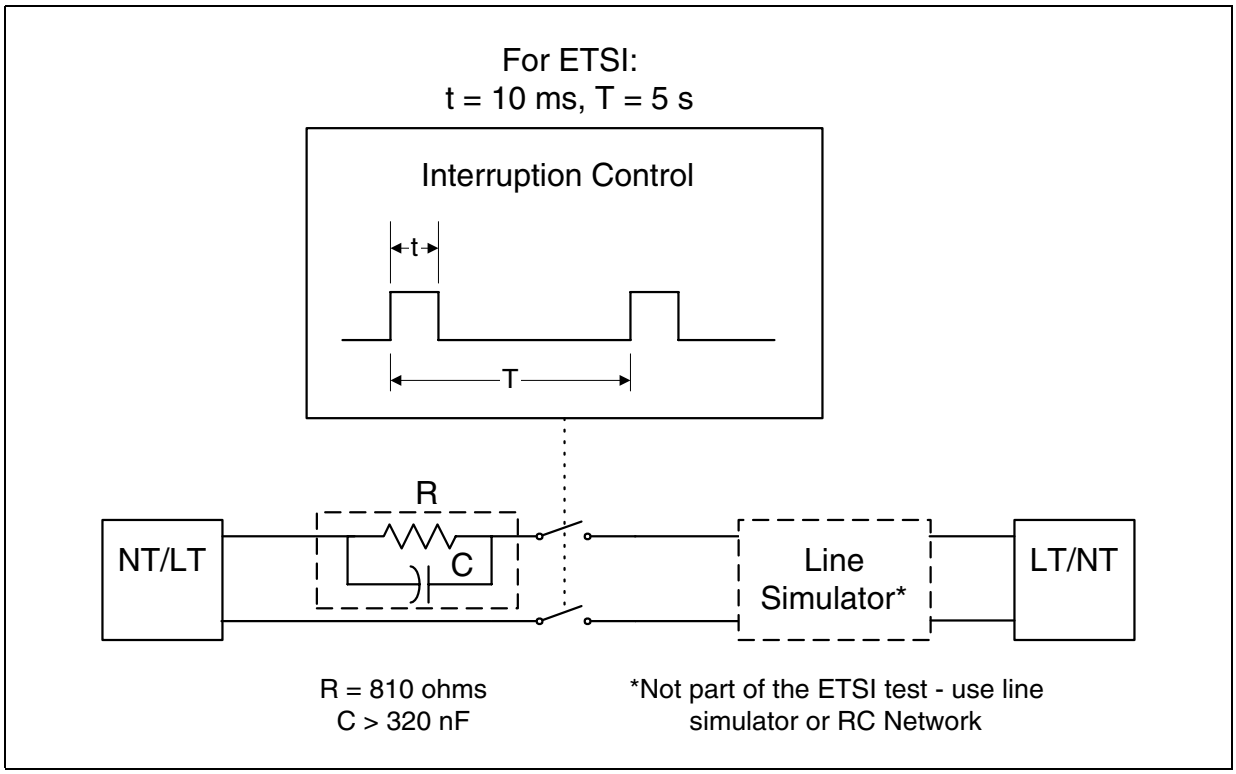


Table 13. MIT Register Setting Example

Line Rate (kbps)	Baud Period (µsec)	Maximum Micro-interruption Time (seconds)
272	7.35	3.84
400	5.00	2.61
528	3.78	1.97
784	2.55	1.33
1,168	1.71	0.89

4.6.2 Loopbacks

The EMDP chip set provides analog and digital loopbacks for system diagnostic purposes. The analog Front End Loopback (FELB) loops the transmitted analog signal back towards the digital interface, while the digital Back End Loop Back (BELB) loops the signal back toward the DSL loop.

In FELB the IAFE receiver input is disabled while the balance network input remains active. The line driver output is normally coupled back into the balance input through external components, looping the transmitted data (TDATA plus any framing signal) back into the receiver and eventually back to RDATA. In FELB the Data Pump receiver activates with its own transmit data and ignores any signal present at the IAFE receiver. Data is transmitted on the line during FELB.

The far end (Slave) Data Pump may activate in response to the signal transmitted from the unit under test. FELB is available only at the Master Data Pump. FELB is initiated only from the Inactive state by asserting the FELB and the ACTREQ signals.

BELB is a data loopback inside the EDSP. Data received by the IAFE is processed through the EDSP and then retransmitted on the DSL loop. BELB is available in both Master and Slave mode at any time the Data Pump is Active. In BELB, the received data and framing signals are supplied to the transmitter which ignores the TDATA and TFP inputs. Receive Data is also available on RDATA during BELB. BELB is initiated by asserting BELB control. Figure 24 shows both the FELB and BELB Loopbacks.

Note: BELB is only available in Framed modes (i.e. modes 6 and 7). During BELB in modes 0, 1, 2, 4 and 5, it is not possible to read the registers; i.e. write only.

4.6.3 TIP/RING Reversal

DSL systems are designed to have the tip and ring leads connected directly, tip at the Master connected to tip at the Slave and ring at the Master connected to the ring at the Slave. In some installations the connection may be reversed, with tip connected to ring and vice versa. If this condition is not detected and corrected, the receiver will improperly sense the sign of the received signal. The EDSP automatically detects and corrects this condition in framed mode by sensing the polarity of the framing signal and performing appropriate corrections.

In Transparent and Independent modes the EDSP is unable to detect the condition of the connection from the received signal since no framing signal is defined. The EDSP allows the application to invert the sense of the received signal by setting bit 7 in the Interrupt Mask and Line Reversal Register (WR2). Table 16 describes the use of this register.

4.6.4 Loop Loss and SNR

In software control mode, EMDP provides information to compute approximate loop loss and SNR. The approximate loop loss (LL) can be calculated as follows:

$LL = 20*\log_{10}(DAGC * AGC\ tap) + AAGC + k\ dB.$

Where:

k = 24 dB if 6 dB receiver gain is disabled.
k = 30 dB if 6 dB receiver gain is enabled.

The value of DAGC and AAGC are calculated as shown in the description of register RD6. See Table 26.

The value of AGC tap is calculated as shown in the description of register RD1. See Table 22.

The signal levels inside the EDSP are dependent on both the line attenuation, and the circuit components outside the EMDP chip set. System manufacturers should calibrate the line attenuation reading using a null loop and other test arrangements with known attenuation and introduce a correction factor (modify k) appropriate for each system implementation. Note that the EDSP relies most heavily on peak pulse amplitude attenuation in performing this calculation. This attenuation is not the same as the attenuation measured at any particular frequency. In most applications and on most loops, attenuation measurements at 20% of the bit rate (157 kHz for a 784 kbps line rate) give a good approximation of the pulse attenuation.

The SNR is computed as follows:

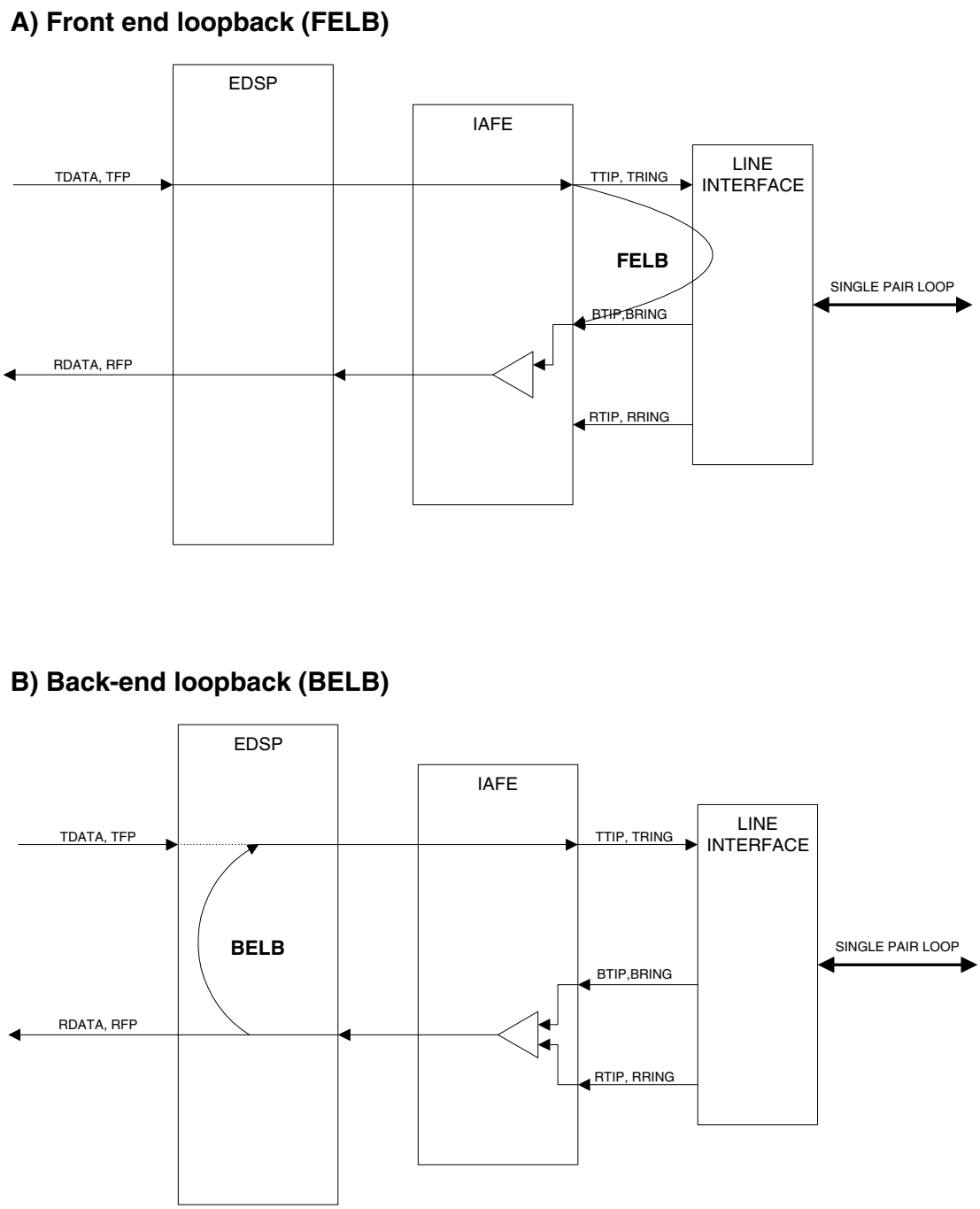
SNR = Noise Margin + 21.5 dB; when WR9 is set to 00h, indicating that receiver gain is set to 0 dB (default).

SNR = Noise Margin + 15.5 dB; when WR9 is set to 0Fh, indicating that receiver gain is set to 6 dB.

Error propagation in the DFE and descrambler may introduce some fractional errors in this formula. The relationship between the SNR and the noise margin remains valid as long as the noise is White Gaussian noise.

Since the period of the noise margin calculation is very short (64 bauds), it is recommended that 1000 samples be averaged for evaluating the operating SNR.

Figure 24. Loopbacks



Note: FELB is also known as local loopback and BELB is also known as remote loopback.

5.0 Register Definitions

The EDSP provides access to various internal registers via microprocessor interface. Ten write registers and seven read registers are available in the EDSP. Several new registers are added in comparison to previous MDSP chips enabling a more programmable and powerful EDSP. Table 14 provides a summary of the EDSP registers.

Some of the registers contain *reserved* bits. Software must deal correctly with reserved fields. During reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. In some cases, software must set reserved bits to a particular value. If necessary, the required value is specified in the individual bit descriptions. After assertion of the RESET signal, the Data Pump initializes its registers to the default values.

Table 14. Register Summary

ADDR	Write Registers			Read Registers		
A3-A0	WR#	Name	Table	RD#	Name	Table
0000	WR0	Main Control	Table 15	RD0	Main Status	Table 21
0001		*reserved*	*n/a*	RD1	AGC Tap Value	Table 22
0010	WR2	Interrupt Mask and Line Reversal	Table 16	RD2	Noise Margin	Table 23
0011	WR3	Coefficient Select and Activation Timer	Table 18	RD3	Coefficient Read Register (lower byte)	Table 24
0100		*reserved*	*n/a*	RD4	Coefficient Read Register (upper byte)	Table 24
0101		*reserved*	*n/a*	RD5	Activation Status	Table 25
0110		*reserved*	*n/a*	RD6	Receiver AGC and FFE Step Gain	Table 26
0111-1000		*reserved*	*n/a*		*reserved*	*n/a*
1001	WR9	Receiver Gain Control	Table 19		*reserved*	*n/a*
1010	WR10	SMT1	Table 20		*reserved*	*n/a*
1011	WR11	SMT2	Table 20		*reserved*	*n/a*
1100	WR12	SMT3	Table 20		*reserved*	*n/a*
1101	WR13	SMT4	Table 20		*reserved*	*n/a*
1110	WR14	SMT5	Table 20		*reserved*	*n/a*
1111	WR15	*reserved*	n/a		*reserved*	*n/a*

5.1 WR0—Main Control Register

Address: A<3:0> = 0000
Default: 00h
Attributes: Write Only.

Main Control Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware Mode. Table 15 lists bit assignments for the WR0 register.

Table 15. Main Control Register (WR0)

Bit	Description
B7	**Transmit Test Pulse Enable (TXTST).** Set TXTST to 1 to transmit isolated pulses. TDATA controls the sign and TFP controls the magnitude of the transmitted pulses according to the 2B1Q encoding rules described in Table 3. The TXTST function is available only in framed modes 6 and 7. In framed mode 6 the pulses are transmitted every 7008 BIT_CLK cycles, corresponding to the ETSI framing sequence. In framed mode 7 the pulses are transmitted every 4704 BIT_CLK cycles. TXTST is available only in the Inactive state of the Data Pump.
B6	**Back-End Loop Back (BELB).** In Active state, set BELB to 1 to enable an internal back-end loopback. RDATA and RFP outputs are used in place of the TDATA and TFP inputs, respectively. TDATA and TFP signals from the external interface are ignored.
B5	**Front End Loop Back (FELB).** In the Master mode, with the Data Pump in Inactive state, set FELB to 1 to enable an IAFE front-end loopback. Upon setting ACTREQ bit to 1, the Data Pump will begin activation using its own signals received at the BTIP and BRING inputs. Proper operation in this mode is dependent on the configuration of external line interface circuit components.
B4	**Repeater Mode (RPTR).** In Master mode, set RPTR bit to 1 to program the Data Pump to operate in repeater mode. This ensures that the phase of BIT_CLK is aligned with the TFP pulse. Note that to configure two Data Pumps to operate as a repeater, MASTER_CLK output from Slave Data Pump is connected to MASTER_CLK input of adjacent Master Data Pump. RFP of the Slave Data Pump is connected to TFP input of Master Data Pump. In Slave mode, RPTR bit has no function and can be set to either 0 or 1. This feature is available only in operating mode 6 and 7.
B3	**Loop Number (LOOPID).** LOOPID is set at the Master end of the loop and selects the frame sync word format to encode the loop number. Set LOOPID=0 for loop number 1 to transmit sync word quats as +3,+3, +3,-3,-3,+3,-3 in accordance with ANSI and ETSI standards. Set LOOPID=1 for loop number 2 to transmit time reversed sync word quats as -3,+3,-3,-3,+3,+3,+3 in accordance with ANSI standard. LOOPID must be set before the Master is activated. This control bit is functional only at the Master Data Pump. The Slave sets its transmitted LOOPID equal to the received LOOPID. In Slave mode this bit has no function and may be set to 0 or 1. LOOPID is provided only when operating in framed modes 6 or 7.
B2	**Insertion Loss Measurement Test (ILMT).** Set ILMT to 1 to transmit a scrambled all ones test pattern. In operating mode 6 and 7 the signals transmitted are framed with valid sync word, whereas in the rest of the operating modes signals transmitted are unframed without any sync word. If the loop is connected to a Slave Data Pump then it may begin activating.
B1	**Quiet Mode (QUIET).** Set QUIET to 1 to force the Data Pump into the Deactivated state thus disabling the transmitter. When this bit goes from 1 to 0, the Master Data Pump will remain in the Inactive state. Neither Data Pump can begin the activation process when QUIET is asserted.
B0	**Activation Request (ACTREQ).** In the Master mode when the Data Pump is in the Inactive state and Quiet is set to 0, set ACTREQ to 1 to initiate an activation sequence. If an activation attempt fails, another activation attempt will begin immediately after the expiration of the Master Activation Timer unless ACTREQ has been set to 0. In Slave mode, this bit has no function and should be set to 0.

5.2 WR2—Interrupt Mask and TIP/RING Reversal Register

Address: A<3:0> = 0010
Default: 00h
Attributes: Write Only.

Table 16 shows the interrupt masks and TIP/RING reversal control provided in register WR2.

Table 16. Interrupt Mask and Line Reversal Control Register (WR2)

Bit	Description
B7	**TRREV.** TIP/RING reversal control. Set to 1 to invert the polarity of the received signal.
B6	**Reserved.** Must be set to 0.
B5	**LOSMSK.** Interrupt mask for the LOS condition. 1=Masked (Interrupt Disabled).
B4	**DEACTMSK.** Interrupt mask for the DEACTVTD condition 1=Masked (Interrupt Disabled).
B3	**ACTBMSK.** Interrupt mask for the $\overline{\text{ACTIVE}}$ condition. 1=Masked (Interrupt Disabled).
B2	**ACTMSK.** Interrupt mask for the TMR_EXP condition and the ACTIVE condition. 1=Masked (Interrupt Disabled).
B1	**Reserved.** Must be set to 0.
B0	**Enable coefficient read register (CRD1).** 1=Enable. 0=Disable. Used in conjunction with WR3, RD3, and RD4 for reading coefficient values.

5.3 WR3—Coefficient Select and Master Activation Timer Register

Address: A<3:0> = 0011

Default 00h

Attributes: Write Only.

This register serves two unrelated functions. Bits 5 and 6 are used to program the Master Activation Timer Constant (MATC) and bits 0-4 are used to select the internal coefficient register. Table 17 and Table 18 describe both of these functions.

Table 17. Master Activation Timer Constant (MATC) (WR3)

Bit	Description
B7	**Reserved.** Must be set to 0
B6:B5	**Master Activation Timer Constant Value:** 00 = 5000 01 = 2500 10 = 1667 11 = reserved

Table 18. Coefficient Select Functions of Register (WR3)

B4:B0 (hex)	Register Selected	Description
00-07	DFE1-DFE8	DFE coefficients 1-8
08-0F	EC1-EC8	Echo Canceller coefficients 1-8
10-15	FFE1-FFE6	FFE coefficients 1-6
16-19	reserved	
1A	AGC Tap	AGC Tap
1B:1F	reserved	

5.4 WR9—Gain Control Register

Address: A<3:0> = 1001
Default: 00h
Attributes: Write Only.

The EMDP has improved performance on loops with low noise. If it is desired to take full advantage of this improved performance capability, set register WR9 to 0Fh after reset and before activation.

Table 19. Gain Control Register (WR9)

Bit	Description
B7:B4	**Reserved.** Must be set to 0.
B3:B0	**Receiver Gain Control.** Set all 4 bits to 1 to increase the receiver gain by 6 dB.

5.5 WR10-WR14—Activation Sub-State Timer Registers

Address: A<3:0> = 1010 through 1110
Default: As shown in Table 20
Attributes: Write Only.

The EMDP allows the user to program each of the timers in the activation state machine. This capability allows the user to optimize the timers for operation at various data rates in a particular application. Table 20 describes the activation sub-state timer registers.

Table 20. Activation Sub-State Timer Registers

Register Address A3-A0	Timer Name	Default Value in Hex (Decimal)		State Ended on Expiration	
		Master	Slave	Master	Slave
1010	SMT1	0A(10)	1B(27)	Pre-AGC	Wait
1011	SMT2	13(19)	13(19)	Pre-EC	AAGC
1100	SMT3	41(65)	27(39)	AAGC	EC
1101	SMT4	4E(78)	4E(78)	EC	PLL2
1110	SMT5	67(103)	40(64)	PLL	PLL1
NOTE: See Figure 20 and Figure 21 for the definition of these state transitions.					

5.6 RD0—Main Status Register

Address: A<3:0> = 0000
Default: xxh (x=undefined)
Attributes: Read Only.

Status Register bits serve the same purpose in Software Mode as the like-named individual pins in Hardware mode. Table 21 lists the bit assignments in this register.

Table 21. Main Status Register (RD0)

Bit	Status Bit Descriptions
B7	**Timer Expiration (TMR_EXP).** Set to 1by EDSP to indicate expiration of the Master Activation Timer. • Causes interrupt on changing from 0 to 1; masked by setting ACTMSK = 1 in register WR2 • Latched event; reset on read, with persistence while in the Active state
B6	**TIP/RING polarity reversal ($\overline{\text{INVERT}}$).** Set to 0 by EDSP to indicate reversal of Tip and Ring signal polarity at the receiver. Valid only in Active1 or Active2 states and only in framed modes 6 and 7.
B5	**Change of Frame Alignment (COFA).** Indicates that re-acquisition of frame synchronization is in a different position with respect to the last frame position. Does not cause interrupt. Latched event; reset on read.
B4	**Loss Of Signal (LOS).** Set to 1 by EDSP to indicate that Data Pump has entered into Inactive state. • Causes interrupt on transitions from 0 to 1 or 1 to 0; masked by setting LOSMSK = 1 in register WR2 • LOS is not a latched event. EDSP continuously updates the status
B3	**Loop Number Indicator (LOOPID).** Set to 0 or 1 by EDSP to indicate loop number 1 or number 2 respectively. Valid only in Active states, 0 in all others. LOOPID is set at the Master end of the loop and selects the frame synchronization word format to encode the loop number. This bit indicates the format of the received frame synchronization word at both the Master and the Slave. The LOOPID function is supported only in framed modes 6 and 7.

Table 21. Main Status Register (RD0) (Continued)

Bit	Status Bit Descriptions
B2	**Deactivation Indicator (DEACTVTD).** Set to 1 by EDSP to indicate expiration of the Deactivation timer and the transition from the Pending Deactivation state to the Deactivated state. • Causes interrupt on changing from 0 to 1; masked by setting DEACTMSK = 1 in register WR2 • Latched event; reset on read; with persistence while in the Deactivated state
B1	**Link Active Indicator, ($\overline{\text{ACTIVE}}$), active Low.** Set to 1 by EDSP upon entering into the Pending Deactivation state, or tome-out state. • Causes interrupt on changing from 0 to 1; masked by setting ACTBMSK = 1 in register WR2 • Latched event; reset on read; with persistence while in the Pending Deactivation state
B0	**Link Active Indicator, (ACTIVE), active High.** Set to 1 by EDSP upon completion of activation process and entering into the Active state. • Causes interrupt on changing from 0 to 1; masked by setting ACTMSK = 1 in register WR2 • Latched event; reset on read with persistence if still in Active state

5.7 RD1—AGC Tap Value Register

Address: A<3:0> = 0001
Default: xxh (x=undefined)
Attributes: Read Only.

This register contains the eight most significant bits of the main FFE AGC tap. B7 is the sign bit and is always equal 0. B0 the least significant bit.

The AGC Tap value can be used to calculate approximate Loop Loss (LL) as described in "Loop Loss and SNR" on page 54.The AGC tap value is determined as follows:

$$\text{AGC Tap} = \sum_{i=0}^{6} Bi*2^{i-6}$$

In this equation Bi is the bit value of register RD1. For example:

RD1 = 01100101 (65h)

AGC Tap = 1+0.5+0.0625+0.015625 = 1.578125.

Table 22. AGC Tap Value Register (RD1)

Bit	Description
B7:B0	**FFE AGC Tap Value** (eight most significant bits): B7 (Sign bit) always = 0 B6 (MSB) - Value: 1 B5 - Value: 0.5 (1/2) B4 - Value: 0.25 (1/4) B3 - Value: 0.125 (1/8) B2 - Value: 0.0625 (1/16) B1 - Value: 0.03125 (1/32) B0 (LSB) - Value: 0.015625 (1/64)

5.8 RD2—Noise Margin Register

Address: A<3:0> = 0010
Default: xxh (x=undefined)
Attributes: Read Only.

RD2 provides a calculated, logarithmic noise margin value which is used by the EMDP state machine. This coded noise margin value is according to ETSI ETR 152 recommendation. The noise margin value is always available, but it is recalculated and updated only every 64 baud. Table 23 shows the noise margin coding.

The indicated noise margin is affected by the setting of the Gain Control Register (WR9). If the receiver gain is increased by 6 dB, the indicated noise margin must be decreased by 6 dB.

Table 23. Noise Margin Register (RD2)

MSB							LSB	Coded Noise Margin[1,2]	MSB							LSB	Coded Noise Margin[1,2]
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	
0	0	1	1	0	1	0	1	+26.5	0	0	0	1	0	0	0	0	+8.0
0	0	1	0	1	1	1	1	+23.5	0	0	0	0	1	1	1	0	+7.0
0	0	1	0	1	0	1	1	+21.5	0	0	0	0	1	1	0	0	+6.0
0	0	1	0	1	0	0	1	+20.5	0	0	0	0	1	0	1	0	+5.0
0	0	1	0	0	1	1	1	+19.5	0	0	0	0	1	0	0	0	+4.0
0	0	1	0	0	1	0	1	+18.5	0	0	0	0	0	1	1	0	+3.0
0	0	1	0	0	1	0	0	+18.0	0	0	0	0	0	1	0	0	+2.0
0	0	1	0	0	0	1	0	+17.0	0	0	0	0	0	0	1	0	+1.0
0	0	1	0	0	0	0	0	+16.0	0	0	0	0	0	0	0	0	0.0
0	0	0	1	1	1	1	0	+15.0	1	1	1	1	1	1	1	0	-1.0
0	0	0	1	1	1	0	0	+14.0	1	1	1	1	1	1	0	0	-2.0
0	0	0	1	1	0	1	0	+13.0	1	1	1	1	1	0	1	0	-3.0

1. Accuracy of noise margin is ±1 dB.
2. Reduce indicated noise margin by 6 dB if receiver gain (Register WR9) is increased by 6 dB.

Table 23. Noise Margin Register (RD2) (Continued)

MSB							LSB	Coded Noise Margin[1,2]	MSB							LSB	Coded Noise Margin[1,2]
7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	
0	0	0	1	1	0	0	0	+12.0	1	1	1	1	1	0	0	0	-4.0
0	0	0	1	0	1	1	0	+11.0	1	1	1	1	0	1	1	0	-5.0
0	0	0	1	0	1	0	0	+10.0	1	1	1	1	0	1	0	0	-6.0
0	0	0	1	0	0	1	0	+9.0									

1. Accuracy of noise margin is ±1 dB.
2. Reduce indicated noise margin by 6 dB if receiver gain (Register WR9) is increased by 6 dB.

5.9 RD3 (LSB), RD4 (MSB)—Coefficient Read Register

Address: RD3<3:0> = 0011, RD4<3:0> = 0100

Default: xxh (x=undefined)

Attributes: Read Only.

RD3 and RD4 are used to read various internal coefficient registers. The address of a particular coefficient register to be read is first written in WR3, then RD3 and RD4 provide the content of that coefficient register. Each coefficient is a 16 bit word whose lower byte is read from RD3 and upper byte is read from RD4. The EDSP updates this word on each rising edge of the serial control frame strobe signal, SRCTL_FS.

Table 24. Coefficient Read Registers (RD3 and RD4)

Bit	Description
7:0	**Coefficient Word Value.** RD3 contains the lower byte; RD4 contains the upper byte.

5.10 RD5—Activating Status Register

Address: A<3:0> = 0101

Default: xxh (x=undefined)

Attributes: Read Only.

The ACT bits shown in Table 25 indicate the current state of the EMDP during the Activating state. (For any state other than the Activating state, the ACT bits will be “0000”.) The contents of the Activating status register may be used to monitor the progress of the training and activating sequence in the EMDP.

Table 25. Activating Status Register (RD5)

Bit	Description	
B7:B4	**Reserved**	
B3:B0	**Activating state in Master Mode**	**Activating state in Slave Mode**
0000	Inactive	Inactive
0001	Pre-AGC	Wait
0010	Pre-EC	AAGC
0011	SIGDET	EC
0100	AAGC	PLL1
0101	EC	PLL2
0110	PLL	4LVLDET
0111	4LVLDET	FRMDET[1]
1000	FRMDET[1]	n/a
0000	Active	Active
1. Available only in operating mode 6 and 7. In other operating modes this state is skipped.		

5.11 RD6— Receiver Gain and State Machine Register

Address: A<3:0> = 0110
Default: xxh (x=undefined)
Attributes: Read Only.

This 8-bit register holds the Analog AGC gain and FFE gain coefficients (AAGC and DAGC, respectively). AAGC is the analog AGC from the IAFE, and DAGC is the Digital AGC in the EDSP. Bit assignments are listed in Table 26.

Bits ST0-ST2 indicate the current state of EMDP in the activation state machine as described in Table 27. Refer to "Activation" on page 39 for further details.

Table 26. Activation State, Receiver AGC and FFE Step Gain Register (RD6)

Bit	Description
B7	**ST2.** Data Pump Activation State Indicator bit 2. Refer to Table Table 27.
B6	**ST1.** Data Pump Activation State Indicator bit 1. Refer to Table Table 27.

Table 26. Activation State, Receiver AGC and FFE Step Gain Register (RD6) (Continued)

Bit	Description
B5:B4	**DAGC1, DAGC0.** Digital Gain Word–bit 1 and Digital Gain Word–bit 0. 00 = 2^0 = 1 → 0 dB 01 = 2^1 = 2 → 6 dB 10 = 2^2 = 4 → 12 dB 11 = 2^3 = 8 → 18 dB
B3	**ST0.** Data Pump Activation State Indicator bit 0. Refer to Table Table 27.
B2:B0	**AAGC2-AAGC0.** Analog Gain Word–bit 2,1 and 0. 000 = -12 dB 001 = -10 dB 010 = -8 dB 011 = -6 dB 100 = -4 dB 101 = -2 dB 110 = 0 dB 111 = +2 dB

Table 27. Data Pump Activation State

ST2	ST1	ST0	Description
0	0	0	Inactive state
0	0	1	Activating state
0	1	0	Active state - Master Activation Timer running (Active1)[1]
0	1	1	Active state - Framed operating Mode only (Active2)[1]
1	0	0	Pending Deactivation state
1	0	1	Deactivated state
1	1	0	Active state - Transparent and Independent operating modes only (Active Tp)
1	1	1	Time-out state - during micro-interruption

6.0 Application Information

6.1 PCB Layout

The following are general considerations for PCB layout using the EMDP chip set:

- Refer to Figure 25 & Figure 26, and Table 28.
- Use a four-layer or more PCB layout, with embedded power and ground planes. Bring the digital power and ground planes over to include pins 1-6 and 24-28 of the IAF.
- Break up the power and ground planes into the following regions. Tie these regions together at the common point where power connects to the circuit:
- Digital Region
- Analog Region
- VCXO subregion
- IAFE, Line I/F, and IBIAS subregion
- Use larger “feed through” (via) and tracks for connecting the power and ground planes to the power and ground pins of the ICs than for signal connections. Place the decoupling capacitors right at the feed-through power/ground plane ties, or on the tracks to the IC power/ground pins as close to the pins as possible.
- On the User Interface Connector, route digital signals to avoid proximity to the TIP, RING, and CT lines.
- Provide at least 100 µF or more of bulk power supply decoupling at the point where power is connected to the Data Pump circuit.

6.1.1 Digital Section

- Keep all digital traces separated from the analog region of the Data Pump layout.
- Provide high frequency decoupling capacitors (0.01 µF ceramic or monolithic) around the EDSP as shown in Figure 26 and Figure 27.

6.1.2 Analog Section

The analog section of the PCB consists of the following subsections:

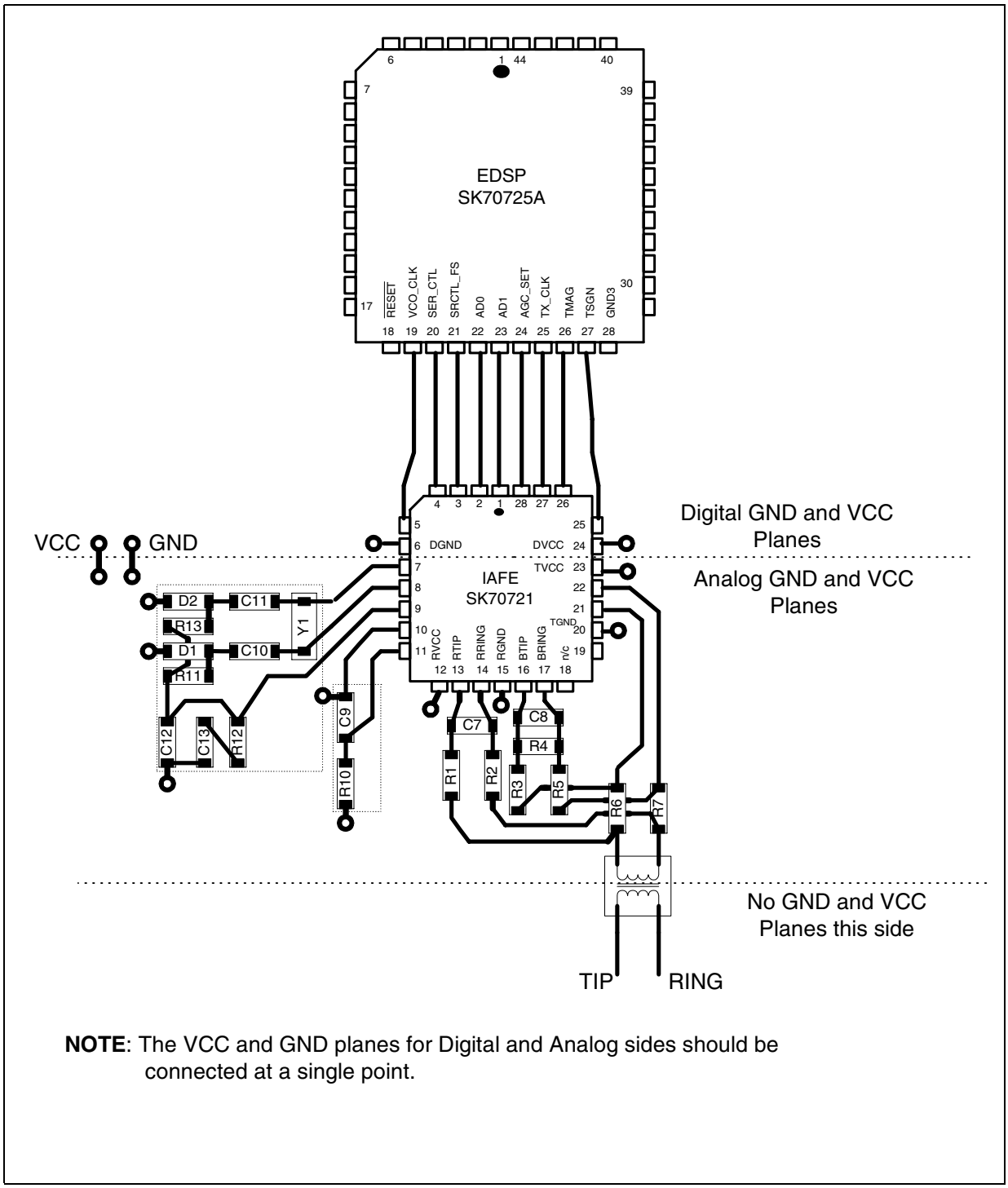
1. IAFE and power supply decoupling capacitors.
2. Bias Current Generator.
3. Voltage Controlled Crystal Oscillator.
4. Line Interface Circuit.
   — Route digital signals AD0, AD1, SRCTL_FS, SER_CTL, TSGN, TMAG, TX_CLK, and AGC_SET on the solder side of the PCB, and route all analog signals on the component side as much as possible.

  - — Route the following signal pairs as adjacent traces but keep the pairs separated from each other as much as possible:
  - — TTIP/TRING
  - — BTIP/BRING
  - — RTIP/RRING
- Do not run the analog ground plane under the transformer line side to maximize high voltage isolation.
- The IAFE should be placed such that pin 1 is near pin 23 of the EDSP and pins 12-18 are near the edge of the PCB, with the line transformer and connector.

6.2 Typical Application

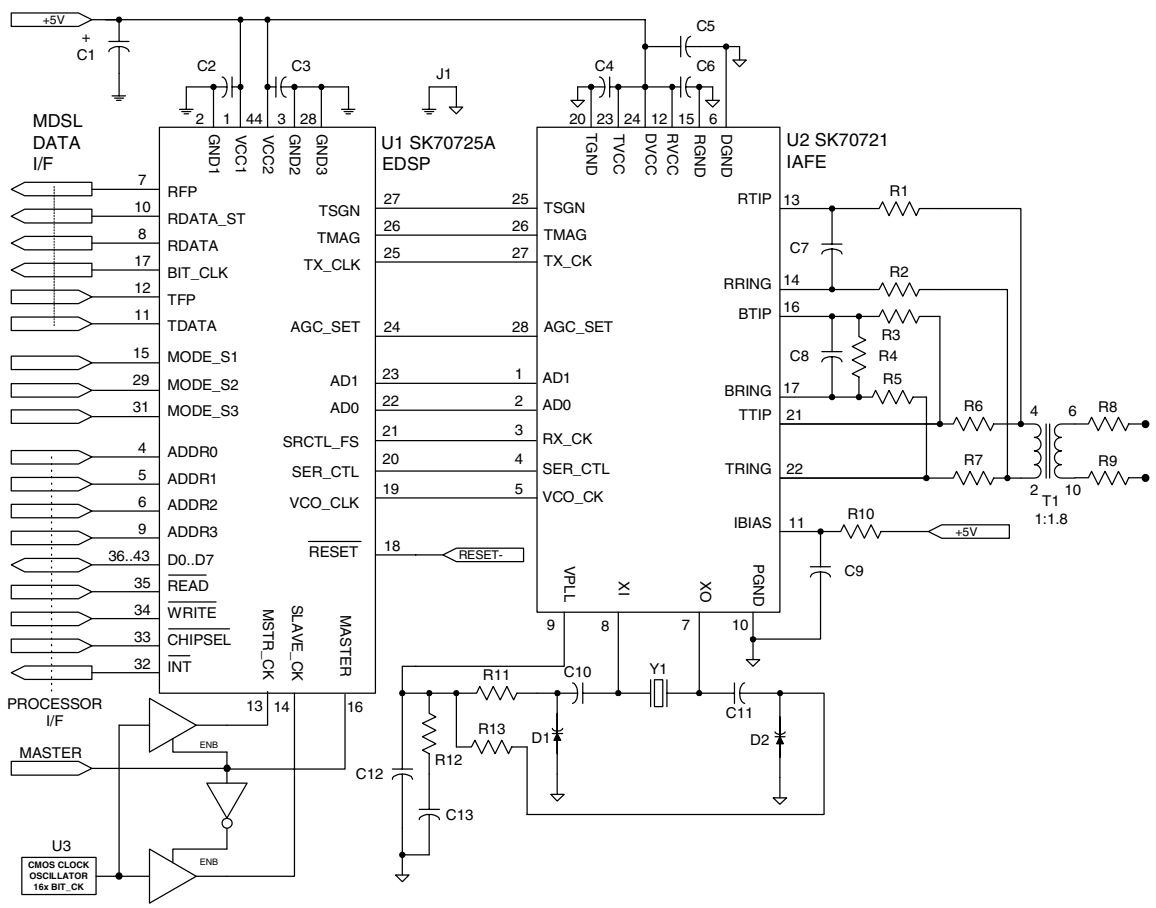
The EMDP can be used in many applications which are shown on page one of this data sheet. Typical Data Pump circuit remains the same in most of the applications. Figure 26 and Figure 27 show typical application schematics. Table 28 through Table 32 describe the components used in these typical applications. Circuits shown in Figure 26 and Figure 27 can be used at all the line rates and meet the ITU G.991.1, ANSI Committee T1E1.4-TR28 (T1E1.4/96-006), and ETSI ETR-152 requirements. The circuit shown in Figure 27 has improved performance in noise free environment at line rates below 784 Kbps. Refer to application note 76 for further details. The schematics show two tri-state buffers and one inverter to enable the use of the same circuit for either Master or Slave.

Figure 25. PCB Layout Guidelines (Figure 26 for schematic)



NOTE: The VCC and GND planes for Digital and Analog sides should be connected at a single point.

Figure 26. Typical Software Mode Application



NOTES:
1. Application is shown for operating mode 6 & 7.
2. The EDSP and IAFE should have independent ground planes connected at a single point near pin 5 of the IAFE.

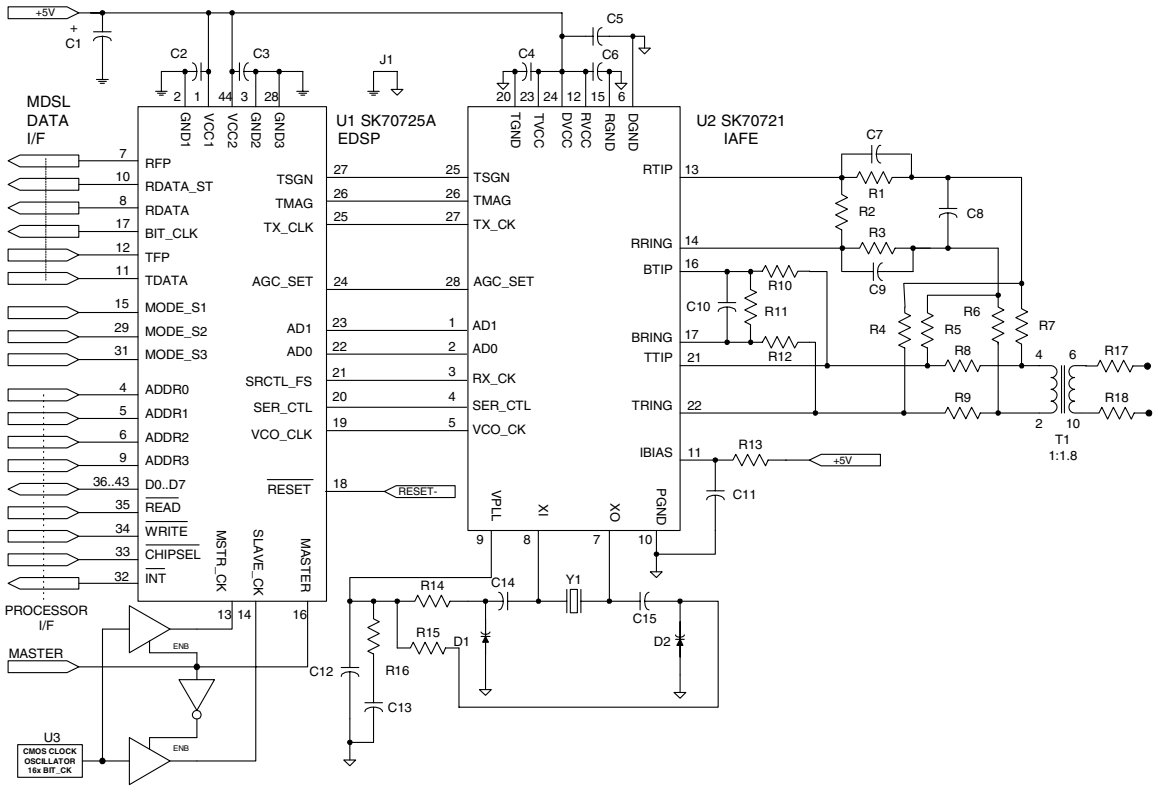
Table 28. Components for Typical Application (Figure 26)

Ref	Description	Ref	Description	Ref	Description
C2, C3, C12	0.01 µF, ceramic, 10%	R12	5.11 kΩ, 1%	D1, D2	Tuning Diode (Motorola MV209)
C13	100 µF, electrolytic, 20% low leakage ≤5 µA @ 25° C	R10	35.7 kΩ, 1%	U3	Clock Oscillator (Comclock, Inc.) 1168 Kbps: p/n - CM31CF - 18.688 MHz 784 Kbps: p/n - CM31CF - 12.544 MHz 528 Kbps: p/n - CM31CF - 8.448 MHz 400 Kbps: p/n - CM31CF - 6.4 MHz 272 Kbps: p/n - CM31CF - 4.352 MHz
		R11, R13	20.0 kΩ, 1%		
C10, 11	1000 pF, ceramic, 20%	R1, R2	301 Ω, 1%		
		R8, R9	5.6 Ω, 1% line feed fuse resistor (ALFR-2-5.6-1, IRC)		

Table 28. Components for Typical Application (Figure 26) (Continued)

Ref	Description	Ref	Description	Ref	Description
C7, 8	470 pF, COG or mica, 10%	R6, R7	18.2 Ω, 1%	Y1	Pullable Crystal 1168 kbps: 37.376 MHz (pn:8125611) 784 kbps: 25.088 MHz (pn:80546/1) 528 kbps: 16.896 MHz (pn:81522/1) 400 kbps: 12.800 MHz (pn:80546/5) 272 kbps: 8.704 MHz (pn:81523/1) (Hy-Q International)
C4, C5, C6, C9	0.1 µF, ceramic, 10%	R3, R5	604 Ω, 1%		
C1	100 µF, electrolytic, 20%	R4	909 Ω, 1%	T1	1:1.8 Transformer 400 kbps < Line rate < 784 kbps: Midcom 671-7376 or Pulse Engineering PE-68614. Line rate = 1168 kbps: Midcom 671-7671 or Pulse Engineering PE-68650. Line rate < 400 kbps: Midcom 50109.

Figure 27. Typical Application Optimized for Noise Free Performance



NOTES:
1. Application is shown for operating mode 6 & 7.
2. The EDSP and IAFE should have independent ground planes connected at a single point near pin 5 of the IAFE.

Table 29. Components for Typical Application (Figure 27)

Ref	Description	Ref	Description	Ref	Description
C2, C3, C12	0.01 µF, ceramic, 10%	R16	5.11 kΩ, 1%	D1, D2	Tuning Diode (Motorola MV209)
C13	100 µF, electrolytic, 20% low leakage ≤5 µA @ 25° C	R13	35.7 kΩ, 1%	Y1	Pullable Crystal (Hy-Q International): 1168 kbps: 37.376 MHz (pn:8125611) 784 kbps: 25.088 MHz (pn:80546/1) 528 kbps: 16.896 MHz (pn:81522/1) 400 kbps: 12.800 MHz (pn:80546/5) 272 kbps: 8.704 MHz (pn:81523/1)
		R14, R15	20.0 kΩ, 1%		
C14, 15	1000 pF, ceramic, 20%	R1, R2, R3	26.1 KΩ, 1%		
C10	470 pF, COG or mica, 10%	R8, R9	18.2 Ω, 1%		
C4, C5, C6, C11,	0.1 µF, ceramic, 10%	R10, 12	51.1 KΩ, 1%	U3	Clock Oscillator (Comclock, Inc.): 1168 Kbps: p/n - CM31CF - 18.688 MHz 784 Kbps: p/n - CM31CF - 12.544 MHz 528 Kbps: p/n - CM31CF - 8.448 MHz 400 Kbps: p/n - CM31CF - 6.4 MHz 272 Kbps: p/n - CM31CF - 4.352 MHz
C1	100 µF, electrolytic, 20%	R11	7.87 kΩ, 1%	T1	1:1.8 Transformer: 400 kbps < Line rate < 784 kbps: Midcom 671-7376 or Pulse Engineering PE-68614. Line rate = 1168 kbps: Midcom 671-7671 or Pulse Engineering PE-68650. Line rate < 400 kbps: Midcom 50109.
C7, 9	1500 pF, COG or mica, 10%	R4, R5	2.0 kΩ, 1%		
C8	270 pF, COG or mica, 10%	R6, R7	1.0 kΩ, 1%		
		R17, R18	5.6 Ω, 1% line feed fuse resistor (ALFR-2-5.6-1, IRC)		

Table 30. Typical Transformer Specifications (Figure 26 and Figure 27)

Parameter	Line Rate 272 kbps		Line Rate 784 kbps		Line Rate 1168 kbps	
	Value	Test Condition	Value	Test Condition	Value	Test Condition
Turns Ratio (IC:Line)	1:1.8 ± 1%		1:1.8 ± 1%		1:1.8 ± 1%	
Line Side Inductance	8.8 mH ± 5%	DC Bias = 0 mA,160 mA Freq = 1 kHz Deviation = ±5%	3.0 mH ± 5%	DC Bias = 0 mA,160 mA Freq = 1 kHz Deviation = ±5%	2.0 mH ± 5%	DC Bias = 0 mA,160 mA Freq = 1 kHz Deviation = ±5%
Leakage Inductance	≤ 30 µH	Line side w/ chip side shorted freq = rate/4 AC Bias 100 mA	≤ 30 µH	Line side w/ chip side shorted freq = rate/4 AC Bias 100 mA	≤ 30 µH	Line side w/ chip side shorted freq = rate/4 AC Bias 100 mA
Interwinding Capacitance	≤ 70 pF		≤ 70 pF		≤ 70 pF	
THD	≤ -70dB	DC Bias = 0 mA,160 mA Freq = 5 kHz	≤ -70dB	DC Bias = 0 mA,160 mA Freq = 5 kHz	≤ -70dB	DC Bias = 0 mA,160 mA Freq = 5 kHz
Longitudinal Balance	≥ 50dB	5 kHz - rate/4 kHz	≥ 50dB	5 kHz - rate/4 kHz	≥ 50dB	5 kHz - rate/4 kHz

Table 30. Typical Transformer Specifications (Figure 26 and Figure 27) (Continued)

Parameter	Line Rate 272 kbps		Line Rate 784 kbps		Line Rate 1168 kbps	
	Value	Test Condition	Value	Test Condition	Value	Test Condition
Return Loss	≥ 20dB ± 1%	40kHz - 200kHz	≥ 20 dB ± 1%	40 kHz - 200 kHz	≥ 20 dB ± 1%	40 kHz - 300 kHz
Isolation	1500 VRMS		1500 VRMS		1500 VRMS	
IC Side DC Resistance	≤ 3.2 Ω	Deviation = ±10%	≤ 3.2 Ω	Deviation = ±10%	≤ 3.2 Ω	Deviation = ±10%
Line Side DC Resistance	≤ 6.0 Ω	Deviation = ±10%	≤ 6.0 Ω	Deviation = ±10%	≤ 6.0 Ω	Deviation = ±10%
Operating Temperature	-40° to 85° C		-40° to 85° C		-40° to 85° C	

Table 31. Typical Crystal Specifications (Figure 26 and Figure 27)

Parameter	Line rate 272 kbps	Line rate 784 kbps	Line rate 1168 kbps
Frequency @C_L = 20 pF	8.704 MHz. Offset: -0, +40 ppm	25.088 MHz. Offset: -0, +40 ppm	37.376 MHz. Offset: -0, +40 ppm
Mode	Fundamental, Parallel Resonance	Fundamental, Parallel Resonance	Fundamental, Parallel Resonance
Pullability (C_L = 24 pF ⇨ 16 pF)	≥ +160 ppm	≥ +160 ppm	≥ +160 ppm
Operating Temperature	-40° to +85° C	-40° to +85° C	-40° to +85° C
Temperature Drift	≤ ±30 ppm	≤ ±30 ppm	≤ ±30 ppm
Aging Drift	≤ 5 ppm/year	≤ 5 ppm/year	≤ 5 ppm/year
Series Resistance	≤ 20 Ω	≤ 20 Ω	≤ 15 Ω
Drive Level	0.5 mW	0.5 mW	0.5 mW

Table 32. Typical Clock Oscillator Specifications

Parameter	Line rate 272 kbps	Line rate 784 kbps	Line rate 1168 kbps
Clock frequency	4.352 MHz	12.544 MHz	18.688 MHz
Tolerance	±32 ppm	±32 ppm	±32 ppm
Operating temperature	-40° to +85° C	-40° to +85° C	-40° to +85° C
Output level	CMOS level	CMOS level	CMOS level
Duty Cycle	40/60%	40/60%	40/60%

7.0 Test Specifications

Note: Table 33 through Table 43 and Figure 28 through Figure 35 represent the performance specifications of the EMDP chip set and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Table 35 through Table 43 are guaranteed over the recommended operating conditions specified in Table 34.

Table 33. IAFE Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage[1] (reference to ground[2])	TVCC, RVCC, DVCC	-0.3	+6.0	V
Input voltage[2, 3], any input pin	TVCC, RVCC, DVCC	- 0.3	VCC + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. No supply input may have a maximum potential of more than ±0.3 V from any other supply input.
2. TGND = 0V; RGND = 0V; DGND = 0V.
3. TVCC = RVCC = DVCC = VCC.

Table 34. IAFE and EDSP Recommended Operating Conditions

Parameter		Symbol	Min	Typ	Max	Unit
DC supply	IAFE EDSP	TVCC, DVCC, RVCC VCC1, VCC2	4.75	5.0	5.25	V
Ambient operating temperature		TA	-40	+25	+85	° C

Table 35. IAFE DC Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current (full operation)	ICC	–	80	120	mA	83 Ω resistor across TTIP and TRING
Input Low voltage	VIL	–	–	0.5	V	
Input High voltage	VIH	4.5	–	–	V	
Output Low voltage[2]	VOL	–	–	0.2	V	IOL < 1.6 mA
Output High voltage[3]	VOH	4.5	–	–	V	IOH < 40 µA
Input leakage current[4]	IIL	–	–	±50	µA	0 < VIN < VCC
Input capacitance (individual pins)	CIN	–	12	–	pF	
Load capacitance (VCO_CLK output)	CLREF	–	–	20	pF	

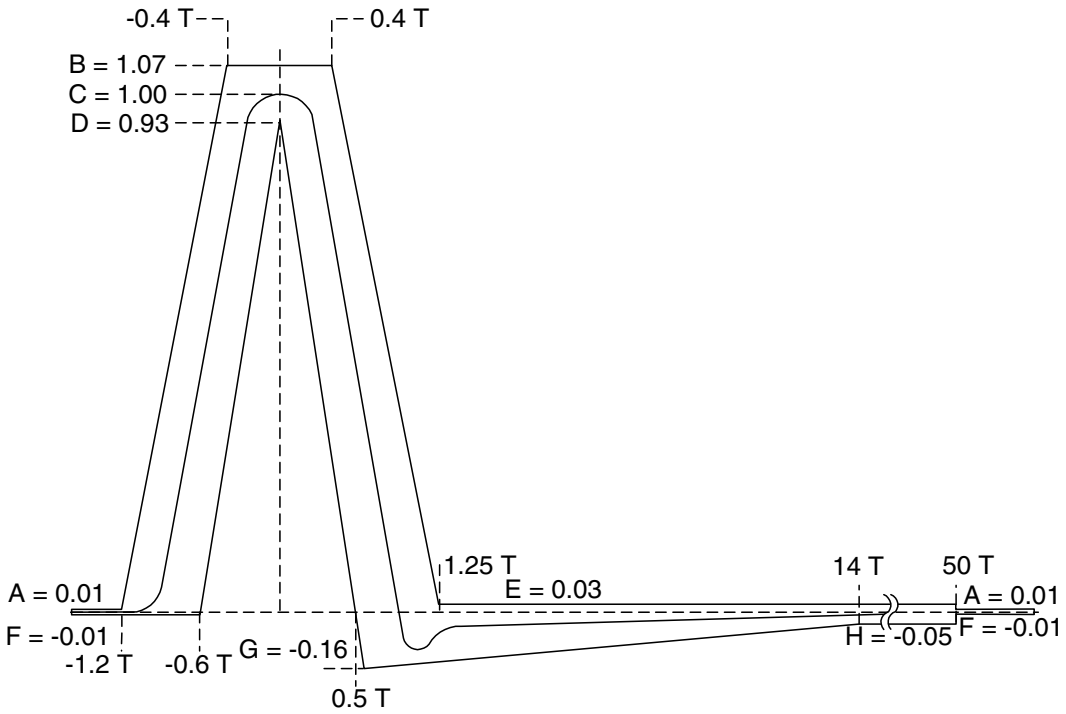
1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. IOL is sinking current.
3. IOH is sourcing current.
4. Applies to pins 3, 4, 25, 26 and 27.

Table 36. IAFE Transmitter Electrical Parameters

Parameter	Sym	Min	Typ[1]	Max	Unit	Test Conditions
Isolated pulse height at TTIP, TRING[2]	–	+2.455	+2.640	+2.825	Vp	TDATA High, TFP Low (+3)
	–	-2.825	-2.640	-2.455	Vp	TDATA Low, TFP Low (-3)
	–	+0.818	+0.880	+0.941	Vp	TDATA High, TFP High (+1)
	–	-0.941	-0.880	-0.818	Vp	TDATA Low, TFP High (-1)
Setup time (TSGN, TMAG)	t_{TSMSU}	5	–	–	ns	
Hold time (TSGN, TMAG)	t_{TSMH}	12	–	–	ns	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. Pulse amplitude measured across a 135 Ω resistor on the line side of the transformer using the application circuit shown in Figure 26 and Table 28.

Figure 28. IAFE Normalized Pulse Amplitude Transmit Template (Table 37)



NOTES:
1. Pulse amplitude measured across a 135 Ohms resistor on the line side of the transformer using the application circuit shown in Figure 26. Transformer specifications are listed in Table 30.
2. T is the baud period.

Table 37. IAFE Normalized Pulse Amplitude Transmit Template Values (Figure 28)

Normalized Levels		Quaternary Symbols (values in Volts)			
		+3	+1	-1	-3
A	.01	0.0264	0.0088	-0.0088	-0.0264
B	1.07	2.8248	0.9416	-0.9416	-2.8248
C	1.00	2.6400	0.8800	-0.8800	-2.6400
D	0.93	2.4552	0.8184	-0.8184	-2.4552
E	0.03	0.0792	0.0264	-0.0264	-0.0792
F	-0.01	-0.0264	-0.0088	0.0088	0.0264
G	-0.16	-0.4224	-0.1408	0.1408	0.4224
H	-0.05	-0.1320	-0.0440	0.0440	0.1320
1. T = 7.35 ms, 5.00 ms, 3.79 ms, 2.55 ms (@ 272, 400, 528 & 784 kbps)					

Figure 29. Transmit Power Spectral Density—Upper Bound

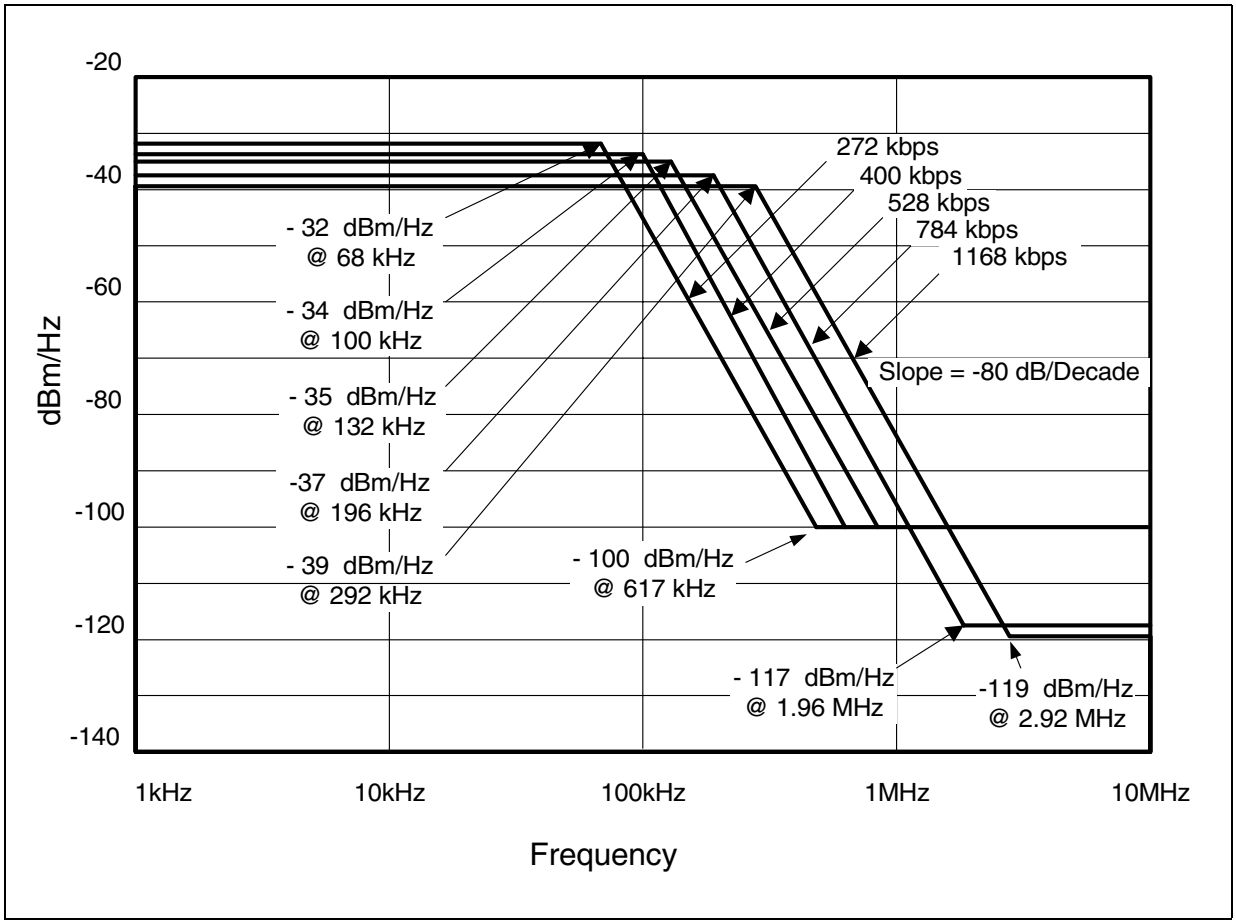
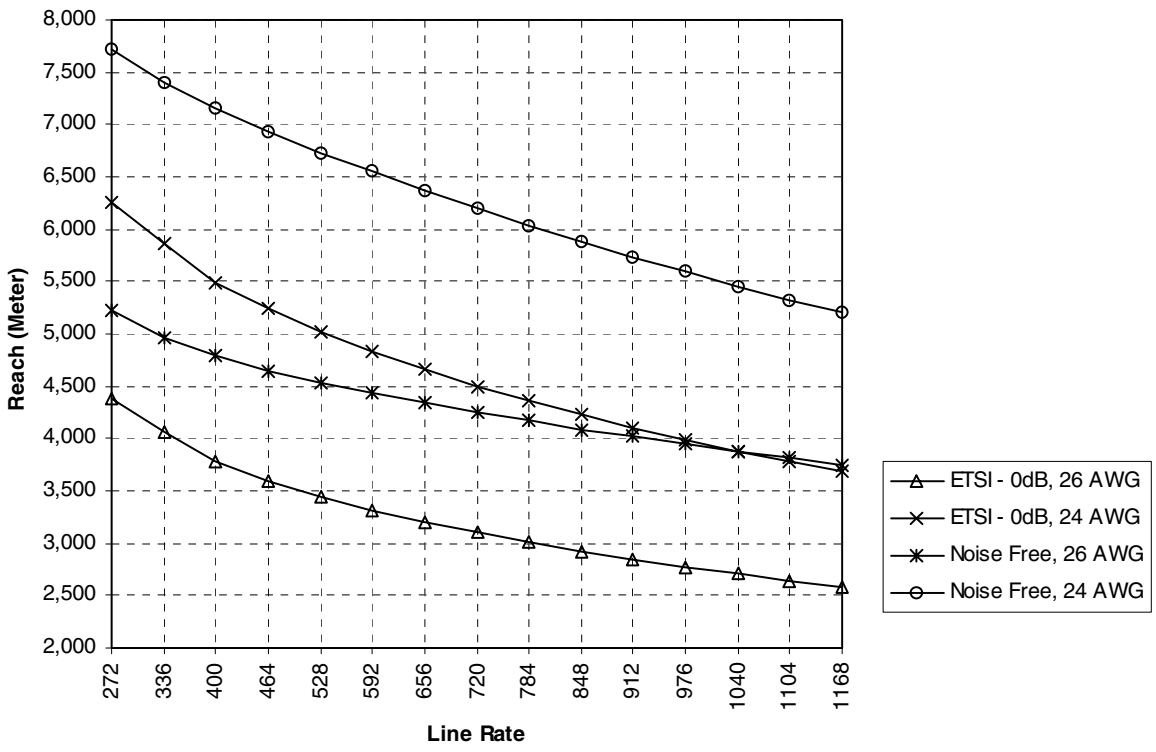


Table 38. IAFE Receiver Electrical Parameters

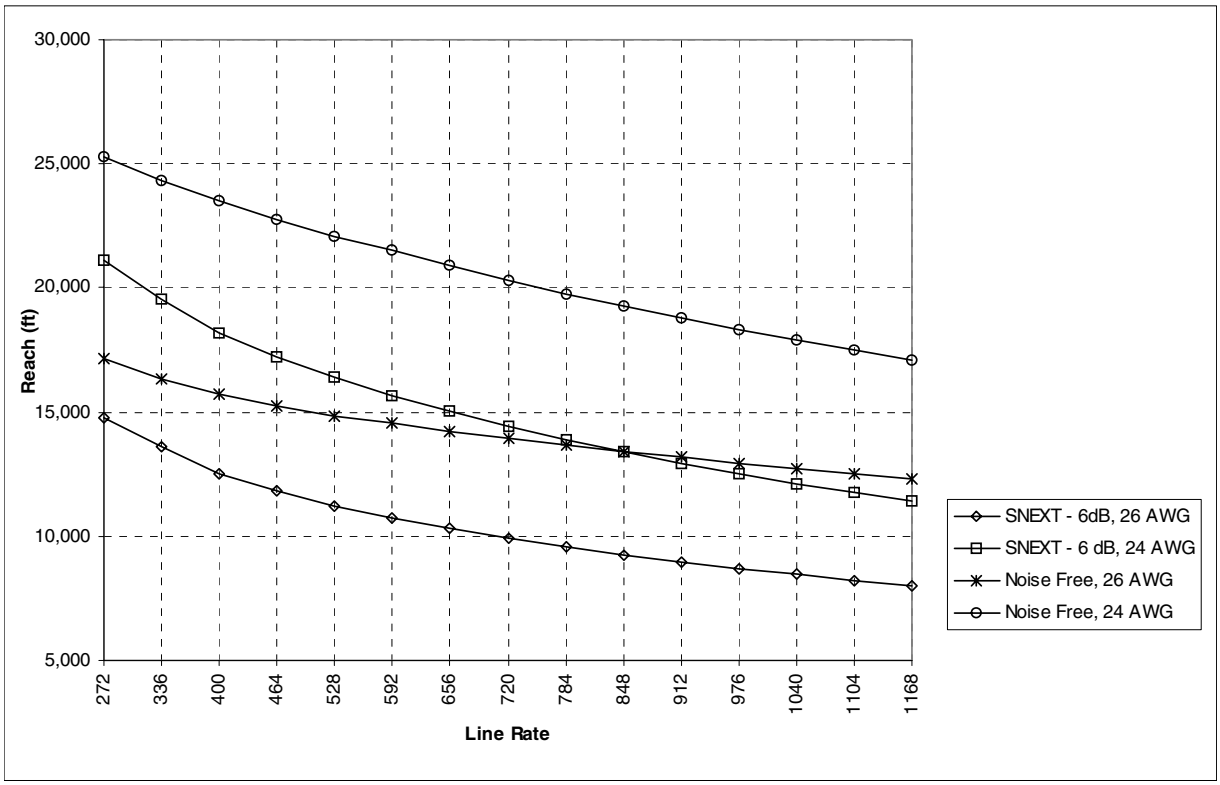
Parameter	Sym	Min	Typ	Max	Unit	Test Conditions
Propagation delay (AD0, AD1)	tADD	–	–	25	ns	
Total harmonic distortion	–	–	-80	–	dB	V(RTIP, RRING) = 3 Vpp @ 50 kHz
RTIP, RRING, to BTIP, BRING gain ratio	–	0.99	1.0	1.01	V/V	

Figure 30. Typical Performance vs. Line Rate and Cable Gauge (Metric)



NOTES:
1. Noise-free range is specified with a Bit Error Ratio (BER) less than or equal to 1.0×10^{-7}.
2. The range with ETSI shaped noise corresponds to a 0 dB margin with a BER less than or equal to 1.0×10^{-7}. The power spectral density for ETSI standard noise is defined in ETSI ETR-152 section 6.3.3.1.

Figure 31. Typical Performance vs. Line Rate and Cable Gauge (English)



NOTES:
1. Noise-free range is specified with a BER less than or equal to 1.0 x 10^{-7}.
2. There are no generally accepted noise models for MDSL systems. Performance is shown based upon the simulation done using self NEXT at all the line rates.
3. The range with ETSI shaped noise corresponds to a 0 dB margin with a BER less than or equal to 1.0 x 10^{-7}. The power spectral density for ETSI standard noise is defined in ETSI ETR-152 section 6.3.3.1.

Table 39. EDSP Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage[1] (reference to ground[2])	VCC2, VCC1	-0.3	+6.0	V
Input voltage[2], any input pin	–	- 0.3	VCC2 + 0.3	V
Continuous output current, any output pin	–	–	±25	mA
Storage temperature	TSTOR	-65	+150	° C

Caution: Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1. The maximum potential between VCC2 and VCC1 must never exceed ±1.2 V.
2. GND3 = 0 V; GND2 = 0 V; GND1 = 0 V.

Table 40. EDSP DC Electrical Characteristics

Parameter		Sym	Min	Typ[1]	Max	Unit	Test Conditions
Supply current	272 kbps 400 kbps 528 kbps 784 kbps 1168 kbps	ICC	– – – – –	40 55 72 106 148	– – – – –	mA	Room temperature, VCC1, VCC2 = +5V
Input Low voltage		VIL	–	–	0.5	V	
Input High voltage		VIH	4.0	–	–	V	
Output Low voltage[2]		VOL	–	–	GND +0.3	V	IOL < 1.6 mA
Output High voltage[3]		VOH	VCC2 - 0.5	–	–	V	IOH < 40 µA
Input leakage current[4]		IIL	–	–	±50	µA	0 < VIN < VCC2
Tristate leakage current[5]		ITOL	–	–	±30	µA	0 < V < VCC2
Input capacitance (individual pins)		CIN	–	12	–	pF	
Load capacitance (MSTR_CLK output)		CLREF	–	–	15	pF	

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. IOL is sinking current.
3. IOH is sourcing current.
4. Applies to pins 4, 5, 11, 12, 14, 16, 18, 19, 22, 23, 24, 29, 31, 33, 34 and 35. Applies to pins 6, 9, 12, 13, and 36-43, when configured as inputs.
5. Applies to pins 7, 8, 10, 15, 17, 30, 32 and 36-43, when tristated.

Table 41. EMDP Data Interface Timing Specifications

Parameter		Symbol	Min	Typ[1]	Max	Unit
BIT_CLK, TBIT_CLK, and RBIT_CLK frequency		Fbit_clk	272	–	1168	kHz
QUAT_CLK, TQUAT_CLK, and RQUAT_CLK frequency		Fquat_clk	136	–	584	kHz
MSTR_CLK frequency		Fmstrclk	4.352	–	18.688	MHz
MSTR_CLK frequency tolerance		Tolmstrclk	-32	0	+32	ppm
MSTR_CLK duty cycle		Dutymstr_clk	40%	50%		percent
SLAVE_CLK frequency tolerance[2]		TolSlave_clk	-32	0	+32	ppm
BIT_CLK, TBIT_CLK, and RBIT_CLK pulse width (High)[3]	272 kbps 400 kbps 528 kbps 784 kbps 1168 kbps	Tbpw	– – – – –	1.840 1.250 0.947 0.638 0.428	– – – – –	µs
BIT_CLK and TBIT_CLK delay from the MSTR_CLK		Tmbdly	–	–	50	ns
QUAT_CLK and TQUAT_CLK delay from the BIT_CLK and TBIT_CLK respectively		Tbqdly	–	–	25	ns
Transition time on any digital output[3]		Tto	–	5	10	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. SLAVE_CLK must meet this tolerance about a frequency of 16 times the BIT_CLK frequency.
3. Measured with 15 pF load.

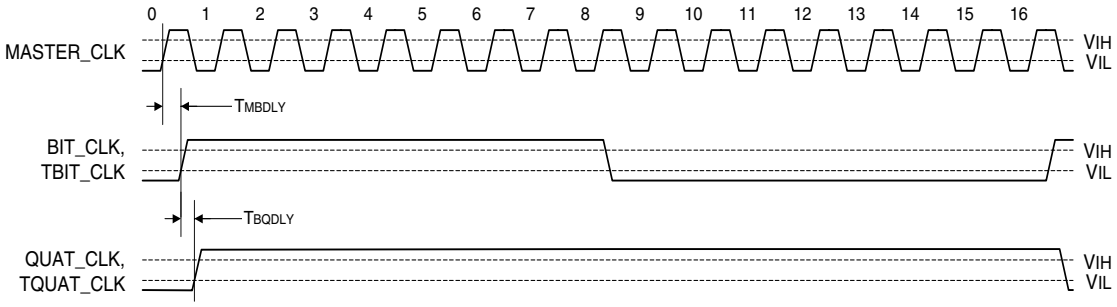
Table 41. EMDP Data Interface Timing Specifications (Continued)

Parameter	Symbol	Min	Typ[1]	Max	Unit
Transition time on any digital input	Tti	–	–	25	ns
TFP setup time to BIT_CLK rising edge	Ttfsub	50	–	–	ns
TDATA setup time to BIT_CLK rising edge in framed mode 6 and 7. TDATA hold time to BIT_CLK and TBIT_CLK falling edge in Transparent and Independent modes 0,1,2,4, and 5.	Tdasub	50	–	–	ns
TFP hold time from BIT_CLK rising edge	Ttfhlb	50	–	–	ns
TDATA hold time to BIT_CLK rising edge in framed mode 6 and 7. TDATA setup time to BIT_CLK and TBIT_CLK falling edge in Transparent and Independent modes 0,1,2,4, and 5.	Tdahlb	50	–	–	ns
RDATA delay from BIT_CLK falling edge in framed mode 6 and 7. RDATA delay from BIT_CLK and RBIT_CLK rising edge in Transparent and Independent modes 0,1,2,4, and 5.	Trdbdly	–	–	50	ns
RFP delay from BIT_CLK falling edge	Trfbdly	–	–	50	ns
RDATA_ST delay from BIT_CLK falling edge	Tstbdly	–	–	50	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.
2. SLAVE_CLK must meet this tolerance about a frequency of 16 times the BIT_CLK frequency.
3. Measured with 15 pF load.

Figure 32. EDSP Clock and Data Interface Timing

A) Clock Timings



B) Timings in Framed Modes 6 and 7

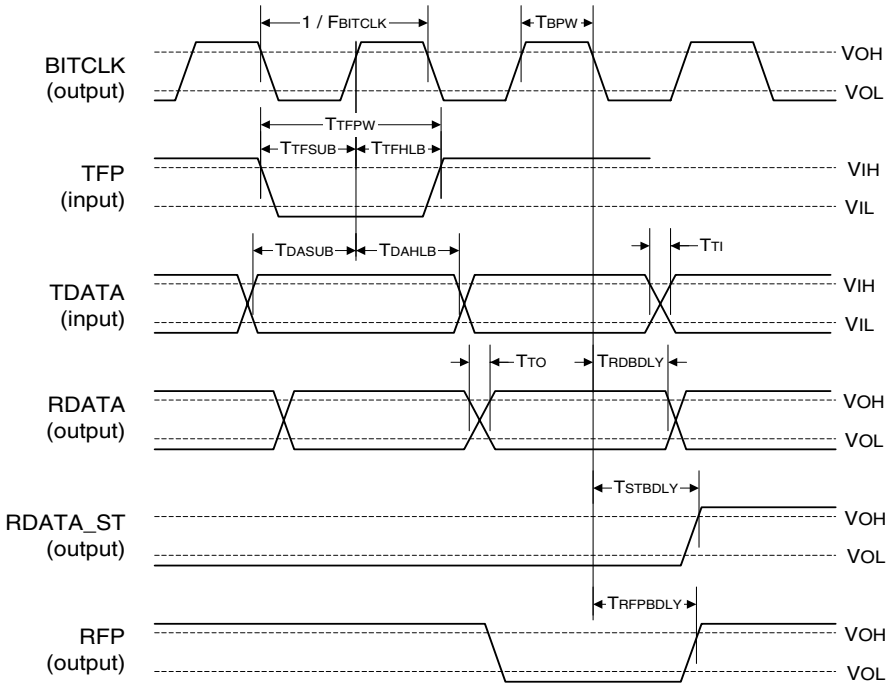


Figure 33. EDSP Data Interface Timing

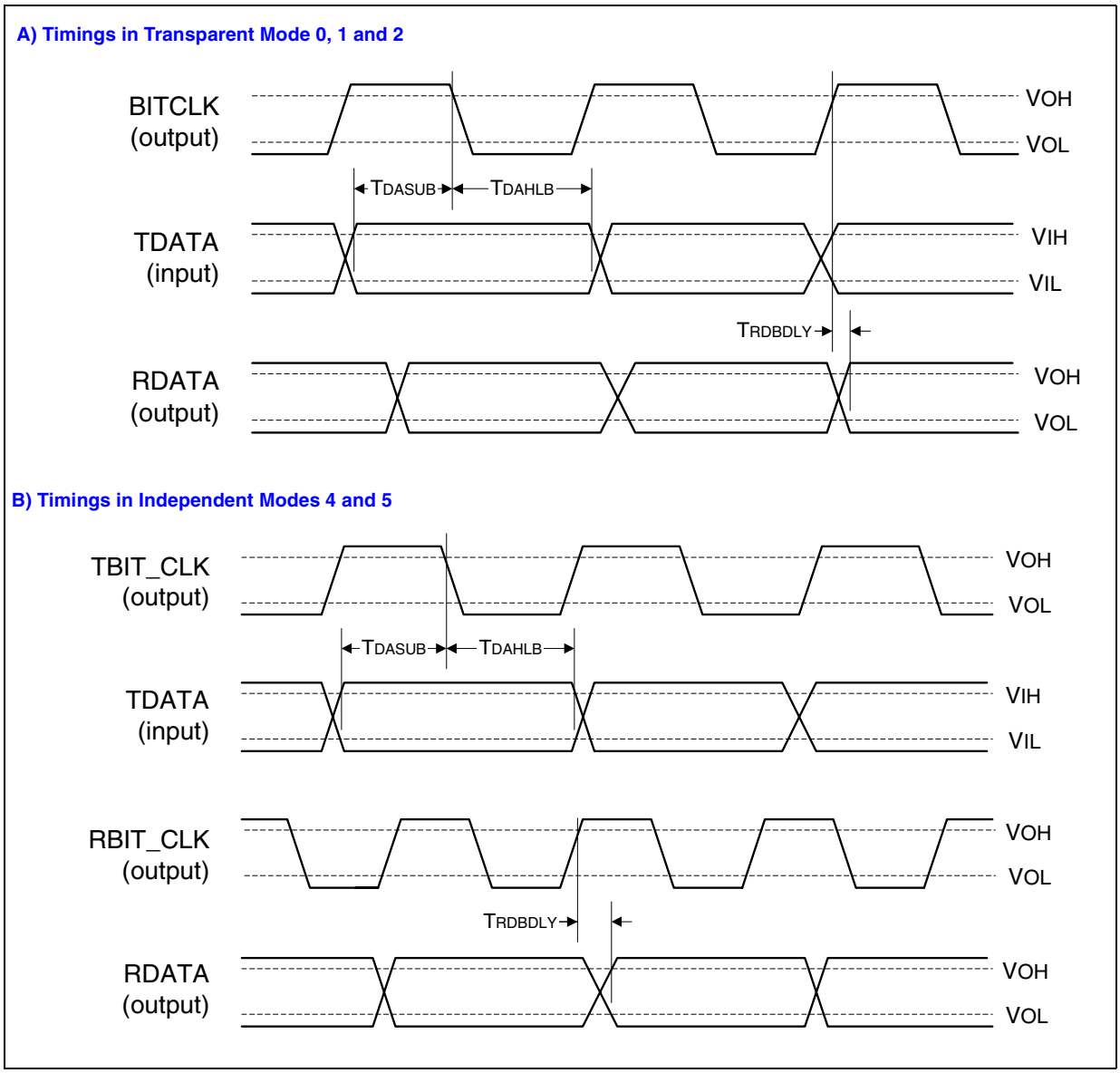


Table 42. EDSP Microprocessor Interface Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{RESET}}$ pulse width Low.	Trpwl	500	–	–	ns
$\overline{\text{RESET}}$ to $\overline{\text{INT}}$ clear (10 kΩ resistor from $\overline{\text{INT}}$ to VCC2).	Tinth	–	–	300	ns
$\overline{\text{RESET}}$ to data tri-state on D0-7.	Tdthz	–	–	100	ns
$\overline{\text{CHIPSEL}}$ setup to $\overline{\text{READ}}$ falling edge.	Tcssur	50	–	–	ns

1. Timing for all outputs assumes a maximum load of 30 pF.
2. “Address” refers to input signals A0, A1, A2, and A3. “Data” refers to I/O signals D0, D1, D2, D3, D4, D5, D6, and D7.

Table 42. EDSP Microprocessor Interface Timing Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{CHIPSEL}}$ setup to $\overline{\text{WRITE}}$ rising edge.	Tcssuw	50	–	–	ns
$\overline{\text{CHIPSEL}}$ hold from $\overline{\text{WRITE}}$ rising edge.	Tcshlw	50	–	–	ns
$\overline{\text{CHIPSEL}}$ High to data tri-state.	Tcsd	–	–	50	ns
$\overline{\text{READ}}$ Low to data active.	Trdda	–	–	100	ns
$\overline{\text{READ}}$ High to data valid	Trddt	80	–	–	ns
$\overline{\text{READ}}$ High to $\overline{\text{INT}}$ clear when reading register RD0.	Trdint	–	–	200	ns
Data setup to $\overline{\text{WRITE}}$ rising edge.	Tdsuw	10	–	–	ns
Data hold from $\overline{\text{WRITE}}$ rising edge.	Tdhlw	10	–	–	ns
Address setup to $\overline{\text{READ}}$ falling edge.	Tadsur	50	–	–	ns
Address hold from $\overline{\text{READ}}$ rising edge.	Tadhlr	10	–	–	ns
Address setup to $\overline{\text{WRITE}}$ rising edge	Tadsuw	50	–	–	ns
Address hold from $\overline{\text{WRITE}}$ rising edge	Tadhlw	10	–	–	ns

1. Timing for all outputs assumes a maximum load of 30 pF.
2. “Address” refers to input signals A0, A1, A2, and A3. “Data” refers to I/O signals D0, D1, D2, D3, D4, D5, D6, and D7.

Figure 34. RESET Timing (Software Control Mode)

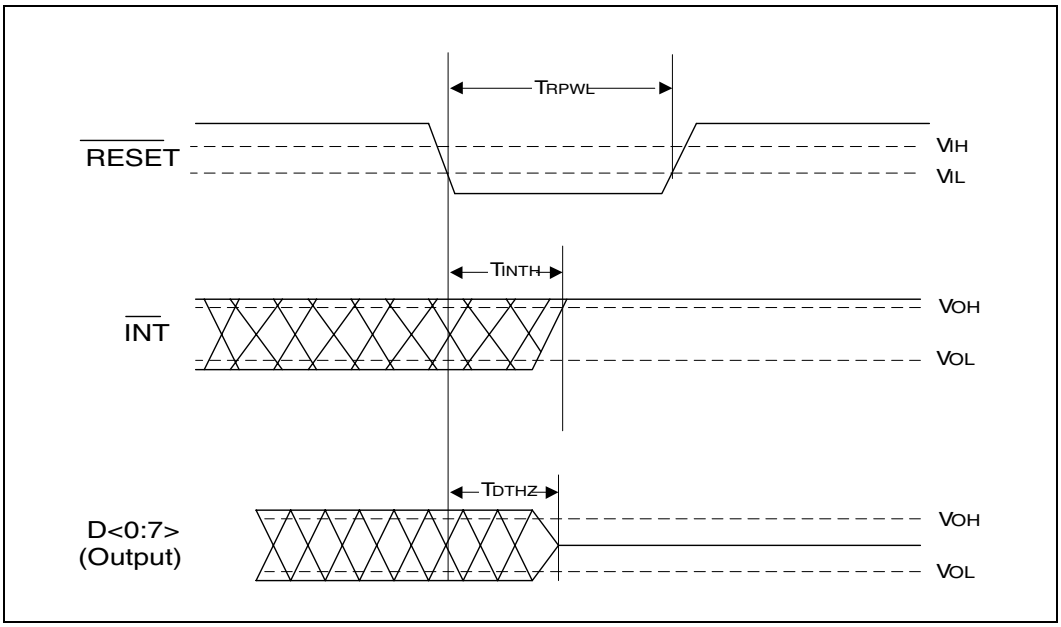


Figure 35. EDSP Read and Write Timing (Software Control Mode)

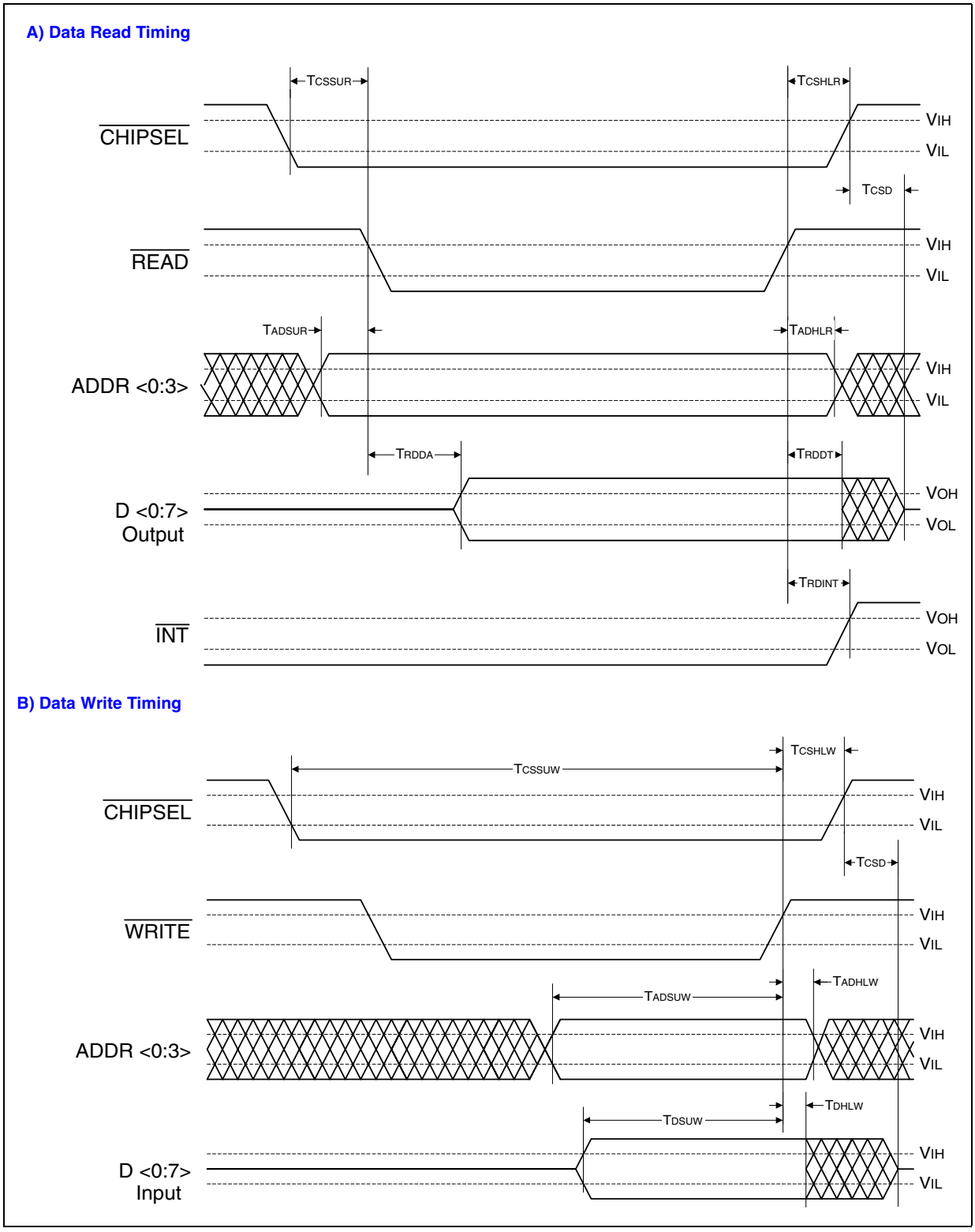
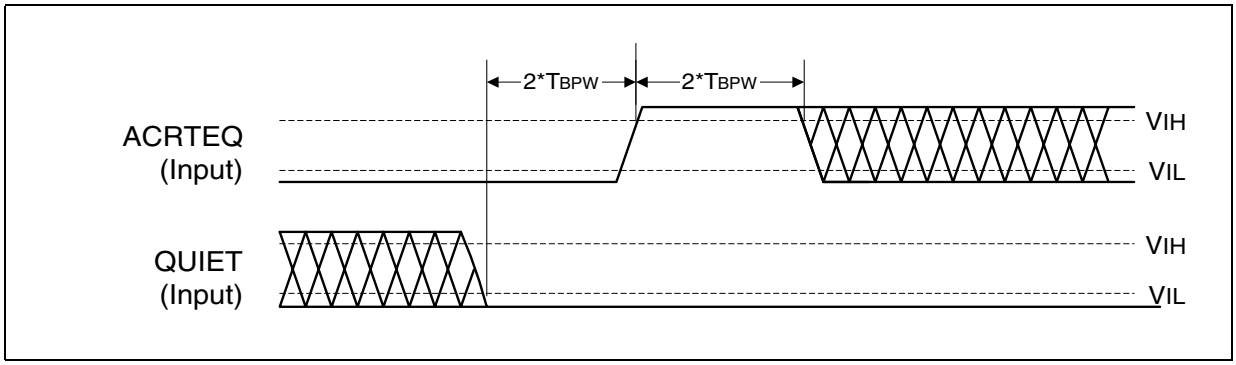


Table 43. General System and Hardware Mode Timing

Parameter		Min	Typ[1]	Max	Unit
Throughput delay from TFP of Master to RFP of Slave in framed modes 6 and 7.	272 kbps	–	221	–	µs
	400 kbps	–	151	–	
	528 kbps	–	114	–	
	784 kbps	–	77	–	
	1168 kbps	–	52	–	
Throughput delay from TDATA of Master to RDATA of Slave in Transparent modes 0, 1 and 2.	272 kbps	–	221	–	µs
	400 kbps	–	151	–	
	528 kbps	–	114	–	
	784 kbps	–	77	–	
	1168 kbps	–	52	–	
Throughput delay from TDATA of Master to RDATA of Slave in Independent modes 4 and 5.	272 kbps	–	215	–	µs
	400 kbps	–	146	–	
	528 kbps	–	111	–	
	784 kbps	–	75	–	
	1168 kbps	–	50	–	
Hardware mode, ACTREQ pulse width (High or Low)		$2*t_{BPW}$	–	–	µs

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Figure 36. ACTREQ Signal Timing (Hardware Mode)

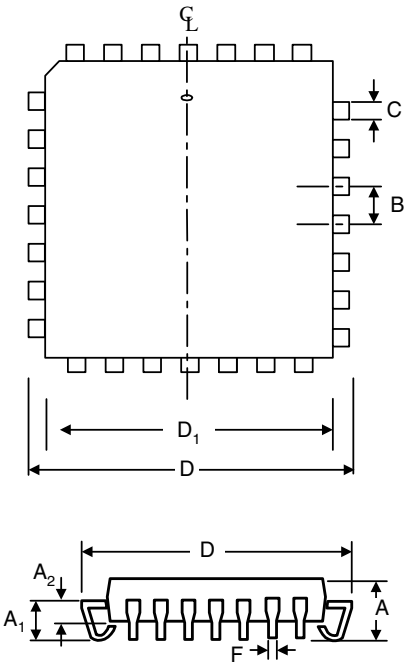


8.0 Mechanical Specifications

Figure 37. Package Specifications

Integrated Analog Front End (IAFE)

- 28 pin PLCC
- P/N SK70721PE
- Extended Temperature Range (-40° to + 85° C)

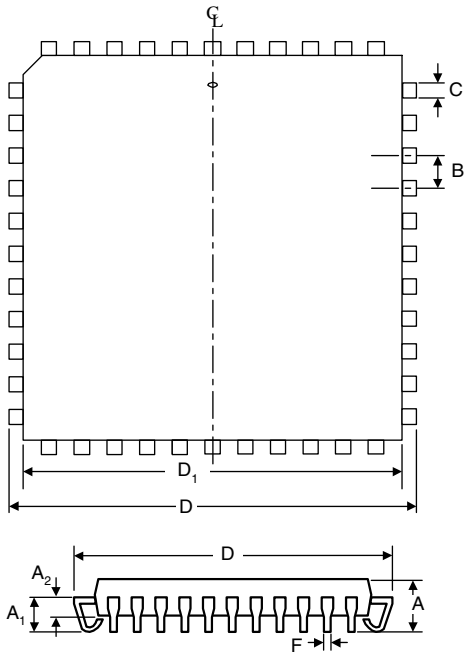


Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.485	0.495	12.319	12.573
D1	0.450	0.456	11.430	11.582
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers

Enhanced Digital Signal Processor (EDSP)

- 44 pin PLCC
- P/N SK70725APE
- Extended Temperature Range (-40° to + 85° C)



Dim	Inches		Millimeters	
	Min	Max	Min	Max
A	0.165	0.180	4.191	4.572
A1	0.090	0.120	2.286	3.048
A2	0.062	0.083	1.575	2.108
B	.050 BSC[1] (nominal)		1.27 BSC[1] (nominal)	
C	0.026	0.032	0.660	0.813
D	0.685	0.695	17.399	17.653
D1	0.650	0.656	16.510	16.662
F	0.013	0.021	0.330	0.533

1. BSC—Basic Spacing between Centers

9.0 Acronyms

Table 44. Acronyms

Acronym	Description
ACTREQ	Activation Request
BELB	Back-End Loop Back
BER	Bit Error Ratio
COFA	Change Of Frame Alignment
DFE	Decision Feedback Equalization
EC	Echo-Canceller
EDSP	Enhanced Digital Signal Processor
EMDP	Enhanced Multi-Rate DSL Data Pump
FFE	Feed Forward Equalizer
FSW	Frame Synchronization Word
FELB	Front End Loopback
ILMT	Insertion Loss Measurement Test
IAFE	Integrated Analog Front-End
LL	Loop Loss
LOOPID	Loop Number
LOS	Loss Of Signal
MAT	Master Activation Timer
MATC	Master Activation Timer Constant
MIT	Micro-Interruption Timer
MITR	Micro-Interruption Timer Register
MSB	Most Significant Bits
PLL	Phase-Locked Loop
RFP	Receive Frame Pulse
RPTR	Repeater Mode
SNR	Signal to Noise Ratio
TXTST	Transmit Test Pulse Enable