

SEMI DRIVER®

Double IGBT driver

SKHI 26 W

SKHI 26 F

Absolute Maximum Ratings (Ta=25 °C)			
Symbol	Term	Values	Unit
V _S	Supply voltage primary	18	V
V _{IH}	Input signal voltage (HIGH)	VS ± 0,3	V
I _{IH}	Input signal current (HIGH)	0,34	mA
Q _{Gate max}	Max. output charge per pulse	± 10	µC
I _{outPEAK}	Output peak current	± 8	A
I _{outAV}	Output average current	± 100	mA
V _{CE}	Collector-emitter maximum voltage sense	1600	V
dv/dt	Rate of rise and fall of voltage (secondary to primary side)	75	kV/µs
V _{isol IO}	Isolation test volt. IN-OUT (2 sec. AC)	4000	V
T _{op}	Operating temperature (SKHI 26 W)	- 25 ... + 85	°C
	Operating temperature (SKHI 26 F)	0 ... + 70	°C
T _{stg}	Storage temperature (SKHI 26 W)	- 25 ... + 85	°C
	Storage temperature (SKHI 26 F)	0 ... + 70	°C

Features

- Double driver for half bridge modules
- SKHI 26 drives all SEMIKRON IGBT's with V_{CE} up to 1200 V
- SKHI 26 F has fibre optic input
- SKHI 26 W has wire (galvanic) input
- CMOS compatible inputs
- Short circuit protection by V_{CE} monitoring and soft switch off
- Driver interlock top/bottom
- Isolation by transformers
- Supply undervoltage protection (< 13 V)
- Error latch / open-collector output (SKHI 26 W)
- Isolation by transformers
- DC bus voltage up to 1200 V

Typical Applications

- High power switches or paralleled IGBTs
- Driver for IGBT modules in bridge circuits in choppers, inverter drives, UPS and welding inverters

Electrical Characteristics (Ta=25 °C)			
Symbol	Term	Values	Unit
V _S	Supply voltage primary side	15 ± 0,6	V
I _S	Supply current primary side max.	700	mA
I _{SO}	Supply current primary side (stand by)	175	mA
V _{IT+}	Input threshold voltage (HIGH) min	12,9	V
V _{IT-}	Input threshold voltage (LOW) max	2,1	V
V _{G(on)}	Turn-on output gate voltage	+ 15	V
V _{G(off)}	Turn-off output gate voltage	- 8	V
td(on) _{IO}	Input-output turn-on propagation time	1,0 + t _{TD}	µs
td(off) _{IO}	Input-output turn-off propagation time	1,0	µs
t _{TD}	Dead time	3,3	µs
t _{pon-error}	propag. delay time - on error	1,0	µs
t _{pReset}	Min. pulse width error memory RESET	5,0	µs
V _{OH} ¹⁾	Logic high output voltage ERROR state	max. 30	V
V _{OL} ¹⁾	Logic low output voltage NO-ERROR state	max. 0,5	V
I _{sink} ¹⁾	Sink output current NO-ERROR	30	mA
V _{CEstat}	Reference voltage for V _{CE} monitoring	5,2	V

¹⁾ Open-collector transistor

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Dimensions of SKHI 26 W

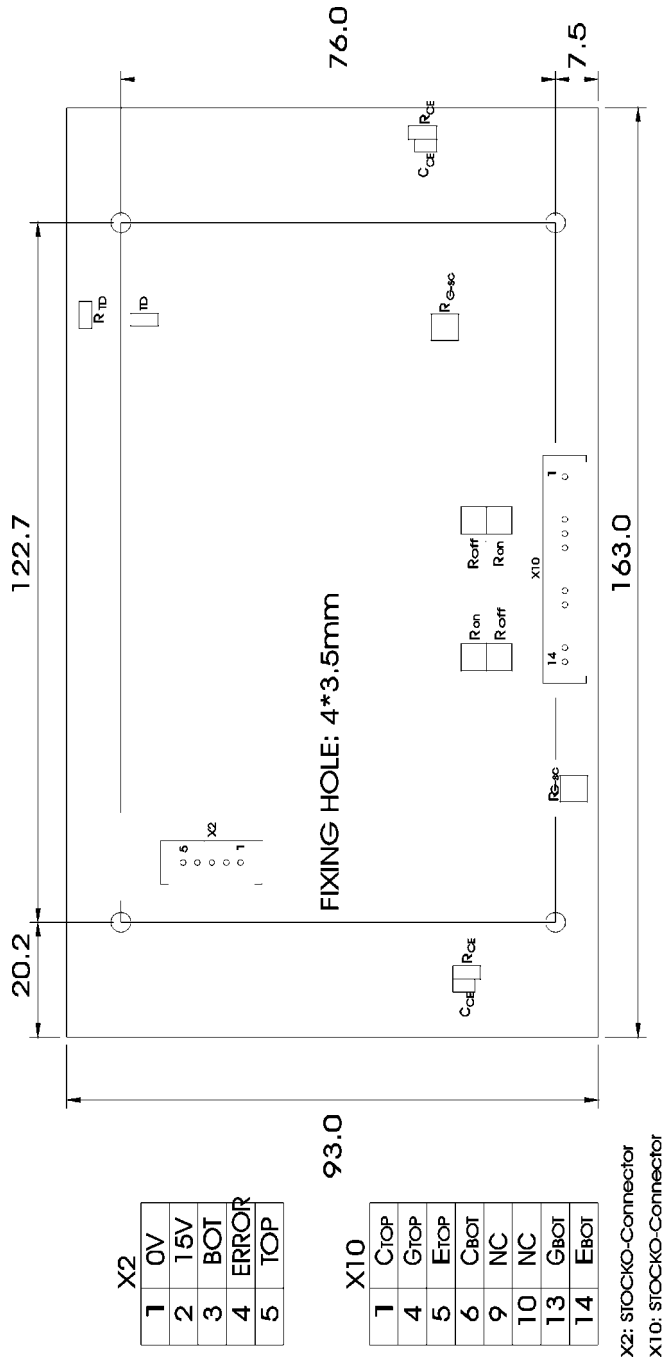


Fig. 2 Positions of the terminals (view from above) and dimensions (in mm).

Dimensions of SKHI 26 F

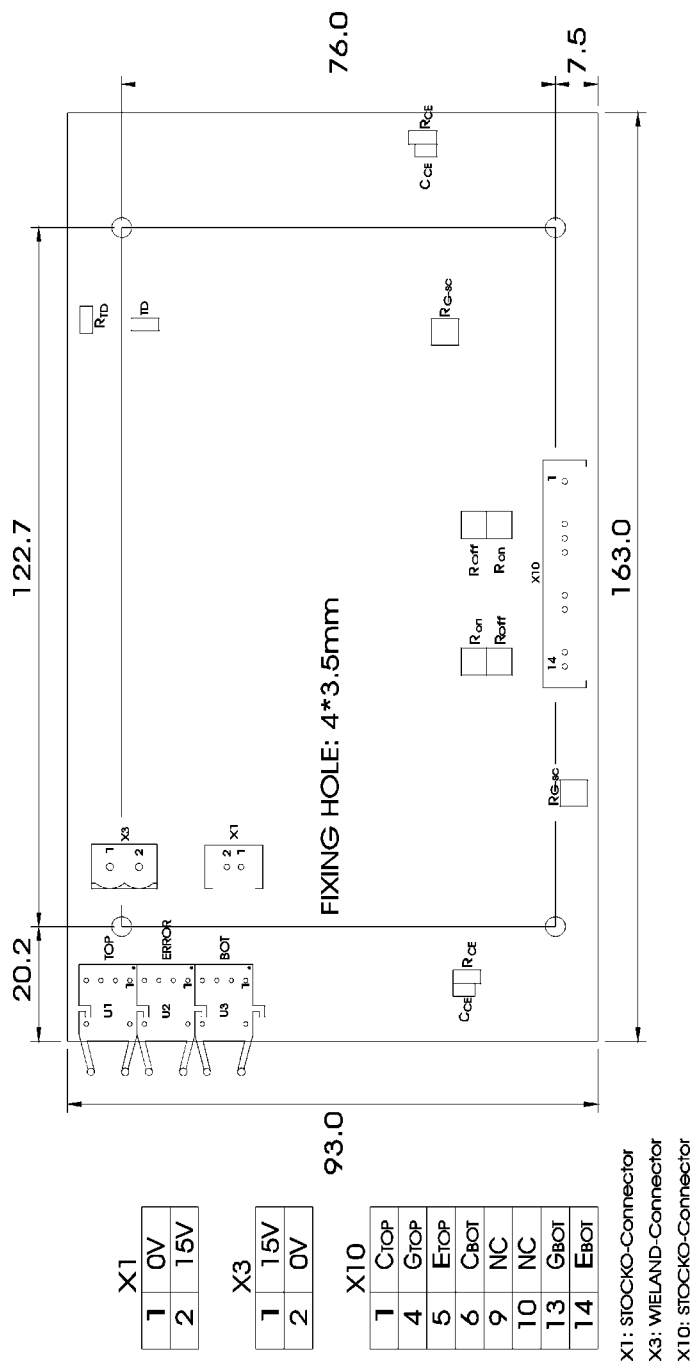


Fig. 3 Positions of the terminals (view from above) and dimensions (in mm). The connectors X1 and X3 can be used selective.

SEMI DRIVER SKHI 26W and SKHI 26F

High Power Double IGBT Driver

Technical Explanations

A. Properties and Functions of the Driver

1. The driver comprises short circuit protection for two IGBTs in half bridge (pair of arms) connection. If a single IGBT is driven, output TOP is to be used, and the terminal C_{BOT} of output BOT is to be connected to terminal E_{BOT}.
2. Short circuit protection is provided by measuring the collector-emitter voltage. In case of short circuit the soft turn-off circuit automatically increases the IGBT turn-off time and hence reduces the DC voltage overshoot.
3. The IGBTs are turned on by applying a positive gate-emitter voltage of 15 V, and turned off by a negative gate-emitter voltage of -8 V. In case of a failure of the supply voltage the gate-emitter connection is provided by a 22 k Ω resistor.
4. The driver also comprises the auxiliary power supplies for the two boosters which are isolated by DC/DC converters.
5. The two IGBTs of the half bridge are interlocked in order to prevent them from being in the on-state simultaneously. The locking time between the turn-off signal for one IGBT and the release of the turn-on signal for the other one is typically 3,3 μ s ($> t_{\text{doff}}$).
6. In the case of a short circuit both IGBTs are turned off immediately. An error memory prevents the IGBTs from being turned on again. The status of this memory may be fed back to the control circuit via an open collector transistor (SKHI 26 W) (error signal). The error memory is only reset when both input signals are zero.
7. The nominal voltage of the power supply V_S is +15 V. Its band of variation is from 14,4 to 15,6 V. The current required is lower than 700 mA (conditions: 85 °C temperature, V_S = 15 V). Any undervoltage below +13 V is monitored, and the IGBTs are turned off. An error signal is released. Overvoltage is not monitored.
8. The switching signals are transmitted by isolating pulse transformers. The isolation test voltages 2,5 kV_{AC}.

The max. dv/dt rating between primary and secondary side is 75 kV/ μ s.
9. The input and output signals are CMOS compatible, for "W" version. The inputs have a Schmitt trigger characteristic to suppress spurious pulses. The thresholds of the inputs are

 $V_{\text{IT+}} = \text{min. } 12,9 \text{ V}$
 $V_{\text{IT-}} = \text{max. } 2,1 \text{ V}$
10. The operating temperature range is 0 ... + 70 °C.
Typ SKHI 26W: T_{amb} = - 25 °C ... + 85 °C.

11. The typical delay times and propagation times for signals are
Turn-on: 1,0 + t_{TD} input to output
Turn-off: 1 μ s input to output
Error: 1 μ s error input to error signal output
12. In order to optimise the turn-on and turn-off speed resistors are connected, but external resistors R_g must be added mainly for parallel connections, according to the conditions of the given application. External resistors R_g, R_{ex} and R_{cx} should be mounted on additional circuit board near the paralleled modules. The R_{ex} assumes a value of 0,5 Ω and its function is to avoid the main current to circulate by the auxiliary emitter which could make the emitter voltage against ground unbalanced.

The R_{cx} has a value of 47 Ω and its function is to create an average of V_{CEsat} in case of short circuit for V_{CE}-monitoring (see Fig. 1).
13. The collectors of the IGBTs are connected to the driver for monitoring the collector-emitter voltage V_{CE}. V_{CEmax} = 1600 V. When paralleling modules, external resistors R_{cx} should be mounted on an additional board near to the modules.

B. Description of the Circuit Block Diagram

The circuit block diagram (Fig. 1) shows the input on the left and the output on the right.

The input side comprises the following components:

1. Input Schmitt trigger, CMOS compatible

In the "F" version we have the necessary optic input buffers respectively ERROR output circuit, to perform the optical and electrical signals.

2. Interlock circuit

The interlock circuit prevents the IGBT turning on before the gate charge of the other IGBT is completely discharged.

3. Short pulse suppression

The short pulse suppression makes sure that only adequate trigger pulses are transmitted to the output flip-flop.

4. Error monitoring

This circuit monitors pulses fed backwards via the pulse transformers.

5. Inhibit pulse generator

In the error monitoring circuit, an inhibit pulse generator discriminates between switching and error signals. After any positive switching pulse edge the error monitoring function is enabled. This is required since the pulse transformer causes a negative peak voltage on its primary during re-magnetization. This peak voltage would trigger the error monitoring without the inhibit pulse.

6. Error memory

The error memory is triggered by the error monitoring circuit. The error memory blocks the turn-on pulses to both IGBTs simultaneously. Resetting is only possible when no pulses from the error monitoring are present and both inputs are zero. The output signal is fed to a terminal which is to be connected to the control circuit (open-collector-transistor SKHI 26 W). An external pull-up-resistor have to be provided on customers control board.

7. DC/DC-Converter

It is the primary side control of the DC/DC converter for transmitting the control power to the IGBTs.

8. Power supply monitoring

The supply voltage V_S is monitored for its minimum value of 13 V. If it falls below this value an error is monitored and the turn-on pulses for the IGBTs are blocked.

At initial switch-on the input pulses may only be released more than 4 μ s after the instant when V_S has reached its nominal value of 15 V.

The output comprises two drivers with the following components:

9. Pulse transformer

It transmits the turn-on and turn-off signals for the IGBT. In the reverse direction the error signal from the V_{CE} monitoring is transmitted via the same transformer.

10. Power supply transformer for the DC/DC converter

11. Rectifier for the auxiliary power supply

12. Flip-flop

The flip-flop is pulse width triggered and is insensitive to spurious pulses and high dv/dt values.

13. Drivers

The output transistors of the power drivers are MOS-FETs.

14. Reverse drivers for the pulse transformers

They transmit the signals from the V_{CE} monitoring to the pulse transformers.

15. V_{CE} monitoring

It monitors the collector-emitter voltage V_{CE} of the IGBT during its on-state. V_{CE} is limited internally to 10 V (see fig. 4).

If the reference voltage V_{Ceref} is exceeded, the output signal switches to zero. V_{Ceref} is dynamic. Immediately

after turn-on of the IGBT a higher value is effective than in the steady state. When the IGBT is turned off, V_{Ceref} is set to this higher value by the signal "reset". The steady-state value V_{CEstat} of V_{Ceref} is set for standard IGBT (1200 V) values and has a typical value of 5,2 V.

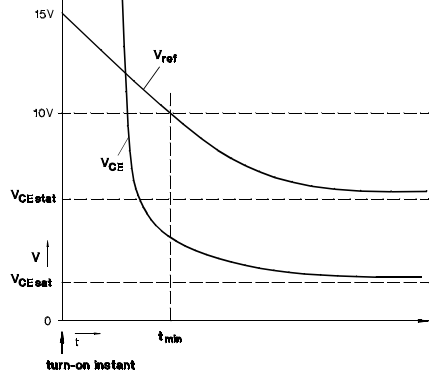


Fig.4 Waveform of the reference voltage V_{Ceref} of the V_{CE} monitoring immediately after the turn-on signal for the IGBT. A possible waveform of V_{CE} is shown. V_{CE} is internally clamped to 10 V.

C. Application / Handling

1. The CMOS inputs of the driver are extremely sensitive to overvoltage. Voltages higher than ($V_S + 0,3$ V) or under - 0,3 V may destroy these inputs.

Therefore the following safety requirements are to be observed:

- To make sure that the control signals do not comprise overvoltages exceeding the above values.
- Protection against static discharges during handling. As long as the driver is not completely assembled the input terminals must be short circuited. Persons working with CMOS devices should wear a grounded bracelet. Any floor coverings must not be statically chargeable. For transportation the input terminals must be short circuited using, for example, conductive rubber. Places of work must be grounded.

The same safety requirements apply to the IGBTs.

2. The connecting leads between the driver and the power module must be as short as possible.

For IGBT the leads should be twisted.

3. Any parasitic inductances should be minimized. Over-voltages may be damped by C or RCD snubber net-orks between the main terminals of the power module.
4. When first operating a newly developed circuit, low collector voltage and load current should be used in the

beginning, and these values should be increased gradually, observing the turn-off behaviour of the freewheeling diodes and the turn-off voltage spikes across the IGBT by means of the oscilloscope. Further the case temperature of the power module should be monitored.

When the circuit works correctly, short circuit tests can be made, starting again with low collector voltage.

5. It is important to feed any errors back to the control circuit and to switch the equipment off immediately in such events. Repeated turn-on of the IGBT into a short