SKY12334-362LF: GaAs 5 Bit Digital Attenuator, 5-Bits, 0.5 dB LSB with Serial-to-Parallel Driver 0.7–4 GHz

Features

- Broadband 700 MHz to 4 GHz
- Attenuation range: 15.5 dB
- Least significant bit attenuation: 0.5 dB
- Low insertion loss: 1 dB @ 900 MHz
- Positive voltage operation (5 V)
- Integrated silicon serial-to-parallel driver
- QFN 4 x 4 mm leadless package
- Available lead (Pb)-free, RoHS-compliant, and Green™, MSL-1 @ 260 °C per JEDEC J-STD-020
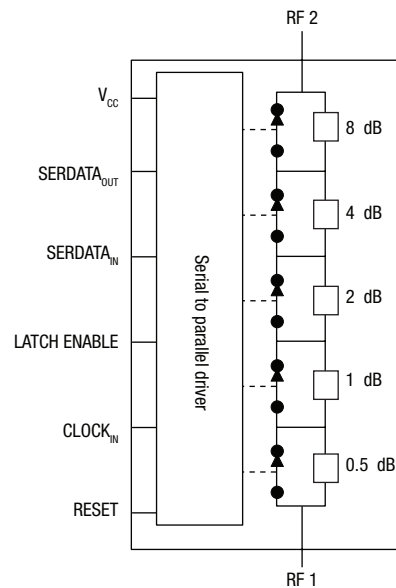
Description

The SKY12334-362LF is a GaAs FET IC 5-bit digital attenuator with a Si serial-to-parallel driver packaged in a 24-pin leadless exposed pad plastic package. It is particularly well suited for applications in which high attenuation accuracy, low insertion loss, and low inter-modulation products are required. Typical applications include base station, wireless and wireless local loop gain control circuits.

NEW Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

Functional Diagram

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Electrical Specifications

V_{CC} = 3–5 V, V_{CTL} = 0/3 V, 5 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_0 = 50 Ω, unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Insertion loss		0.7–1.4 GHz		1.2	1.5	dB
		1.4–2.3 GHz		1.3	2.0	dB
		2.3–2.7 GHz		1.8	2.3	dB
		2.7–4.0 GHz		2.0	2.7	dB
Attenuation range				15.5		dB
Attenuation accuracy	Attenuation referred to insertion loss	0.7–0.9 GHz	± (0.5 + 5% of Atten. Setting) Max.			dB
	All attenuation states	0.9–2.2 GHz	± (0.3 + 4% of Atten. Setting) Max.			dB
		2.2–4.0 GHz	± (0.5 + 5% of Atten. Setting) Max.			dB
Return loss	RF1 and RF2, all atten. states	0.7–1.4 GHz	12	14		dB
		1.4–2.3 GHz	15	18		dB
		2.3–2.7 GHz	12	15		dB
		2.7–4.0 GHz	10	13		dB

Operating Characteristics

V_{CC} = 3–5 V, V_{CTL} = 0/3 V, 5 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_0 = 50 Ω, unless otherwise noted

Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching characteristics: On/rise time Off/fall time	50% V_{CTL} to 90% RF or 10/90% RF 50% V_{CTL} to 10% RF or 90/10% RF			1200 500		ns ns
Input power for 0.1 dB compression	V_{CC} = V_{CTL} = 5 V V_{CC} = V_{CTL} = 3 V	0.7–3.8 GHz 0.7–3.8 GHz		25 23		dBm dBm
Input power for 1.0 dB compression	V_{CC} = V_{CTL} = 5 V V_{CC} = V_{CTL} = 3 V	0.7–3.8 GHz 0.7–3.8 GHz		32 30		dBm dBm
Input Intermodulation Intercept Point (IIP3)	For two tone input power, 0 dBm/tone, 1 MHz spacing. V_{CC} = V_{CTL} = 5 V V_{CC} = V_{CTL} = 3 V	0.7–3.8 GHz 0.7–3.8 GHz		42 42		dBm dBm

DC Characteristics

Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Input voltage high		$V_{IH}(1)$ V_{CC} = +3 V V_{CC} = +5 V	2.3 3.5		3 5	V V
Input voltage low		$V_{IL}(0)$ V_{CC} = +3 V V_{CC} = +5 V	0 0		1.0 1.5	V V
Input leakage current		I_L		0.5		μA
Quiescent current		I_{CC}		500		μA
Supply voltages (V_{CC})		V_{CC}	3	5	5.5	V

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Absolute Maximum Ratings

Characteristic	Value
RF input power @ 5 V	30 dBm
Supply voltage (V_{CC})	6 V
Control voltage	-0.2 V, +8 V
Operating temperature	-40 °C to +85 °C
Storage temperature	-65 °C to +150 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

Electrical Specifications

V_{CC} = 5 V, V_{CTL} = 0/5 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_0 = 50 Ω, C_{BLK} = 47 pF unless otherwise noted
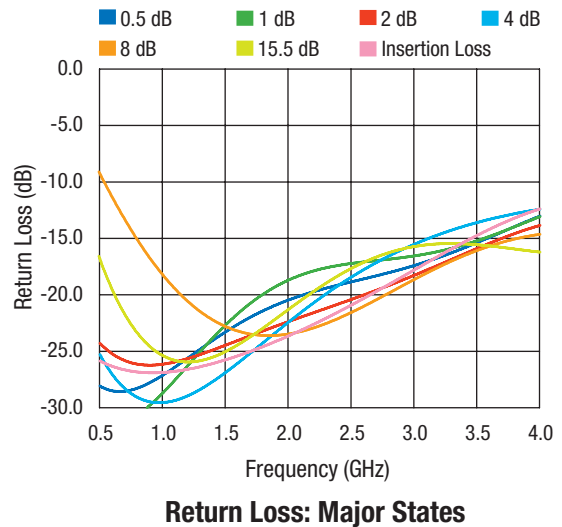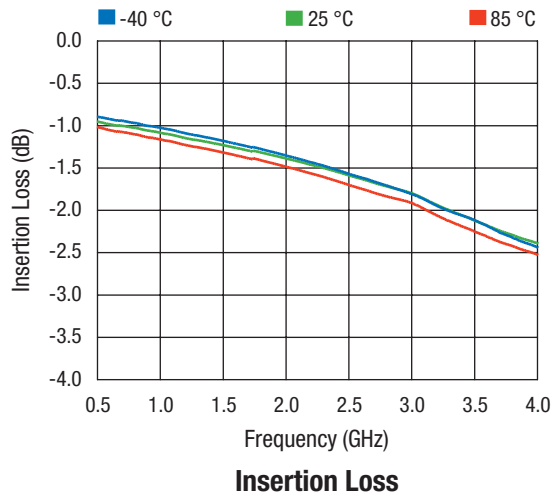
Insertion Loss

Return Loss: Major States

Electrical Specifications

V_{CC} = 5 V, V_{CTL} = 0/5 V, T = 25 °C, P_{INPUT} = 0 dBm, Z_O = 50 Ω, C_{BLK} = 47 pF unless otherwise noted
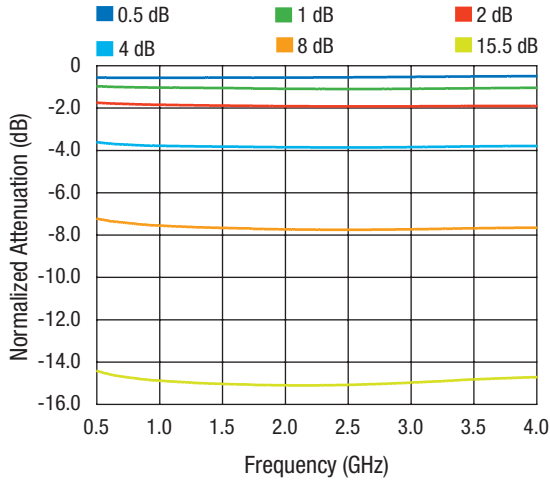
Normalized Attenuation: Major States

Attenuation Bit Error vs. Attenuation State
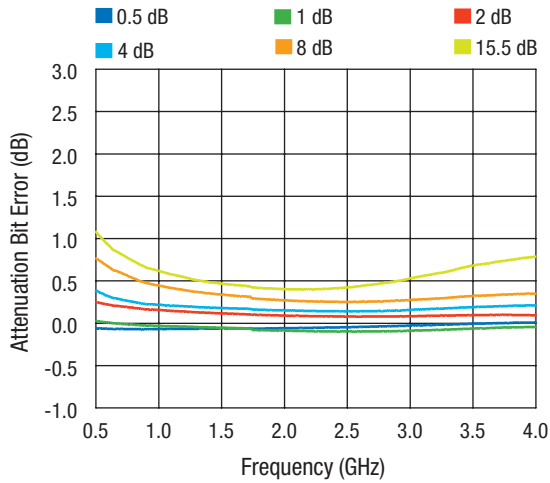
Attenuation Bit Error: Major States

Relative Phase: Major States
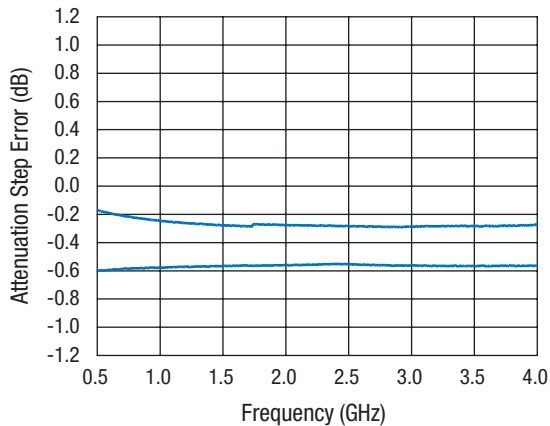
**Worst Case Attenuation Step Error
Between Successive Attenuation States**

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Pin Out (Top View)
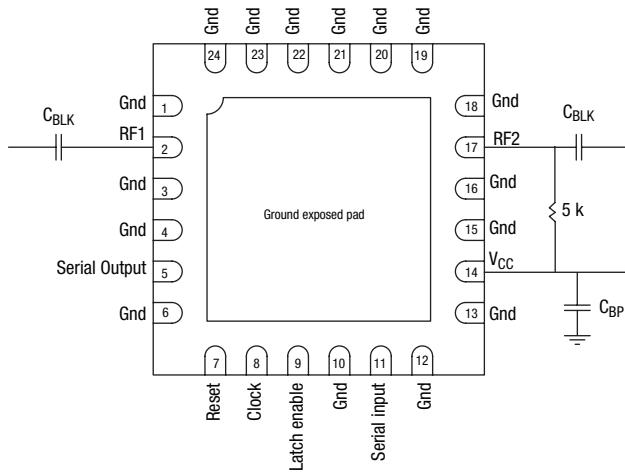
DC blocking caps required on RF1 and RF2 ports.
Recommend 47 to 300 pF.
RF2 or RF1 ports needs to be pulled up to V_{CC} voltage.
Recommend 5 kΩ.
$C_{BP} = C_{BYPASS} = 0.01 \mu F$.

Truth Table

Reset	Serial Data Input					RF In/Out Attenuation
	8 dB	4 dB	2 dB	1 dB	0.5 dB	
1	1	1	1	1	1	Insertion Loss
1	1	1	1	1	0	0.5 dB
1	1	1	1	0	1	1 dB
1	1	1	0	1	1	2 dB
1	1	0	1	1	1	4 dB
1	0	1	1	1	1	8 dB
1	0	0	0	0	0	15.5 dB
0	X	X	X	X	X	15.5 dB

V_{CC} = 5 V
"0" = 0–0.5 V
"1" = 3.5–5 V
"X" = Don't Care

V_{CC} = 3 V
"0" = 0–0.5 V
"1" = 2.3–3 V
"X" = Don't Care

Pin Table

Pin #	Name	Description
1	Gnd	Ground
2	RF1	RF input/output must be DC blocked
3	Gnd	Ground
4	Gnd	Ground
5	Serial output	Data input delayed by 8 clock cycles
6	Gnd	Ground
7	Reset	Reset clears shift registers
8	Clock	Serial clock input
9	Latch enable	On rising edge of pulse, shifts 5 most recent bits clocked in to set attenuation state
10	Gnd	Ground
11	Serial input	input data
12	Gnd	Ground
13	Gnd	Ground
14	V_{CC}	Fixed bias for SPI
15	Gnd	Ground
16	Gnd	Ground
17	RF2	RF input/output must be DC blocked
18	Gnd	Ground
19	Gnd	Ground
20	Gnd	Ground
21	Gnd	Ground
22	Gnd	Ground
23	Gnd	Ground
24	Gnd	Ground
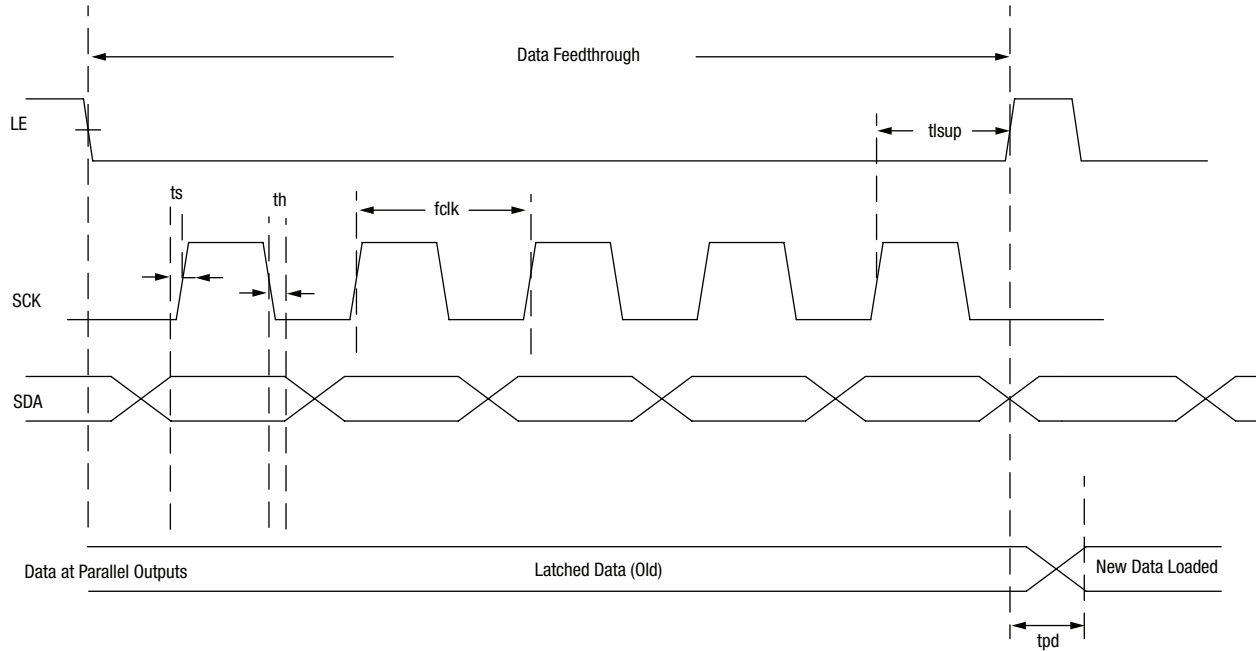
Parameter	Symbol	V_{CC} = 5 V			V_{CC} = 3 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Serial input setup time	ts		5			5		ns
Hold time from serial input to shift clock	th		5			5		ns
Setup time from shift clock to latch enable	tlsup	40			100			ns
Propagation delay, latch enable to C0.5 through C8	tpd			30			70	ns
Setup time from reset to shift clock	-	20			50			ns
Clock freq	fclk			30			10	MHz

Latch Enable	Clock	Reset	Function
X	X	L	Shift register cleared
X	→	H	Shift register clocked
→	X	H	Contents of shift register transferred to digital attenuator

Serial data (SDA) is shifted into the register on the rising edge of the clock (SCK), least significant bit (LSB) first. The attenuator will change states on the rising edge of the latch enable (LE) signal, according to the most recent 5 bits of shifted data accepted since the previous falling edge of the LE signal.

The part includes a serial data output pin that can be used to provide the serial data input to a cascaded attenuator. The serial data output is the serial input data delayed by 8 clock cycles.

Power-up sequence:

0. Connect ground

1. Apply V_{CC}

2. Set all inputs (SCK, SDA, LE)

Power-down sequence should be the reverse of above.

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Example for Setting 0.5 dB State

CLK_S = 30MHz, VDD = +5V, TnTp, 27C
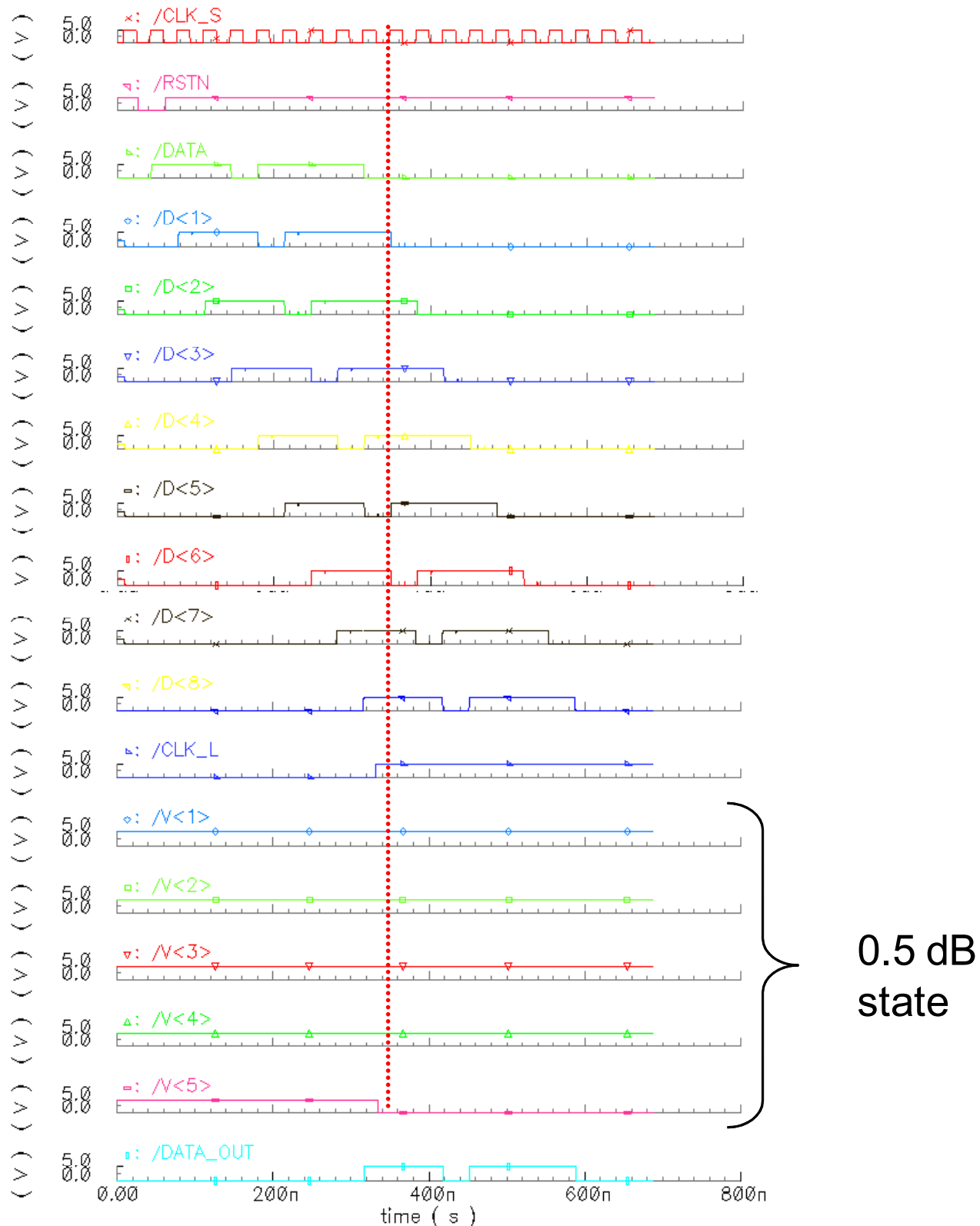
Evaluation Circuit Board

SK41092-1 REV1
ATTENUATOR TEST BOARD
RF1   RF2
C1   C2
SMA
-362
4MM X 4MM QFN
SDO RST CLK LE SDI VCC
SMA
A   A
R1
C3
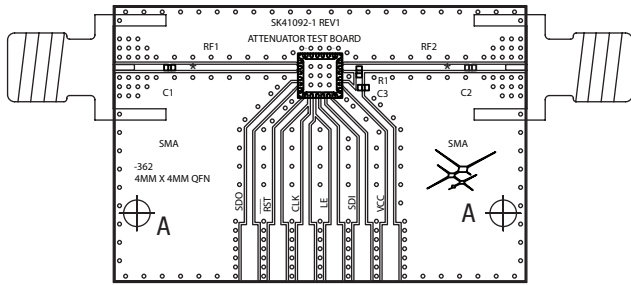
C1 = C2 = 47–300 pF.
C3 = 0.01 µF.
R1 = 5k Ω.

Park Marking

Pin 1
Indicator

Pin 24

Pin 1

S2334
XXXX
YWW

Skyworks P/N

Lot #

Date Code
Y= Calender Year
WW= Week

Top View

Pin 24

Pin 1

Exposed Pad

Bottom View

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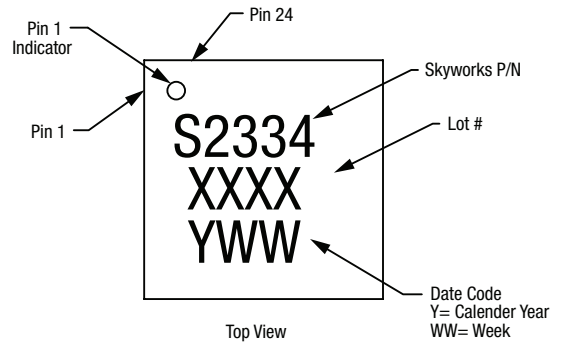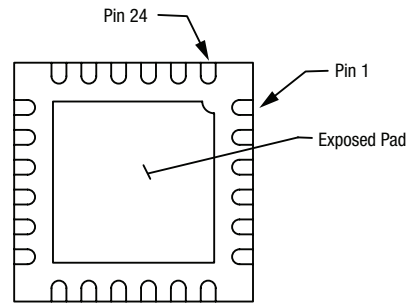
-362 QFN 4 x 4 mm 24-Lead Outline

0.008 Ref.
(0.20 mm)
Seating Plane

0.02 mm + 0.03 mm
0.02 mm - 0.02 mm

Pin 1
Indicator

0.157 (4 mm)

0.157 (4 mm)

24X

0.035 (0.90 mm) ± 0.004 (0.10 mm)

0.106 (2.70 mm) + 0.004 (0.10 mm)
0.106 (2.70 mm) - 0.006 (0.15 mm)

Exposed Pad

See Detail A

0.106 (2.70 mm)
+ 0.004 (0.10 mm)
0.106 (2.70 mm)
- 0.006 (0.15 mm)

0.098
(2.500 mm)

Detail C

Detail B
4 Places

0.098
(2.500 mm)

R0.20

0.014 (0.35 mm)
± 0.004 (0.10 mm)

0.25 mm + 0.05 mm
0.25 mm - 0.07 mm

Detail A

Detail C

0.019 (0.5 mm)

0.0100 (0.25 mm)

C_L

Detail B

1. Dimensioning and tolerancing per ASME Y14.5m - 1994.
2. Dimensions are in inches and (millimeters). Controlling
   dimension is millimeters.
3. Coplanarity applies to the exposed heat sink slug
   as well as the terminals.
4. Plating requirement per source control drawing (SCD) 2504.

-362 QFN 4 x 4 mm 24-Lead Suggested Land Pattern

1.60
(To Metal Pads)

R0.20

0.50

0.25

4x Plated Thru Vias

See Detail A

Metal Gnd Pad (Sq.) 2.70

0.25

0.60

Exposed
Soldering
Area

Detail A
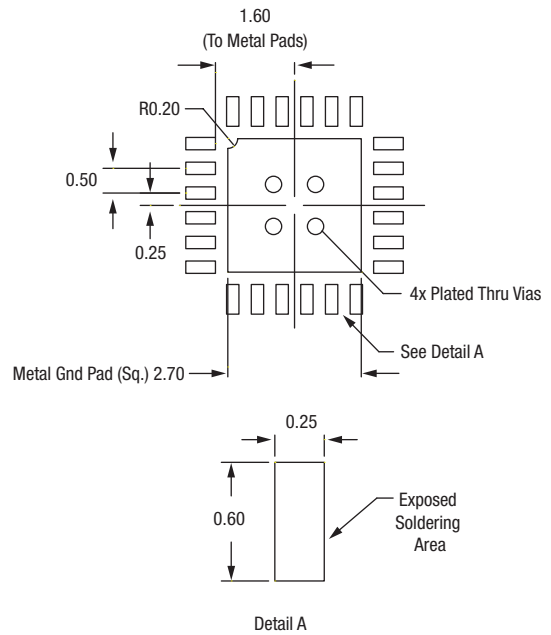
Recommended Solder Reflow Profiles

Refer to the *"Solder Reflow Information"* Application Note, document number 200164.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note, document number 200083.

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