SKY65050-372LF: Low Noise Transistor

Applications

- Wireless infrastructure: WLAN, WiMAX, broadband, cellular base stations
- Test instrumentation
- LNA for GPS receiver
- Satellite receivers

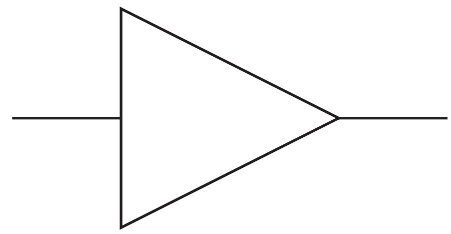


Figure 1. Functional Block Diagram

Features

- 850–6000 MHz frequency of operation
- Noise figure of 0.4 dB at 2.4 GHz
- Noise figure of 0.4 dB at 2.0 GHz
- Gain of 14 dB at 2.4 GHz
- Gain of 16 dB at 2.0 GHz
- OIP3 of 20 dBm at 2.4 GHz
- $P_{1\ dB}$ of 8 dBm at 2.4 GHz
- Single DC supply
- Operating current of 16 mA
- Small footprint 4-lead SC-70 package, lead (Pb)-free, RoHS-compliant, and Green™

Description

The SKY65050-372LF is a high performance, low noise, n-channel, depletion mode pHEMT, fabricated from Skyworks advanced pHEMT process and packaged in a miniature 4-lead SC-70 package. The transistor's low noise figure, high gain and excellent third order intercept (IP3) allows this transistor to be used in various receiver and transmitter applications.

The SKY65050-372LF is lead (Pb)-free, RoHS-compliant, and Green™.

NEW

Skyworks Green™ products are RoHS (Restriction of Hazardous Substances)-compliant, conform to the EIA/EICTA/JEITA Joint Industry Guide (JIG) Level A guidelines, are halogen free according to IEC-61249-2-21, and contain <1,000 ppm antimony trioxide in polymeric materials.

Operating Characteristics

$T = 25\ °C$, $Z_0 = 50\ \Omega$, $V_{DD} = 2\ V$, $I_{DD} = 16\ mA$, parameters include matching network optimized for noise, unless otherwise noted

Parameter	Symbol	Condition	Frequency	Min.	Typ.	Max.	Unit
Saturated drain current	I_{DSS}	$V_{DS} = 2\ V$, $V_{GS} = 0\ V$		40	55	70	mA
Pinchoff voltage	V_P	$V_{DS} = 2\ V$, $I_{DS} = 2.5\%$ of I_{DSS}		-0.95	-0.8	-0.65	V
Transconductance	g_m	$V_{DS} = 2\ V$, $g_m = \Delta I_{DS} / \Delta V_{GS}$, measured at $I_{DS} = 20\%\ I_{DSS}$		40	80	120	mS
Gate leakage current	I_{GSS}	$V_{GD} = V_{GS} = -3\ V$			1	200	µA
Noise figure(1)	NF		2.4 GHz 2.0 GHz		0.4 0.4	0.85	dB dB
Associated gain $\|S_{21}\|$	G_A		2.4 GHz 2.0 GHz	12	14 16	16	dB dB
Output third order intercept point	OIP3	$P_{OUT} = -10$ dBm/tone $\Delta F = 1$ MHz	2.4 GHz		20		dBm
Output 1 dB compression point	$OP_{1\ dB}$		2.4 GHz		8		dBm
Input return loss	$\|S_{11}\|$		2.4 GHz		-8		dB
Output return loss	$\|S_{22}\|$		2.4 GHz		-12		dB
Reverse isolation	$\|S_{12}\|$		2.4 GHz		-27		dB

1. Input RF connector and matching network loss de-embedded from measurement.

Absolute Maximum Ratings ($T_A = 25\ °C$)

Characteristic	Value
Drain source voltage (V_{DS})	6 V
Gate-source voltage (V_{GS})	-5 V
Gate-drain voltage (V_{GD})	-5 V
Drain current (I_{DS})	55 mA
Gate current (I_{GS})	100 µA
Power dissipation (P_{DISS})	240 mW
Channel temperature (T_{CHAN})	150 ºC
Storage temperature range (T_{ST})	-65 °C to +125 °C
Operating temperature range (T_{OP})	-40 °C to +85 °C
Thermal resistance (θ_{JC})	TBD ºC/W

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

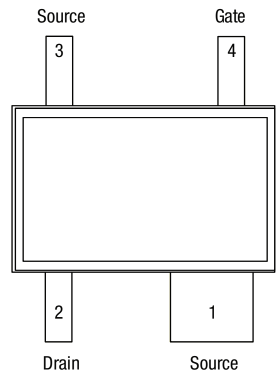


Figure 2. 4-Lead SC-70 Package and Pin Out

Table 1. Pin Description and Function

Pin No.	Pin Name	Description
2	Drain	RF output of transistor, requires external matching network for optimum performance. Supply voltage required through external RF choke.
1, 3	Source	Source lead of transistor, provides DC self biasing point and AC ground.
4	Gate	RF input of transistor, requires external matching network for optimum performance.

Typical Performance Data

V_{DD} = 2 V, Z_0 = 50 Ω, I_{DD} = 16 mA, T = 25 °C, includes 2.4 GHz matching network, unless otherwise noted

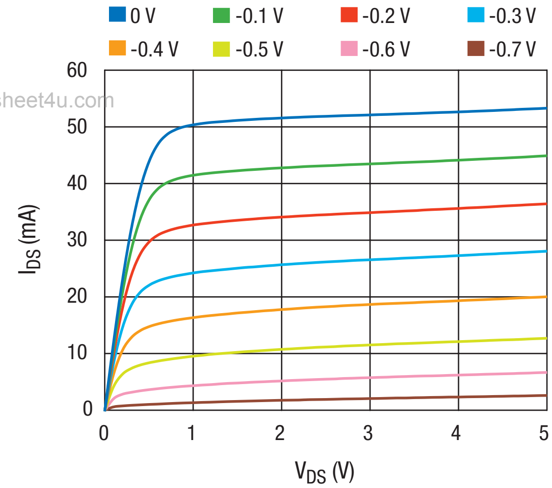


Figure 3. Typical IV Curves

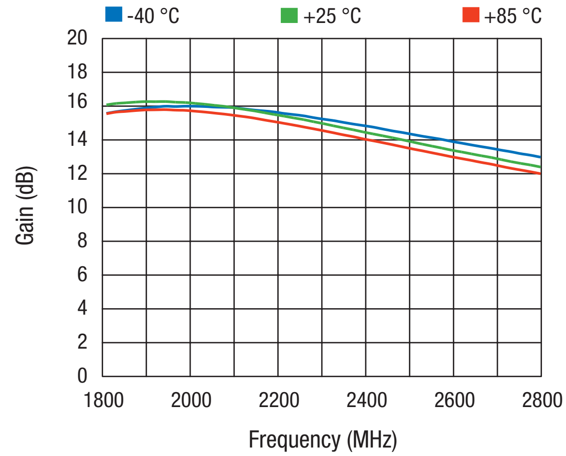


Figure 4. Small Signal Gain vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm

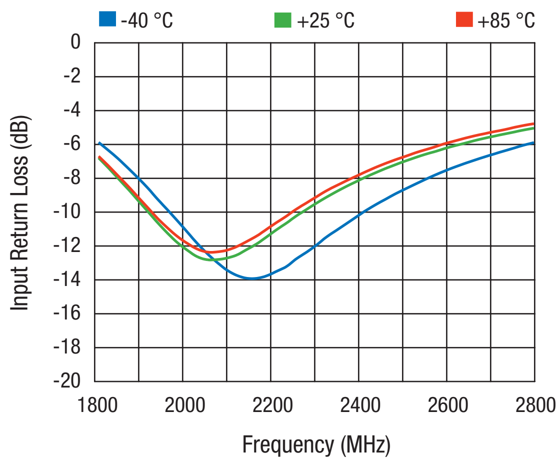


Figure 5. Input Return Loss vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm

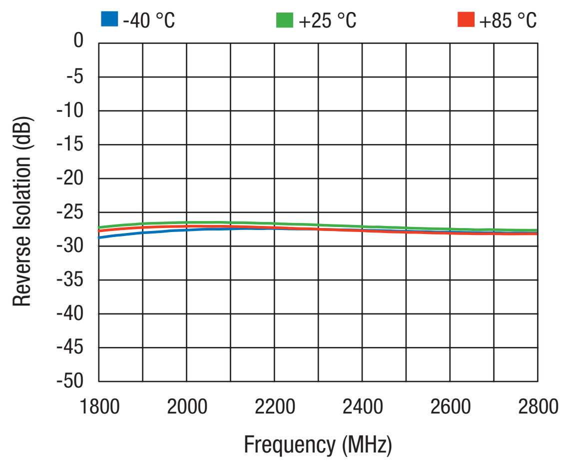


Figure 6. Reverse Isolation vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm

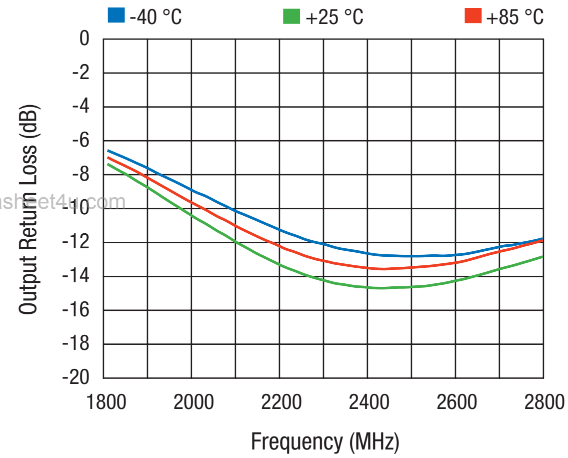


Figure 7. Output Return Loss vs. Frequency for Multiple Temperatures, P_{IN} = -20 dBm

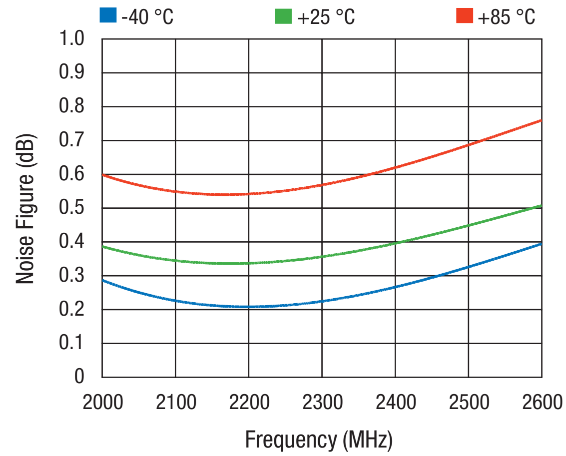


Figure 8. Noise Figure vs. Frequency for Multiple Temperatures, Input RF Connector and Matching Network Loss De-embedded from Measurement

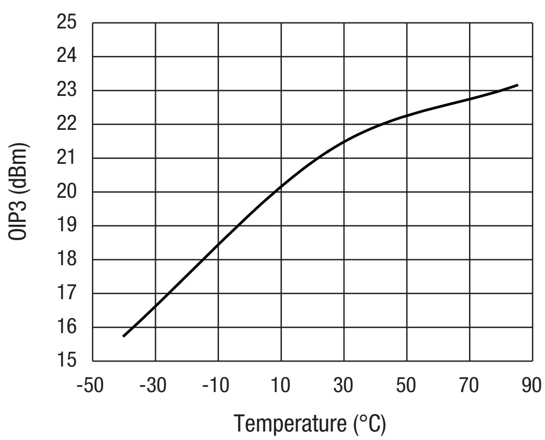


Figure 9. OIP3 vs. Temperature, F = 2.4 GHz, P_{IN} = -24 dBm/Tone, ΔF = 1 MHz

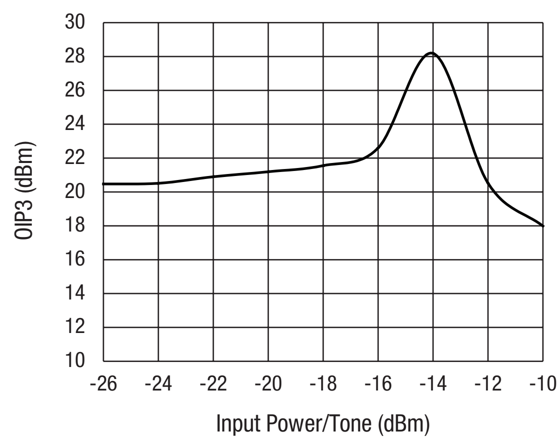


Figure 10. OIP3 vs. P_{IN}/Tone, F = 2.4 GHz, ΔF = 1 MHz

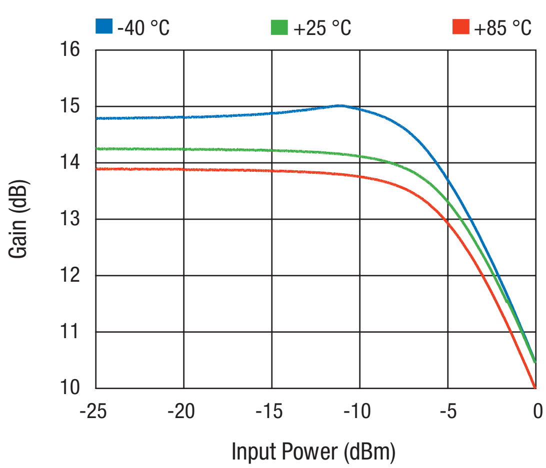


Figure 11. Gain vs. Input Power for Multiple Temperatures, F = 2.4 GHz

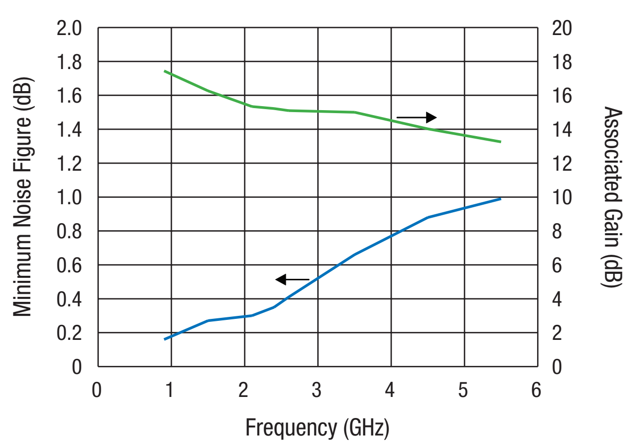


Figure 12. Minimum Noise Figure and Associated Gain vs. Frequency

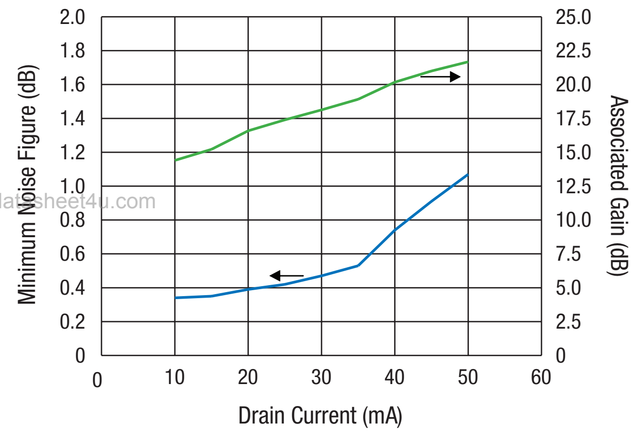


Figure 13. Minimum Noise Figure and Associated Gain vs. Drain Current

Introduction

The SKY65050-372 is a depletion mode PHEMT designed for low noise, high frequency applications. The SKY65050-372 has a typical noise figure of 0.65 dB tested at the 2.4 GHz wireless LAN frequency band. A gain of 14 dB typical is achieved using the same circuit. If the frequency of operation is lowered to the 1 GHz range, noise figure performance of the device can approach 0.5 dB.

De-embedded scattering and noise parameters are provided in addition to typical circuit topologies for commonly used frequency bands. With an appropriate circuit, the SKY65050-372 can be used for any application from 850 MHz up to 6 GHz. The SC-70 4-lead package makes the SKY65050-372 an ideal low noise and low cost solution.

Biasing

To properly bias a depletion mode PHEMT, both the gate and drain of the device must be biased properly. At V_{GS} = 0 V and V_{DS} $\geq$ 2 V, the device is in its saturated state and will draw the maximum amount of current, I_{DSS}. Typically, the device achieves the best noise performance at V_{DS} = 3 V and I_{DS} = 15 mA. In order to control I_{DS}, V_{GS} must be biased with a negative voltage supply.

To eliminate the need of a negative DC supply, self-biasing should be used where a resistor is placed between one of the source leads and ground. A bypass capacitor should be placed in parallel to this resistor to provide a RF ground and to ensure performance at the operating frequency remains unchanged. When current flows from drain to source and through the resistor, the source voltage becomes biased above DC ground. The gate pin of the device should be left unbiased at 0 V, thus creating the desired negative V_{GS} value. This largely simplifies the design by eliminating the need for a second DC supply. Table 2 contains resistor values to bias the SKY65050-372 properly.

Table 2. Self-Bias Resistance

Resistor Value (Ω)	Drain Current (mA)
47	10
27	15
20	20
15	25
10	30

RF Matching Networks

The circuit schematic in Figure 14 shows the recommended RF matching network used for the 2.4 GHz wireless LAN frequency band. De-embedded s and noise parameters were used to design this network. This circuit was primarily tuned for gain, noise figure, and input and output return loss while maintaining proper stability.

Optimal noise performance is attained when the impedance presented to the input of the amplifier is equal to its NFMIN impedance point. Components C1, L1, and L2 provide the necessary impedance match for noise figure and input return loss. Circuit board and input matching structure losses on the input of the amplifier add directly to the overall noise figure of the amplifier. It is critical to minimize RF trace lengths and to use high Q components to achieve optimal noise figure performance.

R1 and C2 provide self bias for the device as well as RF grounding for one of the two source lead. C7 is placed on the opposing source lead and is used to tune the transistor's internal source inductance. The effect of source inductance will vary with frequency. Too little source inductance will increase gain and high frequency stability, but at the cost of decreased in-band stability. Too much source inductance will decrease high frequency stability and gain, but increase in-band stability. It is very important to find the optimum tuning of source inductance that will balance all of these variables.

The output matching topology is typical for a RF amplifier. L3 is the RF choke that prevents RF signals from reaching the DC supply. C4 is the DC blocking capacitor. R2 is added for increased stability at the expense of decreased output power. This resistance can be increased from its nominal value of 180 to improve output power at the expense of broadband stability. Figure 15 shows a recommended layout.

Application notes, device models, S-parameters, and noise parameters are available at www.skyworksinc.com.

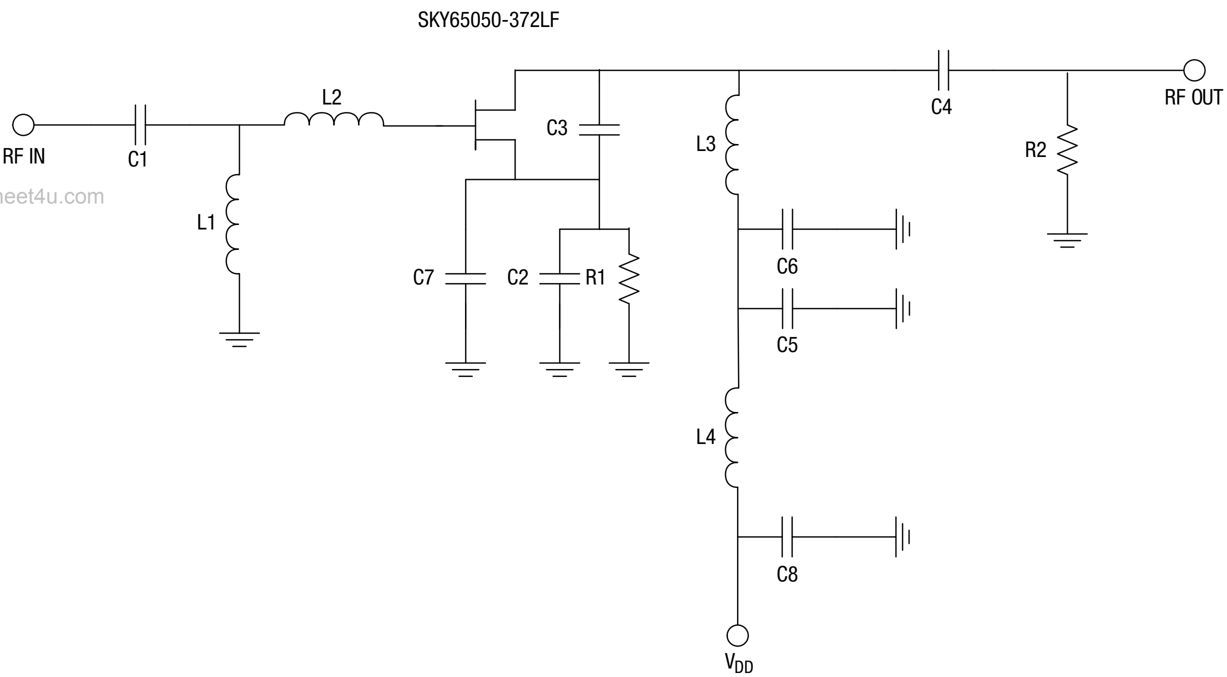


Figure 14. Evaluation Board Schematic

Table 3. Recommended Evaluation Board Components for 2.4 GHz

Component	Value	Size	Manufacturer	Part Number	Notes
C1	33 pF	0201	Johanson	250R05L330JV4SK	
C2	1000 pF	0201	Murata	GRM033R71E102KA01	
C3	0.5 pF	0201	Murata	GRM0335C1ER50C	
C4	15 pF	0201	Murata	GRM0335C1E150JD01	
C5	DNP	-	-		
C6	1000 pF	0201	Murata	GRM033R71E102KA01	
C7	1000 pF	0201	Murata	GRM033R71E102KA01	Place approx. 25 mils (0.635 mm) from pin 3
C8	1000 pF	0201	Murata	GRM033R71E102KA01	
L1	3.3 nH	0402	Coilcraft	0402CS-3N3XJL	
L2	1.8 nH	0402	Coilcraft	0402CS-1N8XJL	
L3	3.6 nH	0201	TDK	MLG0603S3N6C	
L4	27 nH	0201	TDK	MLG0603S27NJ	
R1	27 Ω	0201	Panasonic	ERJ1GEF27R0	
R2	180 Ω	0201	Panasonic	ERJ1GEF1800	

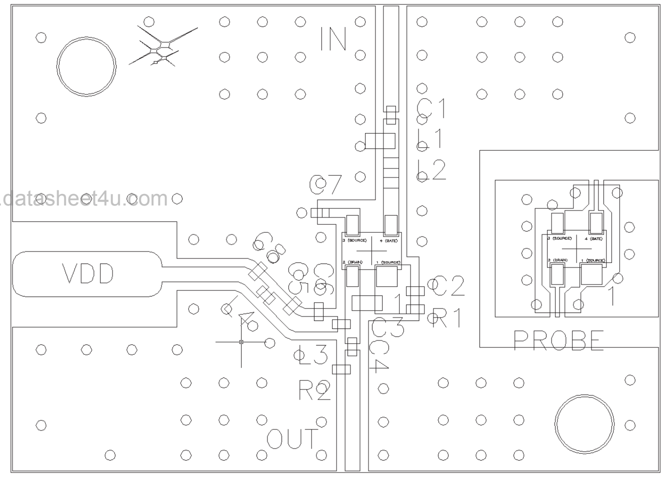
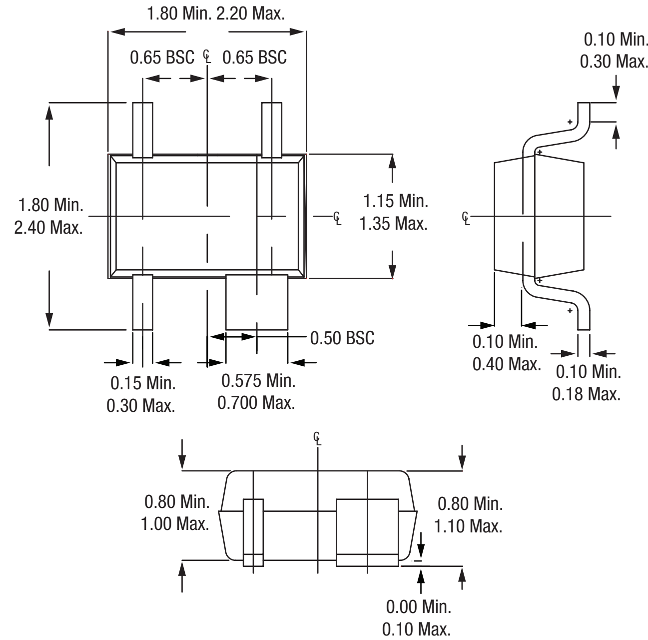


Figure 15. Evaluation Board Layout



All dimensions are in millimeters.
Dimensions are inclusive of plating.
Dimensions are exclusive of mold flash and metal burr.
All specifications comply to EIAJ SC70.

Figure 16. 4-Lead SC-70 Package Dimensions

Evaluation Board Desciption

The SKY65050-372 evaluation board allows the part to be fully exercised. The board is populated for 2.4 GHz operation and contains a separate probe footprint for general device testing or source and load pull characterization. The board is provisioned with two RF connectors and a 3 pin DC launch. RF connector and board loss up to component C1 is approximately 0.15 dB.

Board material is 10 mil thick Rogers 4350B with 1 oz. copper cladding. RF traces are 20 mils wide with 11 mil spacing to ground.

Evaluation Board Test Procedure

Step 1: Connect RF test equipment to amplifier input/output SMA connectors

Step 2: Connect DC ground.

Step 3: Connect VDD to a 2 V supply with a current limit of 60 mA. Verify that the board draws approximately 16 mA.

Step 4: Apply RF signal or noise source and verify performance detailed on page 4.

Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

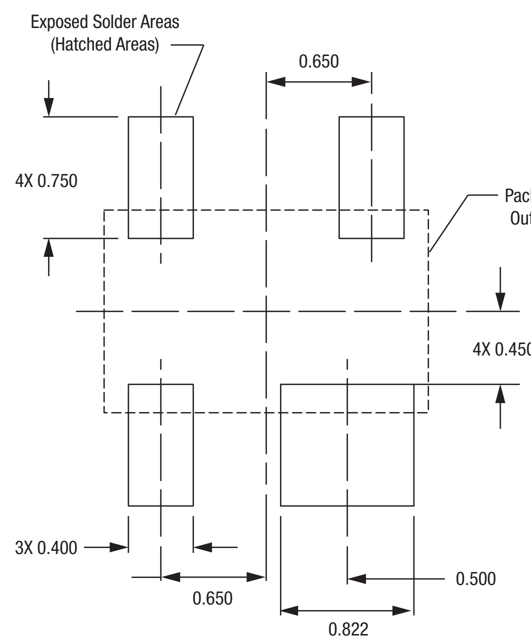


Figure 17. Land Pattern