

DATA SHEET

SKY67175-306LF: 1.5 to 3.8 GHz Two-Stage, High-Gain Low-Noise Amplifier

Applications

- LTE, GSM, WCDMA, HSDPA macro-base and micro-base stations
- L and S band ultra-low-noise receivers
- Cellular repeaters, small-cell, macro-cell, DAS, and RRH/RRUs
- High-temperature transceiver applications to +105 °C

Features

- Part of complete SDARS LNA reference design
- Ultra-low reference design NF: 0.64 dB @ 3.5 GHz
- High gain: 33 dB @ 3.5 GHz
- Low quiescent current: 115 mA
- Stage 1 and Stage 2 adjustable current
- Small QFN (16-pin, 4 x 4 mm) Pb-free package (MSL1, 260 °C per JEDEC J-STD-020)



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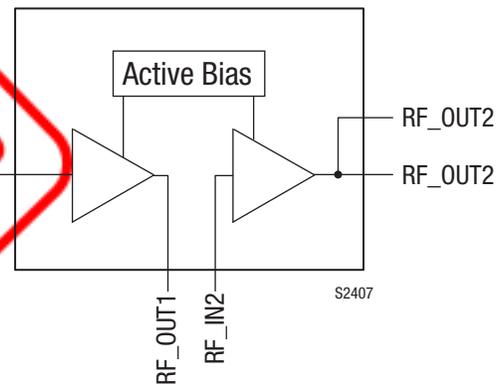
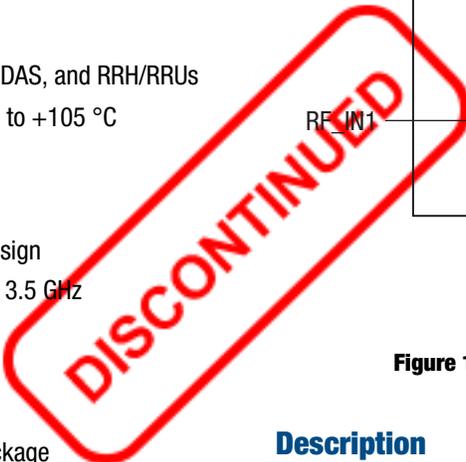


Figure 1. SKY67175-306LF Block Diagram

Description

The SKY67175-306LF is a two-stage, GaAs pHEMT low-noise amplifier (LNA) with active bias and high-linearity performance. The pHEMT front end of the device provides an ultra-low noise figure (NF) while the cascode output stage provides high gain, linearity, and efficiency.

With excellent thermal performance, the SKY67175-306LF is rated for operation up to +105 °C.

The SKY67175-306LF is provided in a 4 x 4 mm, 16-pin Quad Flat No-Lead (QFN) package. A functional block diagram is shown in Figure 1. The pin configuration and package are shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

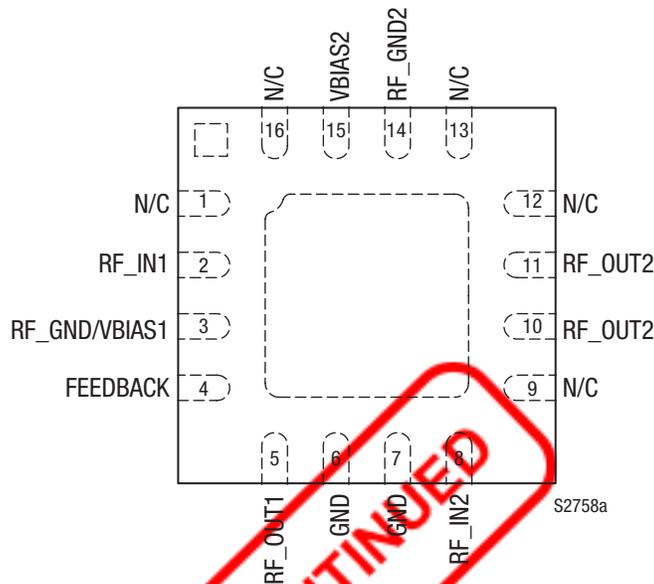


Figure 2. SKY67175-306LF Pinout (Top View)

Table 1. SKY67175-306LF Signal Descriptions

Pin	Name	Description	Pin	Name	Description
1	N/C	No connection. May be grounded with no change in performance.	9	N/C	No connection. May be grounded with no change in performance.
2	RF_IN1	RF input to first stage LNA	10	RF_OUT2	RF output of second stage amplifier
3	RF_GND/VBIAS1	AC ground for first stage bias circuit and bias voltage input that sets the first stage bias current.	11	RF_OUT2	RF output of second stage amplifier
4	FEEDBACK	Feedback pin. Leave open when not used. This feedback option is typically not used since it reduces gain.	12	N/C	No connection. May be grounded with no change in performance.
5	RF_OUT1	RF output of first stage LNA	13	N/C	No connection. May be grounded with no change in performance.
6	GND	Ground	14	RF_GND2	AC ground for second stage bias circuit
7	GND	Ground	15	VBIAS2	bias voltage input that sets the second stage bias current
8	RF_IN2	RF input to second stage amplifier	16	N/C	No connection. May be grounded with no change in performance.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY67175-306LF are provided in Table 2. Electrical specifications are provided in Table 3.

Typical performance characteristics of the SKY67175-306LF are illustrated in Figures 3 through 13.

Table 2. SKY67175-306LF Absolute Maximum Ratings¹

Parameter	Symbol	Minimum	Maximum	Units
Supply voltage	V _{DD}		6.0	V
RF input power	P _{IN}		+20	dBm
Operating temperature	T _{OP}	-40	+105	°C
Storage temperature	T _{STG}	-65	+125	°C
Junction temperature	T _J		+150	°C
Thermal resistance: Stage 1	Θ _{JC}		50	°C/W
Stage 2			65	°C/W
Electrostatic discharge:	ESD			
Charged Device Model (CDM), Class 4			1000	V
Human Body Model (HBM), Class 1A			250	V
Machine Model (MM), Class A			25	V

¹ Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD HANDLING: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.

Table 3. SKY67175-306LF Electrical Specifications¹

(V_{DD} = +5 V, T_{OP} = +25 °C, P_{IN} = -30 dBm, Optimized for 3.4 to 3.6 GHz Operation, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
RF Specifications						
Noise figure ²	NF	@ 3500 MHz		0.64	0.84	dB
Small signal gain	IS21I	@ 3500 MHz	30	33		dB
Input return loss	IS11I	@ 3500 MHz		17		dB
Output return loss	IS22I	@ 3500 MHz		18		dB
Reverse isolation	IS12I	@ 3500 MHz		48		dB
Third order input intercept point	IIP3	@ 3500 MHz, Δf = 1 MHz, P _{IN} = -30 dBm/tone	-3.5	+0.5		dBm
Third order output intercept point	OIP3	@ 3500 MHz, Δf = 1 MHz, P _{IN} = -30 dBm/tone	+29.5	+33.5		dBm
1 dB input compression point	IP1dB	@ 3500 MHz	-19.5	-16.5		dBm
1 dB output compression point	OP1dB	@ 3500 MHz	+13.5	+16.5		dBm
DC Specifications						
Supply voltage	V _{DD}			5		V
Quiescent current	I _{DD}	Set with external resistor		115		mA

¹ Performance is guaranteed only under the conditions listed in this table. Specifications are for the entire reference design including the interstage SAW filter and the output high pass filter.

² Noise figure has been de-embedded as 0.1 dB @ 3500 MHz for connector and board loss.

Typical Performance Characteristics

(VDD = +5 V, Top = +25 °C, PIN = -30 dBm, Reference Design Optimized for 3.4 to 3.6 GHz Operation, Unless Otherwise Noted)

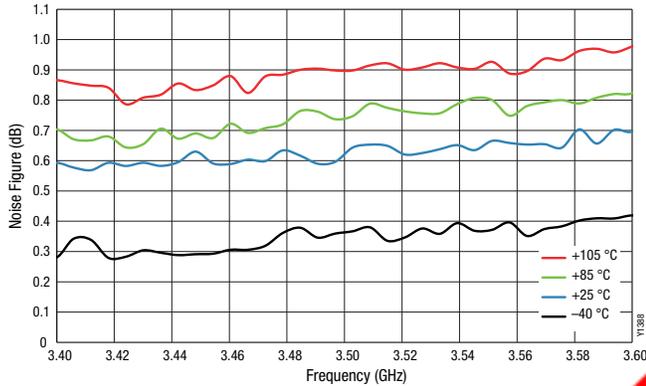


Figure 3. Noise Figure vs Frequency Over Temperature

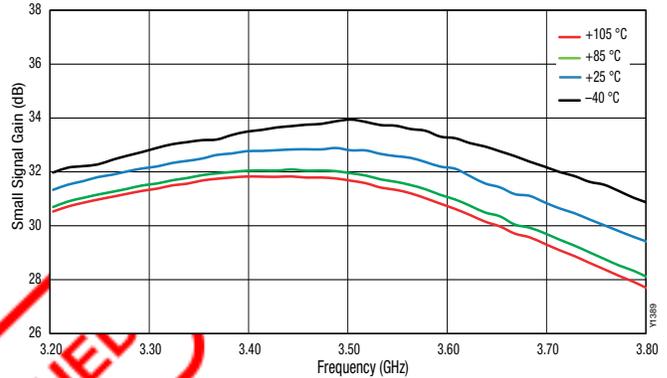


Figure 4. Small Signal Gain vs Frequency Over Temperature Narrow Band

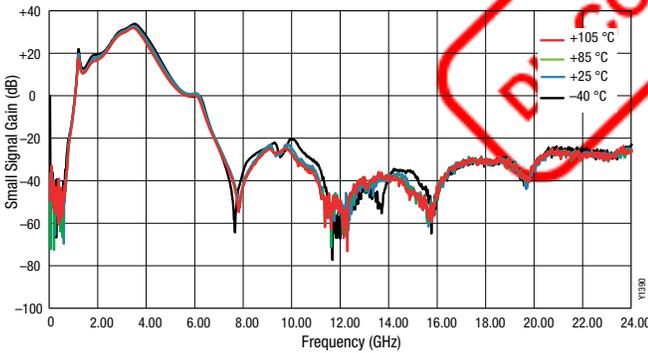


Figure 5. Small Signal Gain vs Frequency Over Temperature, Wide Band

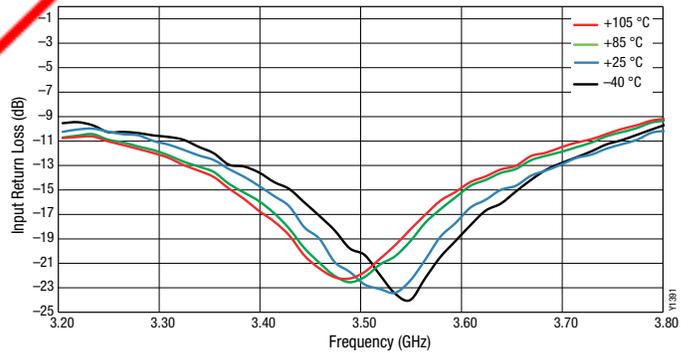


Figure 6. Input Return Loss vs Frequency Over Temperature, Narrow Band

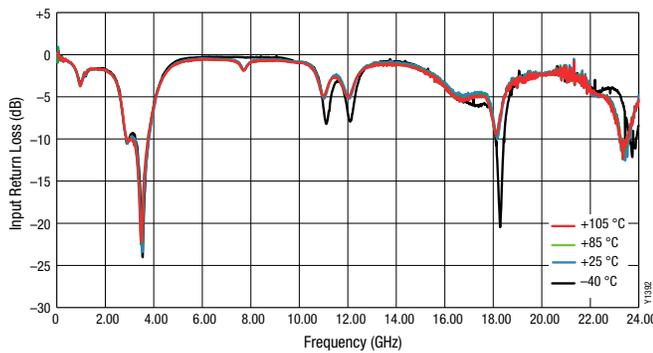


Figure 7. Input Return Loss vs Frequency Over Temperature, Wide Band

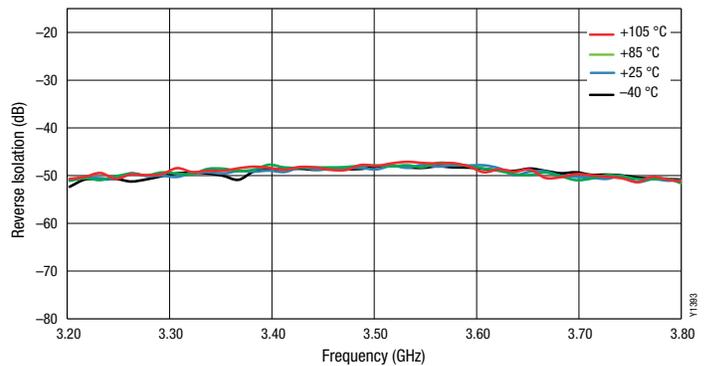


Figure 8. Reverse Isolation vs Frequency Over Temperature, Narrow Band

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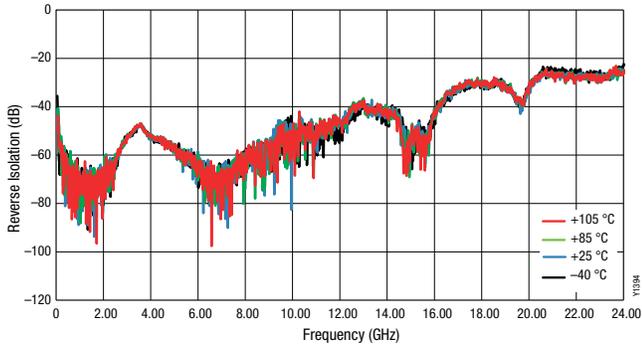


Figure 9. Reverse Isolation vs Frequency Over Temperature, Wide Band

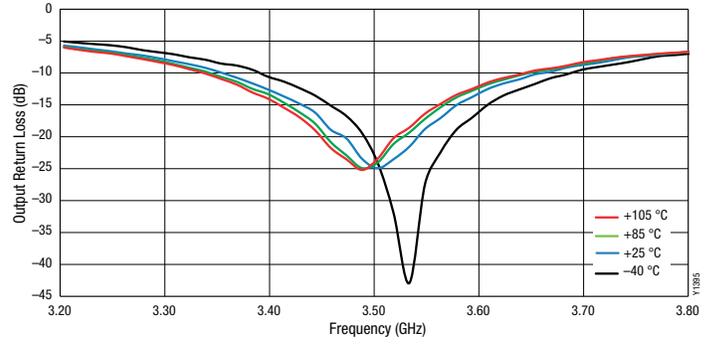


Figure 10. Output Return Loss vs Frequency Over Temperature, Narrow Band

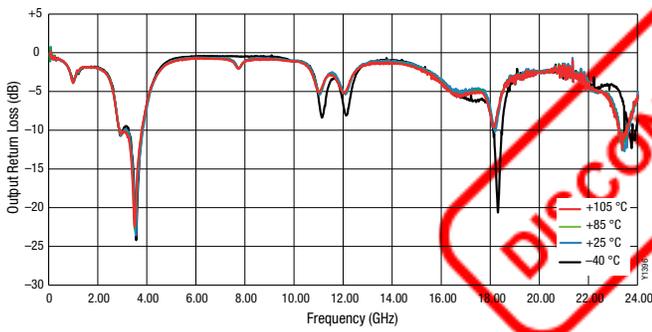


Figure 11. Output Return Loss vs Frequency Over Temperature, Wide Band

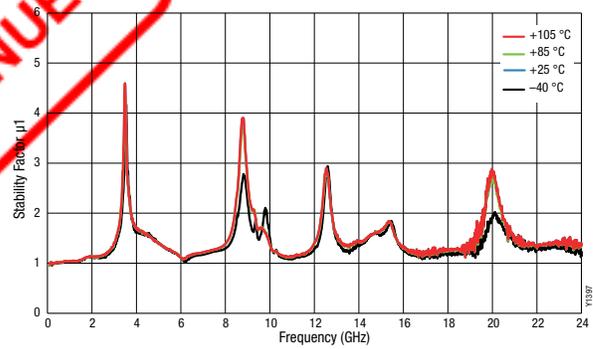


Figure 12. Stability Factor (μ_1) vs Frequency Over Temperature

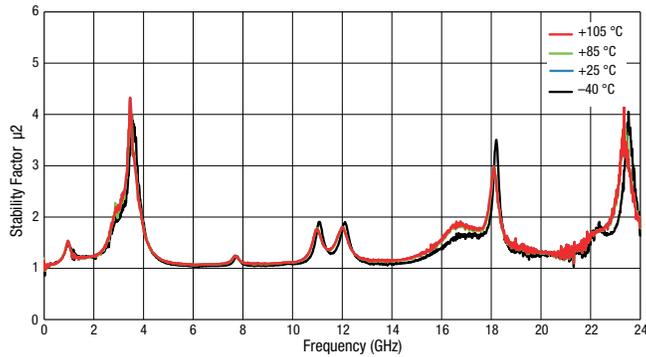


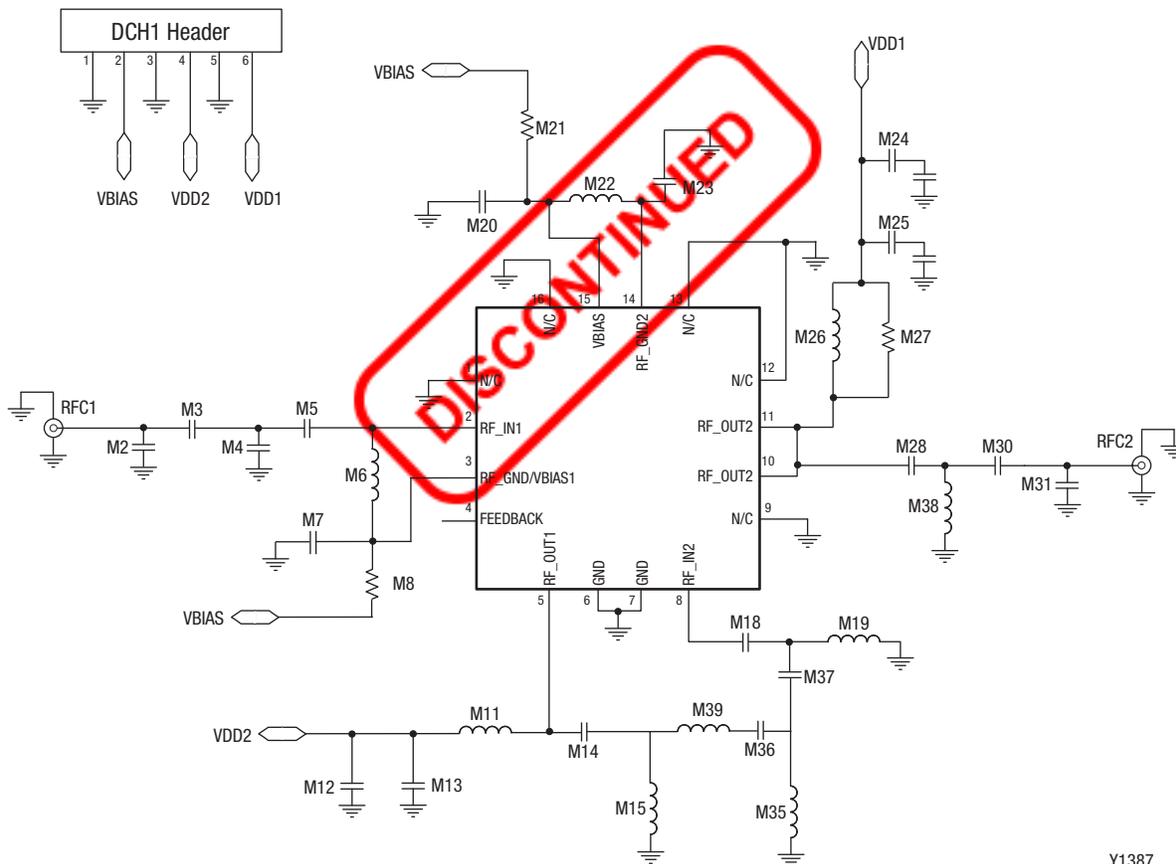
Figure 13. Stability Factor (μ_2) vs Frequency Over Temperature

Evaluation Board Description

The SKY67175-306LF Evaluation Board is used to test the performance of the SKY67175-306LF two-stage LNA.

An Evaluation Board schematic diagram is provided in Figure 14 and Table 5 provides the Evaluation Board Bill of Materials.

The Evaluation Board assembly drawing is shown in Figure 15.



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Figure 14. SKY67175-306LF Evaluation Board Schematic

Table 5. SKY67175-306LF Evaluation Board Bill of Materials (Complete Reference Design)

Component	Type	Value	Size	Manufacturer	Manufacturer Part Number
M2	Capacitor	DNP			
M3	Capacitor	8.2 pF	0402	Murata GJM	GJM1555C1H8R2DB01D
M4	Capacitor	1.0 pF	0402	Murata GJM	GJM1555C1H1R0CB01D
M5	Inductor	8.2 pF	0402	Murata GJM	GJM1555C1H8R2DB01D
M6	Inductor	18 nH	0402	Coilcraft HP	0402HP-18NX_LU
M7		DNP			
M8	Resistor	18 k Ω	0402	Panasonic	ERJ-2RKF1802X
M11	Inductor	3.3 nH	0402	Murata LQG	LQG15HN3N3S02D
M12	Capacitor	1000 pF	0402	Murata GRM	GRM155R71H102KA01
M13	Capacitor	10000 pF	0402	Murata GRM	GRM155R71H103KA88
M14	Capacitor	100 pF	0402	Murata GRM	GRM1555C1H101JA01D
M15	Inductor	1 nH	0402	Murata LQG	LQG15HN1N0S02D
M18	Capacitor	1.0 pF	0402	Murata GRM	GRM1555C1H1R0BA01D
M19	Inductor	5.1 nH	0402	Murata LQG	LQG15HN5N1S02D
M20	Capacitor	5.6 pF	0402	Murata GRM	GRM1555C1H5R6DZ01
M21	Resistor	7.5 k Ω	0402	Panasonic	ERJ-2RKF7501X
M22	Inductor	15 nH	0402	Coilcraft HP	0402HP-15NX_L
M23	Capacitor	1000 pF	0402	Murata GRM	GRM155R71H102KA01
M24	Capacitor	1 μ F	0402	Murata GRM	GRM155R61A105KE15
M25	Capacitor	10 pF	0402	Murata GRM	GRM1555C1H100JZ01
M26	Inductor	9.1 nH	0402	Murata LQG	LQG15HN9N1J02D
M27		DNP			
M28	Capacitor	2.2 pF	0402	Murata GJM	GJM1555C1H2R2CB01D
M30	Capacitor	5.6 pF	0402	Murata GJM	GJM1555C1H5R6DB01D
M31		DNP			
M35		DNP			
M36	Resistor	0 Ω	0402	Panasonic	ERJ-2GE0R00X
M37	Resistor	0 Ω	0402	Panasonic	ERJ-2GE0R00X
M38	Inductor	1.5 nH	0402	Murata LQW	LQW15AN1N5B00D
M39	Capacitor	1.3 pF	0402	Murata GJM	GJM1555C1H1R3CB01D

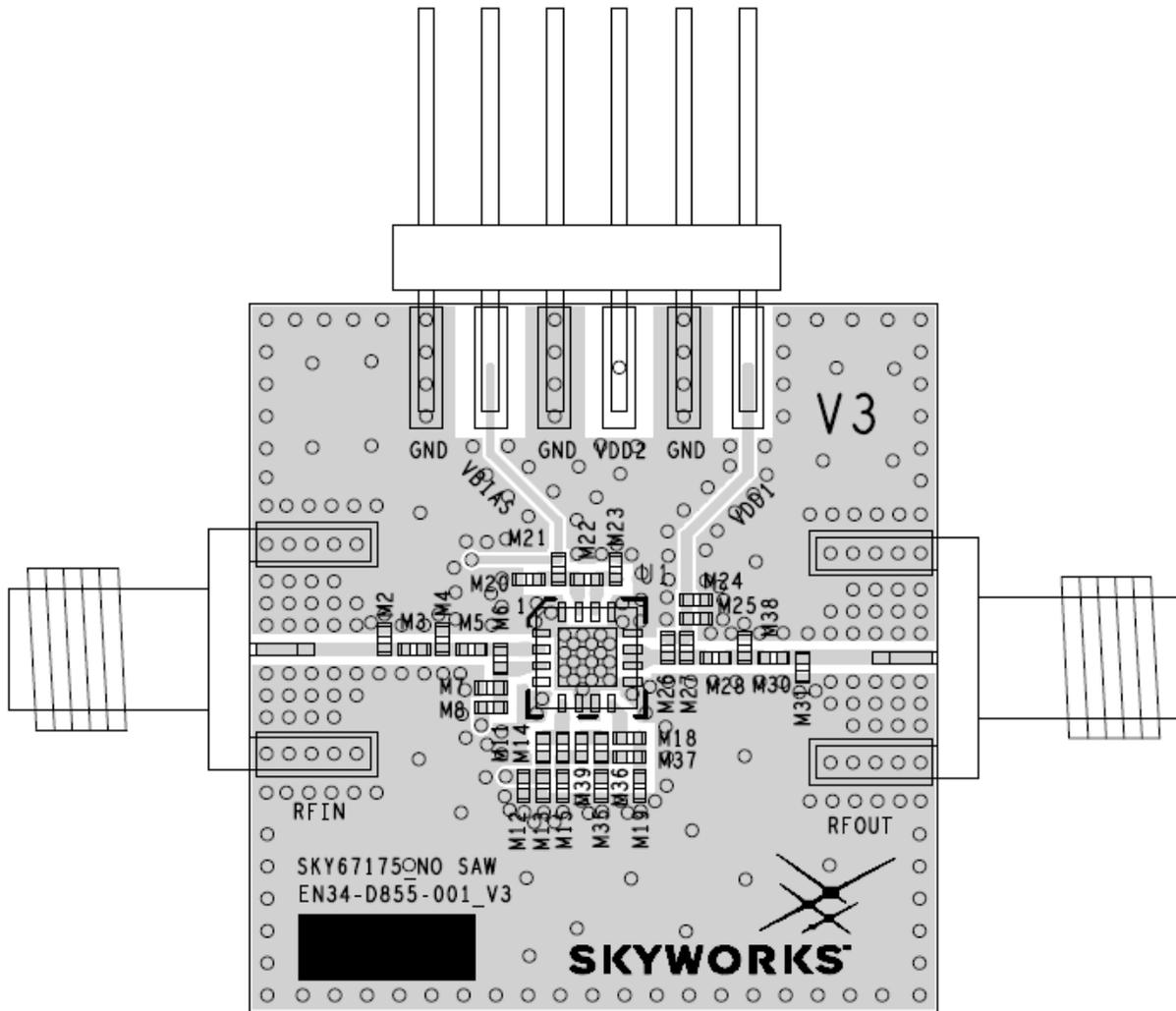


Figure 15. SKY67175-306LF Evaluation Board Assembly Diagram

Package Dimensions

The PCB layout footprint for the SKY67175-306LF is shown in Figure 16. Typical part markings are noted in Figure 17. Package dimensions are shown in Figure 18, and tape and reel dimensions are provided in Figure 19.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY67175-306LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

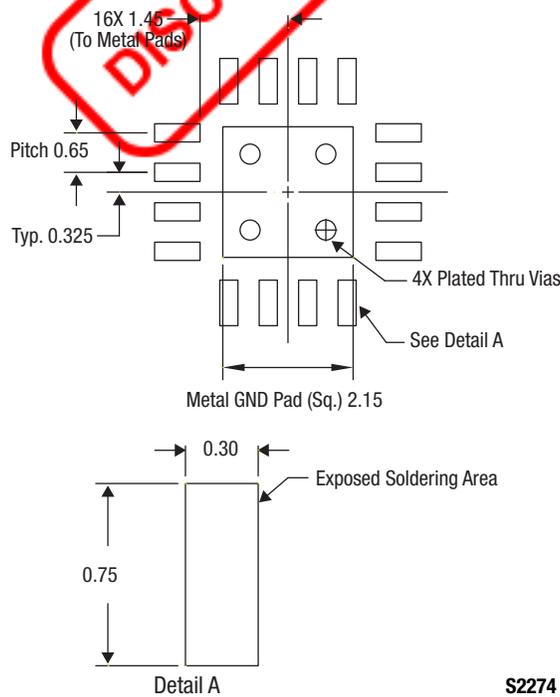


Figure 16. SKY67175-306LF PCB Layout Footprint

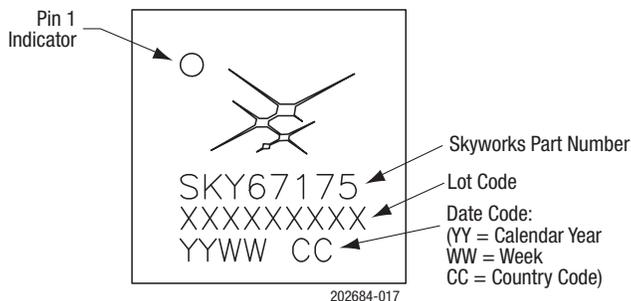
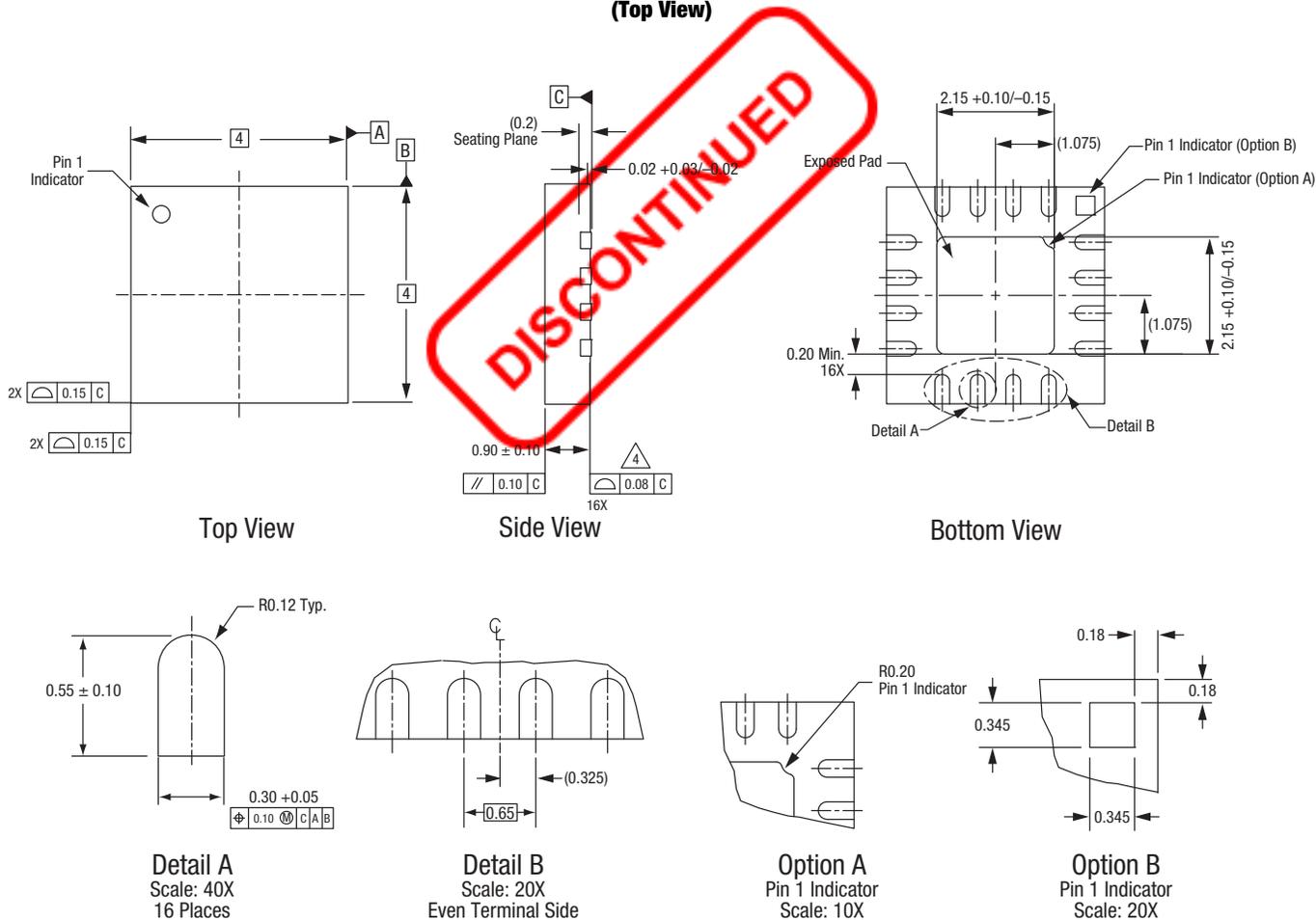


Figure 17. Typical Part Markings (Top View)



Notes:

1. All measurements are in millimeters.
2. Dimensioning and tolerancing according to ASME Y14.5M-1994.
3. Coplanarity applies to the exposed heat sink slug as well as the terminals.
4. Package may have option A or option B pin 1 indicator.

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Figure 18. SKY67175-306LF Package Dimensions

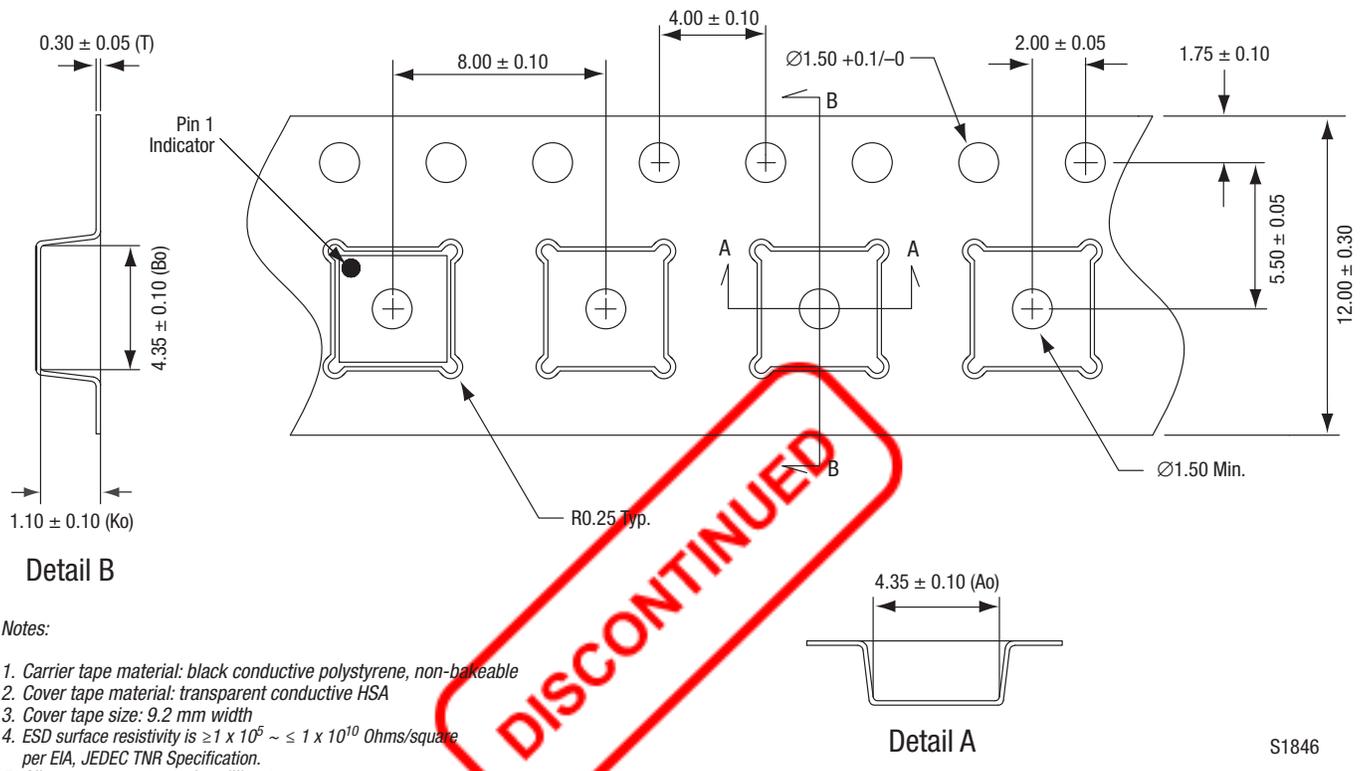


Figure 19. SKY67175-306LF Tape and Reel Dimensions

Ordering Information

Product Description	Product Part Number	Evaluation Board Part Number
SKY67175-306LF: Two-Stage, High-Gain LNA	SKY67175-306LF	SKY67175-306LF-EVB



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