DATA SHEET

SKY77764 Power Amplifier Module for CDMA/ WCDMA/ HSDPA/ HSUPA/ HSPA+/ LTE – Bands III, IV, IX (1710 MHz–1785 MHz)

Applications

- WCDMA handsets
- HSDPA
- HSUPA
- HSPA+
- LTE
- CDMA2000
- EVDO

Features

- Low voltage positive bias supply 3.0 V to 4.5 V
- Good linearity
- High efficiency
  - 46% at 28.6 dBm
- Large dynamic range
- Small, low profile package
  - 3 mm x 3 mm x 0.9 mm
  - 10-pad configuration
- Power down control
- InGaP
- Supports low collector voltage operation
- Digital Enable
- No V_{REF} required
- CMOS compatible control signals
- Integrated Directional Coupler

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to Skyworks *Definition of Green*™, document number SQ04-0074.

Description

The SKY77764 Power Amplifier Module (PAM) is a fully matched 10-pad surface mount module developed for Wideband Code Division Multiple Access (WCDMA) applications. This small and efficient module packs full 1710-1785 MHz bandwidth coverage into a single compact package. Because of high efficiencies attained throughout the entire power range, the SKY77764 delivers unsurpassed talk-time advantages. The SKY77764 meets the stringent spectral linearity requirements of High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), and Long Term Evolution (LTE) data transmission with high power added efficiency. An integrated directional coupler eliminates the need for any external coupler.

The Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all amplifier active circuitry, including input and interstage matching circuits. The silicon CMOS support die, providing precision biasing for the MMIC affords a true CMOS-compatible control interface. Output match into a 50-ohm load, realized off-chip within the module package, optimizes efficiency and power performance.

The SKY77764 is manufactured with Skyworks' InGaP GaAs Heterojunction Bipolar Transistor (HBT) process which provides for all positive voltage DC supply operation and maintains high efficiency and good linearity. While primary bias to the SKY77764 can be supplied directly from any suitable battery with an output of 3.2 V to 4.2 V, optimal performance is obtained with VCC2 sourced from a DC-DC power supply adjusted within 0.5 V to 3.6 V based on target output power levels. Power down executes by setting VENABLE to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

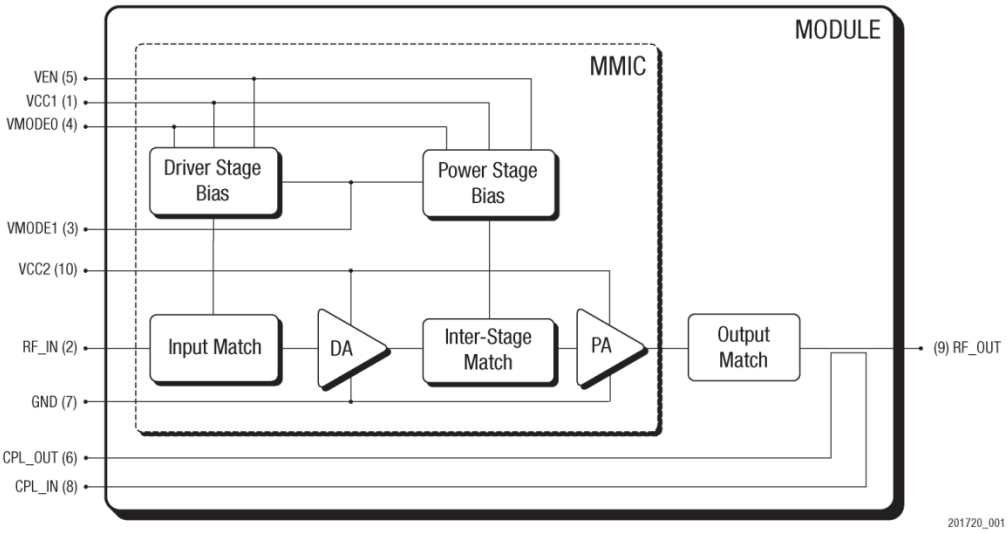


Figure 1. SKY77764 Functional Block Diagram

Electrical Specifications

The following tables list the electrical characteristics of the SKY77764 Power Amplifier. Table 1 lists the absolute maximum ratings and Table 2 shows the recommended operating conditions. Electrical specifications for nominal operating conditions are listed in Table 4. Table 3 presents a truth table for the power settings. Tables 5 through 8 provide the standard test configurations for WCDMA (STC1), HSDPA (STC2), and HSUPA (STC3, STC4) respectively.

Table 1. Absolute Maximum Operating Conditions

No damage assuming only one parameter is set at limit at a time with all other parameters set at nominal value.

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power		P_{IN}	—	0	10	dBm
Supply Voltage	No RF	V_{CC1} V_{CC2}	—	3.4	6.0	Volts
	With RF		—	—	4.6	
Enable Control Voltage		V_{EN}	—	1.8	4.2	Volts
Mode Control Voltage		V_{MODE0}	—	1.8	4.2	Volts
		V_{MODE1}	—	1.8	4.2	
Case Temperature[1]	Operating	T_{CASE}	–30	25	+110	°C
	Storage	T_{STG}	–40	—	+150	

1 Case Operating Temperature (T_{CASE}) refers to the temperature of the GROUND PAD at the underside of the package.

Table 2. Recommended Operating Conditions

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
RF Output Power[1]	WCDMA	P_{OUT_MAX}	28.6	—	—	dBm
	HSDPA		27.6	—	—	
	HSUPA		25.0	—	—	
	LTE		27.6	—	—	
	CDMA2000		28.0	—	—	
Operating Frequency		f_0	1710.0	1747.5	1785.0	MHz
Supply Voltage[2]		V_{CC1}	3.0	3.4	4.5	Volts
		V_{CC2}	0.5	—	3.6	
Enable Control Voltage	Low	V_{EN_L}	0.0	0.0	0.5	Volts
	High	V_{EN_H}	1.35	1.8	3.1	
Mode Control Voltage	Low	V_{MODE0}	0.0	0.0	0.5	Volts
		V_{MODE1}	0.0	0.0	0.5	
	High	V_{MODE0}	1.35	1.8	3.1	
		V_{MODE1}	1.35	1.8	3.1	
Case Operating Temperature		T_{CASE}	–20	+25	+85	°C

1 For V_{CC} < 3.4 V, output power back-off = 0.5 dB.

2 Specifications in Table 4 are specified at VCC1 = 3.2 V–4.2 V.

Table 3. Modes of Operation

Power Setting	ENABLE	VMODE0	VMODE1	VCC
Power Down Mode	Low	Low	Low	On
Standby Mode	Low	—	—	On
High Power Mode (17.0 dBm ≤ P_{OUT} ≤ 28.6 dBm)	High	Low	—	On
Medium Power Mode (7.0 dBm ≤ P_{OUT} ≤ 17.0 dBm)	High	High	Low	On
Low Power Mode (P_{OUT} ≤ 7.0 dBm)	High	High	High	On

Table 4. Electrical Specifications for Nominal Operating Conditions

Per Table 2 over dynamic range up to 28.6 dBm output power for STC1 modulation, unless otherwise specified.

Characteristics		Symbol	Condition	Minimum	Typical	Maximum	Unit
Gain[1]		G_{LOW}	P_{OUT} = 7.0 dBm V_{CC2} = 0.8 V	12.0	16.0	19.0	dB
		G_{MED}	P_{OUT} = 17.0 dBm V_{CC2} = 1.5 V	20.0	24.0	28.0	
		G_{HIGH}	P_{OUT} = 28.6 dBm	25.0	28.0	31.0	
Rx Band Gain	Band III	RxG	P_{OUT} = 28.6 dBm	—	—	–1	dB
	Band IV			—	—	–6	
	Band IX			—	—	–1	
		$RxG_{\_GPS}$		—	—	–1	
		$RxG_{\_ISM}$		—	—	–10	
Power Added Efficiency		PAE_{LOW}	P_{OUT} = 7.0 dBm, V_{CC2} = 0.8 V	10.5	12.5	—	%
		PAE_{MED}	P_{OUT} = 17.0 dBm, V_{CC2} = 1.5 V	22.0	26.0	—	
		PAE_{HIGH}	P_{OUT} = 28.6 dBm	43.0	46.0	—	
Total Supply Current		I_{CC_LOW}	P_{OUT} = 7.0 dBm, V_{CC2} = 0.8 V	—	45	55	mA
		I_{CC_MED}	P_{OUT} = 17.0 dBm, V_{CC2} = 1.5 V	—	125	150	
		I_{CC_HIGH}	P_{OUT} = 28.6 dBm	—	460	500	
Quiescent Current		I_{Q_LOW}	Low Power Mode	—	23	27	mA
		I_{Q_MED}	Medium Power Mode	—	33	42	
Enable Control Current		I_{EN}	—	—	20	40	µA
Mode Control Current		I_{MODE0}	—	—	20	40	µA
		I_{MODE1}	—	—	20	40	
Total Supply Current in Power Down Mode		I_{PD}	V_{CC} = 4.5 V V_{EN} = Low V_{MODE0} = Low V_{MODE1} = Low	—	1	10	µA
ICC1 Current		I_{CC1_HIGH}	—	—	—	10	mA
Adjacent Channel Leakage power Ratio[2]	5 MHz offset	ACLR5	P_{OUT} = 7.0 dBm	—	–43.0	–38.5	dBc
			P_{OUT} = 17.0 dBm	—	–47.0	–39.0	
			P_{OUT} = 28.6 dBm	—	–42.0	–39.0	
	10 MHz offset	ACLR10	P_{OUT} = 7.0 dBm	—	–67.0	–52.0	
			P_{OUT} = 17.0 dBm	—	–65.0	–52.0	
			P_{OUT} = 28.6 dBm	—	–55.0	–52.0	

Table. 4 [continued] **Electrical Specifications for Nominal Operating Conditions**

Per Table 2 over dynamic range up to 28.6 dBm output power for STC1 modulation, unless otherwise specified.

Characteristics			Symbol	Condition	Minimum	Typical	Maximum	Unit
Adjacent Channel Leakage power Ratio[3]		EUTRA offset	$ACLR_{EUTRA}$	$P_{OUT} \leq (P_{OUT\_MAX} - MPR^4)$	—	–40	—	dBc
		UTRA offset	$ACLR1_{UTRA}$		—	–42	—	
			$ACLR2_{UTRA}$		—	—	—	
Adjacent Channel Power Ratio[5,6]	1.25 MHz offset		ACPR1	P_{OUT} = 28.25 dBm	—	–49	—	dBc
	1.98 MHz offset		ACPR2		—	–57	—	
Harmonic Suppression		Second	$f_0 2$	$P_{OUT} \leq$ 28.6 dBm	—	–45	–35	dBc
		Third	$f_0 3$		—	–50	–45	
Tx Noise in Rx Bands[1]		Rx Band III		1805 MHz–1880 MHz	—	—	–137	dBm/Hz
		Rx Band IV		2110 MHz–2170 MHz	—	—	–140	
		Rx Band IX		1840 MHz–1879.9 MHz	—	—	–136	
		GPS Rx		1574 MHz–1577 MHz	—	—	–134	
		ISM Rx		2400 MHz–2483.5 MHz	—	—	–143	
Error Vector Magnitude			EVM1	$P_{OUT} = P_{OUT\_MAX}$	—	—	3.35	%
			EVM2	$P_{OUT} = P_{OUT\_MAX} - 3$	—	—	2.50	
Rise / Fall Time		DC	TON_{DC}	—	—	—	20	µs
			$TOFF_{DC}$	—	—	—	20	
		RF	TON_{RF}	—	—	—	6	
			$TOFF_{RF}$	—	—	—	6	
Coupling Factor			CPL	$P_{OUT} = P_{OUT\_MAX}$	–22	–20	–18	dB
CPL_{OUT} / P_{OUT} Power Ratio Variation Over Output VSWR				2.5:1 VSWR at P_{OUT} all VSWR phases CPL_{IN} 50 Ω terminated	—	±0.32	—	dB
Daisy-chain	VSWR			CPL_{IN} and CPL_{OUT} ports 698 MHz to 2620 MHz V_{EN} = Low	—	—	1.6:1	dB
	Insertion Loss			CPL_{IN} to CPL_{OUT} ports 698 MHz to 2620 MHz V_{EN} = Low	—	—	0.25	
Input Voltage Standing Wave Ratio			VSWR	—	—	1.7:1	1.95:1	—
Stability (Spurious output)[1]			S	6:1 VSWR All phases	—	—	–70	dBc
Ruggedness – no damage[1,7]			Ru	$P_{OUT} \leq$ 28.6 dBm	10:1	—	—	VSWR

1 Over conditions

2 ACLR is expressed as a ratio of total adjacent power to WCDMA modulated in-band, both measured in 3.84 MHz bandwidth at specified offsets.

3 LTE: EVM and ACLR are measured with QPSK modulation with 20 MHz bandwidth and 18 resource blocks. (Maximum Power Reduction = 0 dBm per 3GPP TS36.101.

4 MPR is the maximum power reduction as defined in 3GPP TS36.101

5 ACPR is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

6 For CDMA2000 test configured as [PCD at –7.40 dB, DCCH–9600 bps at –15.35 dB; SCHO–9600 bps at –15.63 dB] and other test configurations that yield a peak-to-average up to 4.02 dB for CCDF = 1%, up to 1 dB power back off from the maximum listed for IS95 may be required to meet specified maximum ACP performance under worst-case conditions.

7 All phases, time = 10 seconds.

Table 5. Standard Test Configuration – STC1 WCDMA Mode

Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βec	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	8/15	—	—	—	—	–6.547
DPDCH	60 kbps	16	64	I	—	15/15	—	—	—	–1.087

Table 6. Standard Test Configuration – STC2 HSDPA Mode

Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βec	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	12/15	—	—	—	—	–7.095
DPDCH	60 kbps	16	64	I	—	15/15	—	—	—	–5.157
HS-DPCCH	15 kbps	64	256	Q	—	—	24/15	—	—	–3.012

Table 7. Standard Test Configuration – STC3 HSUPA Mode

Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βec	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	8/15	—	—	—	—	–19.391
DPDCH	960 kbps	1	4	I	—	15/15	—	—	—	–13.931
HS- DPCCH	15 kbps	64	256	Q	—	—	8/15	—	—	–19.391
E-DPCCH	15 kbps	1	256	I	—	—	—	10/15	—	–17.338
E-DPDCH	960 kbps	2	4	I	—	—	—	—	71.5/15	–0.371

Table 8. Standard Test Configuration – STC4 HSUPA Mode

Parameter	Level	Spread Code	Spread Factor	I/Q	βc	βd	βhs	βec	βed	Relative Power (dB)
DPCCH	15 kbps	0	256	Q	6/15	—	—	—	—	–12.499
DPDCH	960 kbps	1	4	I	—	15/15	—	—	—	–4.540
HS- DPCCH	15 kbps	64	256	Q	—	—	2/15	—	—	–22.041
E-DPCCH	15 kbps	1	256	I	—	—	—	12/15	—	–6.478
E-DPDCH	960 kbps	2	4	I	—	—	—	—	15/15	–4.425

Evaluation Board Description

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the SKY77764, the evaluation board schematic and assembly diagrams are included for analysis and design. Figure 2 shows the basic schematic of the board for the 1710 MHz to 1785 MHz range.

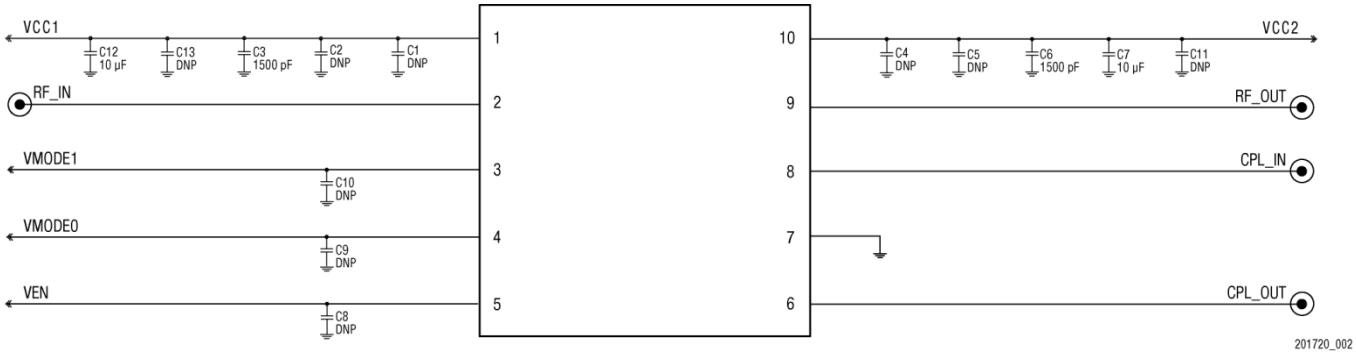
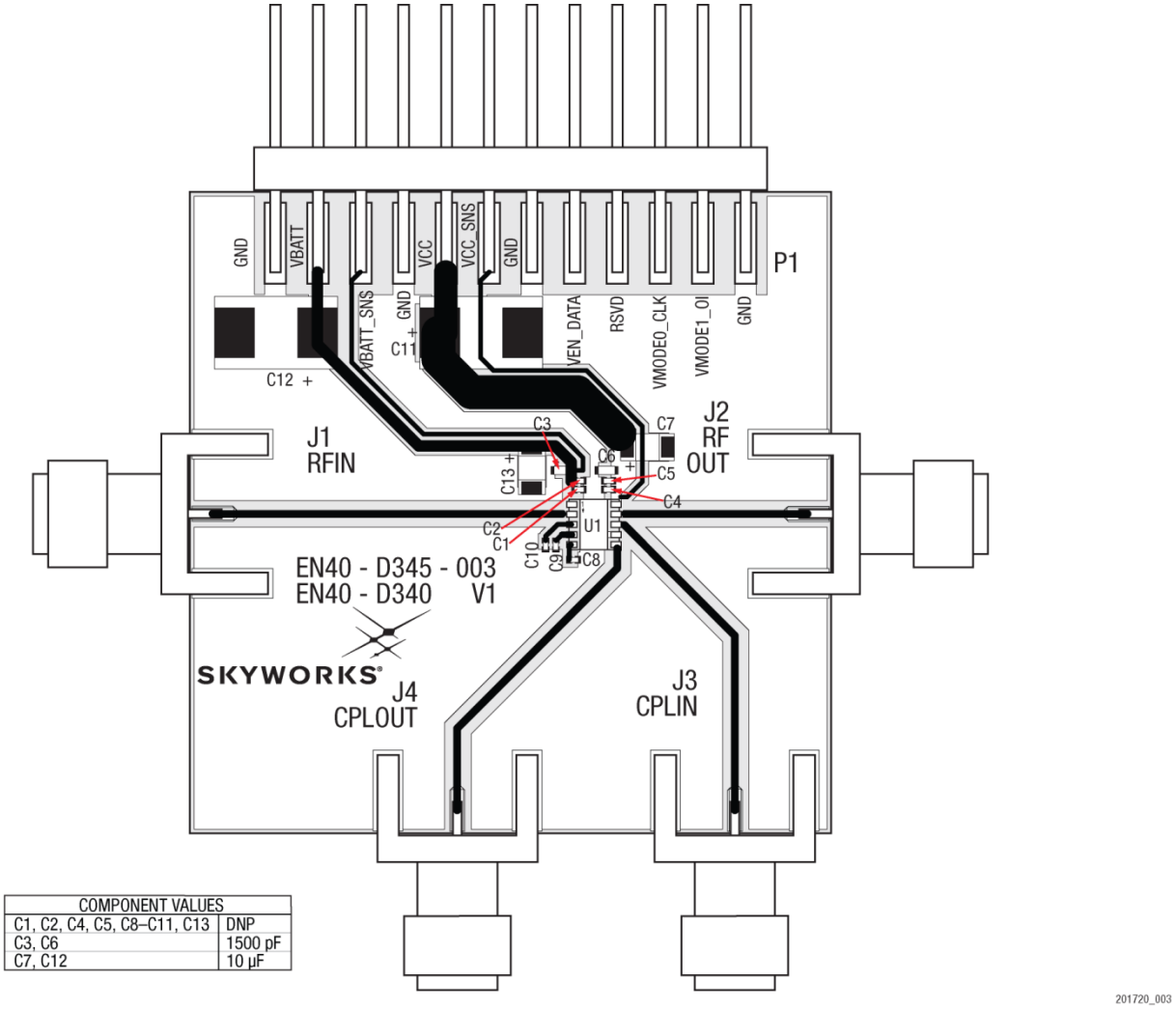


Figure 2. Evaluation Board Schematic

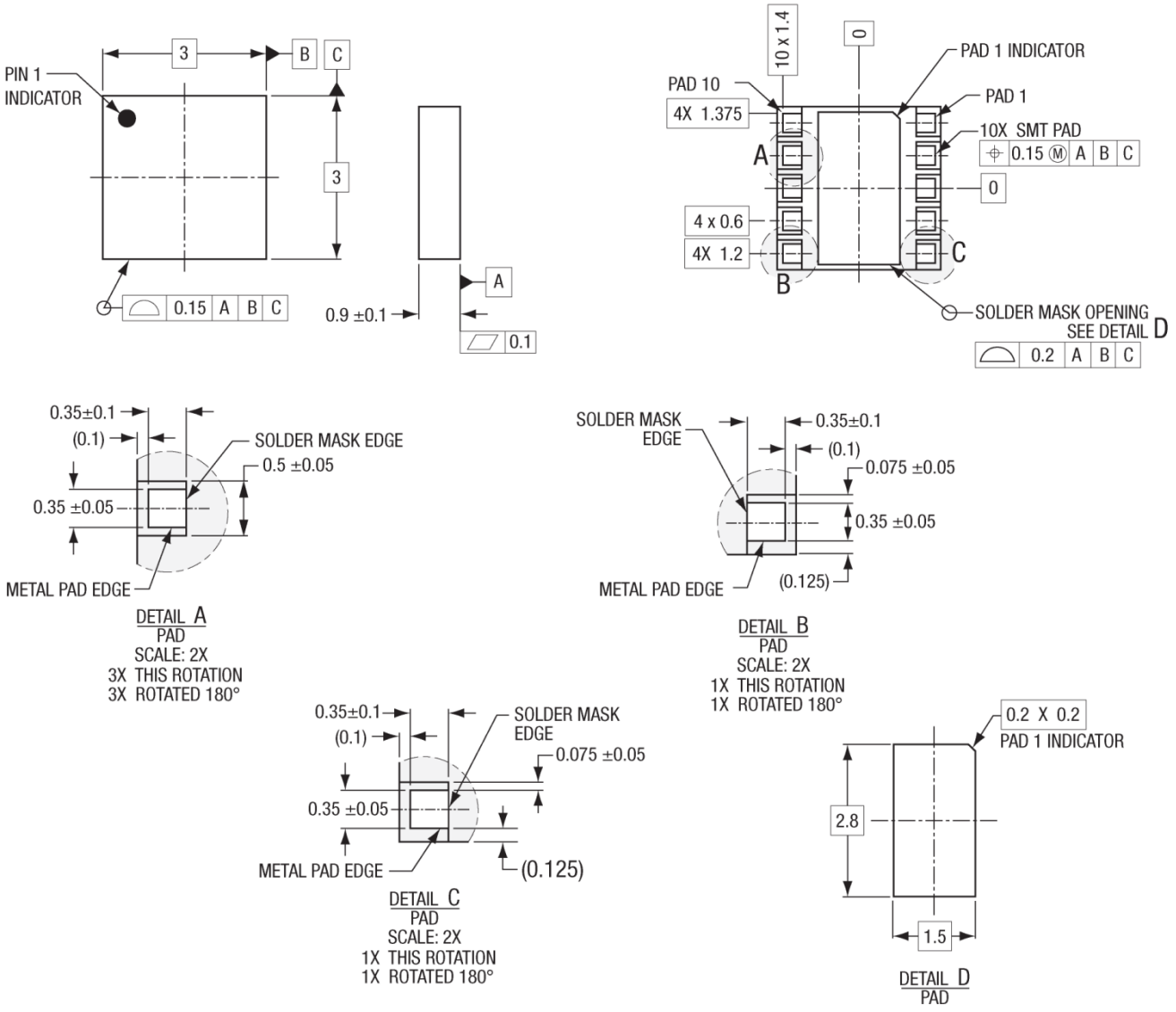


COMPONENT VALUES	
C1, C2, C4, C5, C8–C11, C13	DNP
C3, C6	1500 pF
C7, C12	10 µF

Figure 3. Evaluation Board Assembly Diagram

Package Dimensions

The SKY77764 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 4 is a mechanical drawing of the pad layout for this package. Figure 5 provides a recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals.



NOTES: Unless otherwise specified.
1. Dimensioning and Tolerancing in accordance with ASME Y14.5M–1994
2. All dimensions are in millimeters.

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201720_004

Figure 4. Dimensional Diagram for 3 mm x 3 mm x 0.9 mm Package – SKY77764 Specific

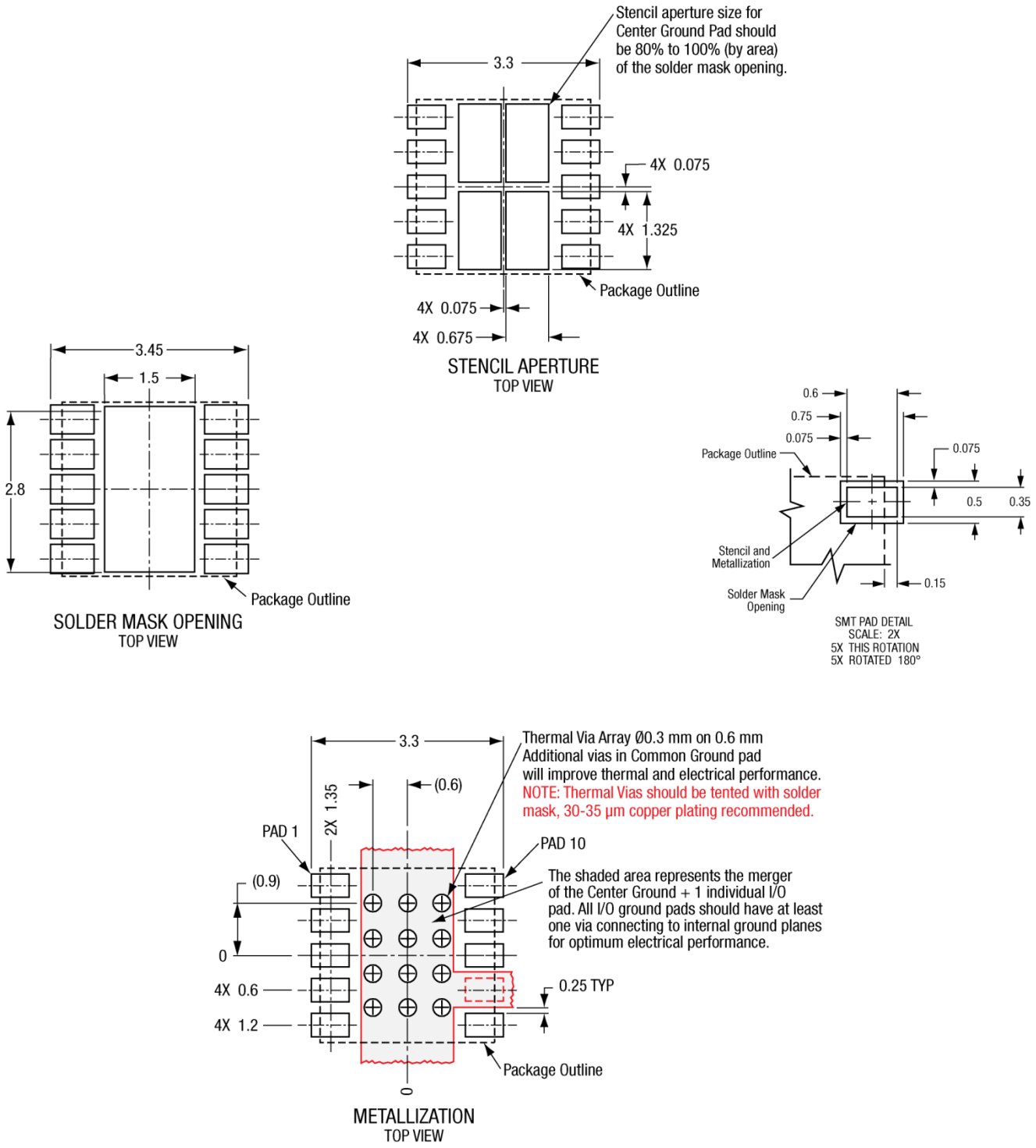
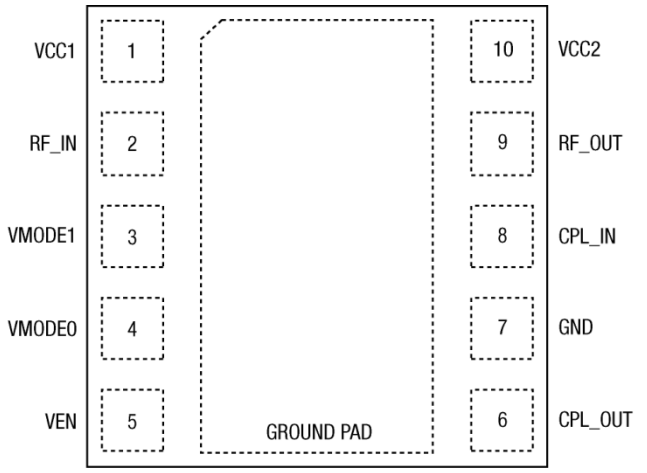


Figure 5. Phone PCB Layout Diagram – 3 mm x 3 mm, 10-Pad Package – SKY77764

Package Description

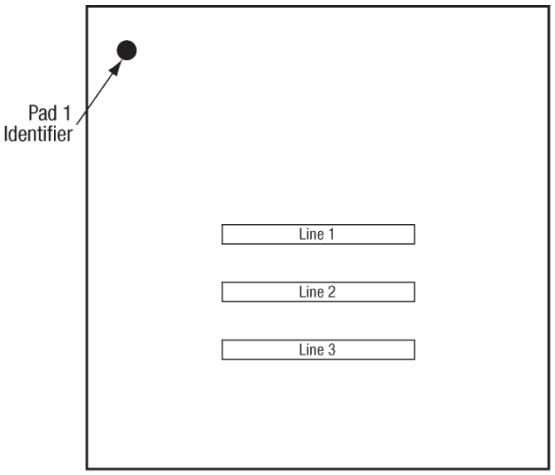
Figure 6 shows the pad functions and the pad numbering convention, which starts with pad 1 in the upper left and increments counter-clockwise around the package. Typical case markings are illustrated in Figure 7.



Pad layout as seen from Top View looking through the package.
GROUND PAD is package underside.

201720_006

Figure 6. SKY77764 Pad Names and Configuration (Top View)



NOTE: Lines 1, 2, 3 have a maximum of 7 characters
Line 1 = Part Number and Version
Line 2 = Lot Number
Line 3 = Year–Week–Country Code (MX)

201075_007

Figure 7. Typical Case Markings

Package Handling Information

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY77764 is capable of withstanding an MSL3/260 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 3 °C per second; maximum temperature should not exceed 260 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 260 °C for more than 10 seconds. For details on attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to Skyworks Application Note: *PCB Design and SMT Assembly/Rework*, Document Number 101752. Additional information on standard SMT reflow profiles can also be found in the JEDEC Standard J-STD-020.

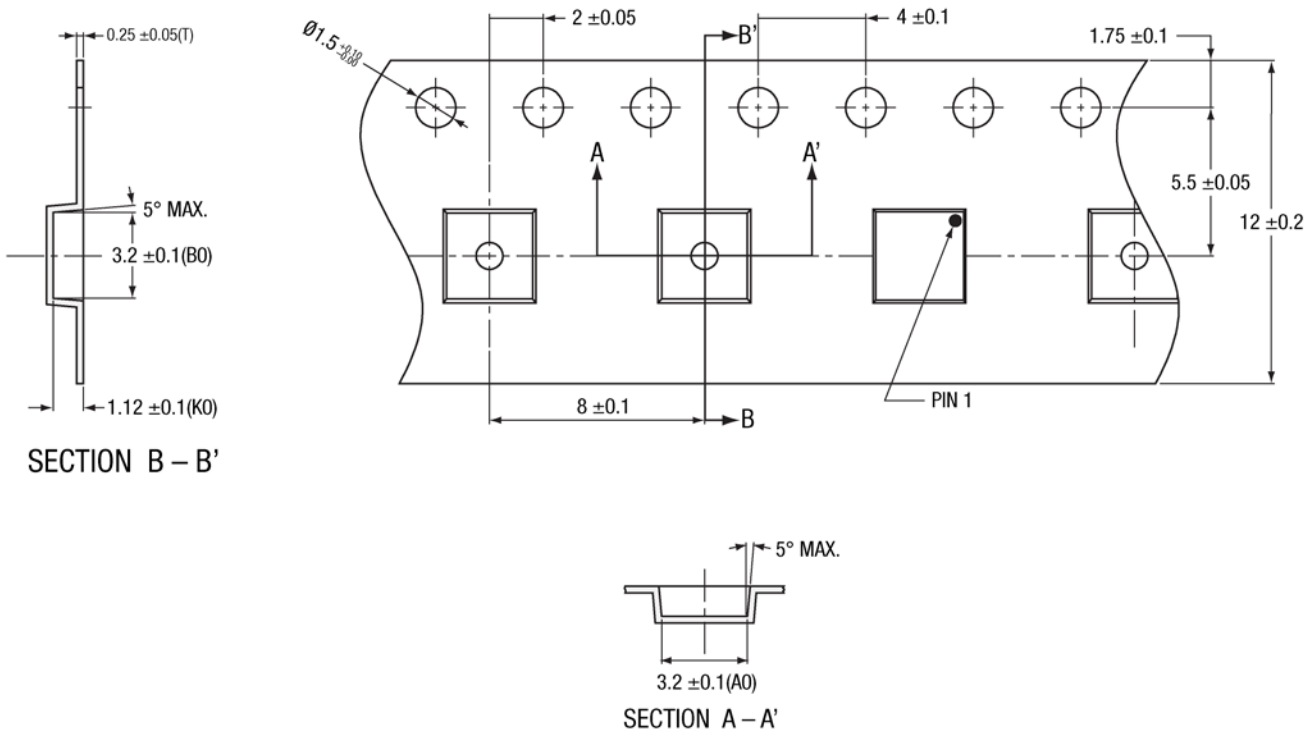
Production quantities of this product are shipped in the standard tape-and-reel format (Figure 8).

Electrostatic Discharge (ESD) Sensitivity

The SKY77764 meets class 1C JESD22-A114 Human Body Model (HBM), class IV JESD22-C101 Charged-Device Model (CDM), and class A JESD22-A115 Machine Model (MM) electrostatic discharge (ESD) sensitivity classification.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the ESD handling precautions listed below.

- Personnel Grounding
  - Wrist Straps
  - Conductive Smocks, Gloves and Finger Cots
  - Antistatic ID Badges
- Protective Workstation
  - Dissipative Table Top
  - Protective Test Equipment (Properly Grounded)
  - Grounded Tip Soldering Irons
  - Solder Conductive Suckers
  - Static Sensors
- Facility
  - Relative Humidity Control and Air Ionizers
  - Dissipative Floors (less than 1,000 MΩ to GND)
- Protective Packaging and Transportation
  - Bags and Pouches (Faraday Shield)
  - Protective Tote Boxes (Conductive Static Shielding)
  - Protective Trays
  - Grounded Carts
  - Protective Work Order Holders



NOTES:

1. CARRIER TAPE IS BLACK CONDUCTIVE POLYCARBONATE OR POLYSTYRENE.
2. COVER TAPE IS TRANSPARENT AND CONDUCTIVE.
3. ESD-SURFACE RESISTIVITY IS ≤ 1 X 10^{10} OHMS/SQUARE PER EIA, JEDEC TNR SPECIFICATION.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE: ±0.2 mm
5. Ao & Bo MEASURED ON PLANE 0.3 mm ABOVE THE BOTTOM OF THE POCKET.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

CARRIER TAPE OVERMOLD MCM / RFLGA 3 x 3 x 0.75 / 0.90 mm BODY SIZE -108A
201075_008

Figure 8. Dimensional Diagram for Carrier Tape Body Size 3 mm x 3 mm x 0.75 / 0.90 mm – MCM

Ordering Information

Product Name	Order Number	Evaluation Board Part Number
SKY77764 Power Amplifier Module	SKY77764-11	EN40-D345-003

Revision History

Revision	Date	Description
A	December 20, 2011	Initial Release – Information
B	March 8, 2012	Revise: Figures 1, 4, 5; Tables 1, 4 Add: Figures 2, 3
C	April 9, 2012	Revise: Change Data Sheet status from to PRELIMINARY; Features list (p1); Description (p1); Tables 2–4
D	August 5, 2012	Revise: Change Data Sheet status from PRELIMINARY to FINAL; Table 4; Ordering Information Table (last page)

References

Skyworks Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752.

Standard SMT Reflow Profiles: JEDEC Standard J–STD–020

Electrostatic Discharge Sensitivity (ESD) Testing: JEDEC Standard, JESD22-A114 Human Body Model (HBM)

Electrostatic Discharge Sensitivity (ESD) Testing: JEDEC Standard, JESD22-A115 Machine Model (MM)

Electrostatic Discharge Sensitivity (ESD) Testing: JEDEC Standard, JESD22-C101 Charged Device Model (CDM).