

The SL2017 is a fully integrated mixer with output AGC, intended primarily for application in satellite tuners, where it downconverts the first high IF from the outdoor unit to the second IF for data demodulation.

The device contains a low noise RF input amplifier and mixer functioning to 2.15GHz, an integrated low phase noise local oscillator buffer and an AGC IF output buffer amplifier. The IF signal is available at one of two outputs selected by the IF-OP-SEL input.

The signal handling of the SL2017 is sufficient to greatly simplify or remove the requirement for input AGC with appropriate image filtering in full band systems, or to remove the requirement for band limit filtering with appropriate AGC in half band systems.

FEATURES

- Single chip full band solution, compatible with digital and analog transmissions
- Low noise RF input
- High input signal handling to eliminate the requirement for front end AGC
- Low phase noise local oscillator buffer optimised for low symbol rate applications
- Low radiation design
- IF AGC amplifier with dual selectable outputs
- ESD protection. (Normal ESD handling procedures should be observed)

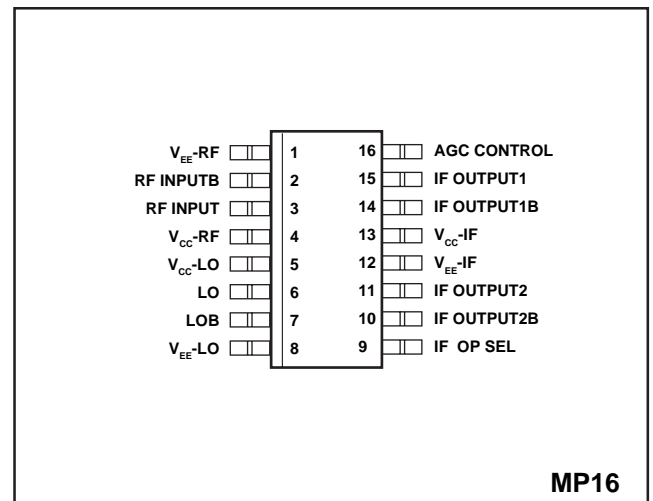


Fig.1 Pin connections - top view

ORDERING INFORMATION

SL2017/KG/MP1S (Tubes)
SL2017/KG/MP1T (Tape and Reel)

APPLICATIONS

- Satellite tuners
- Communications systems

QUICK REFERENCE DATA

Characteristic		Units
RF input noise figure	18	dB
Maximum conversion gain	33	dB
Minimum conversion gain	-5	dB
IF1 and IF2 output gain match	2	dB
IP3 _{2T} input referred at minimum conversion gain	+3	dBm
IP2 _{2T} input referred at minimum conversion gain	+17	dBm

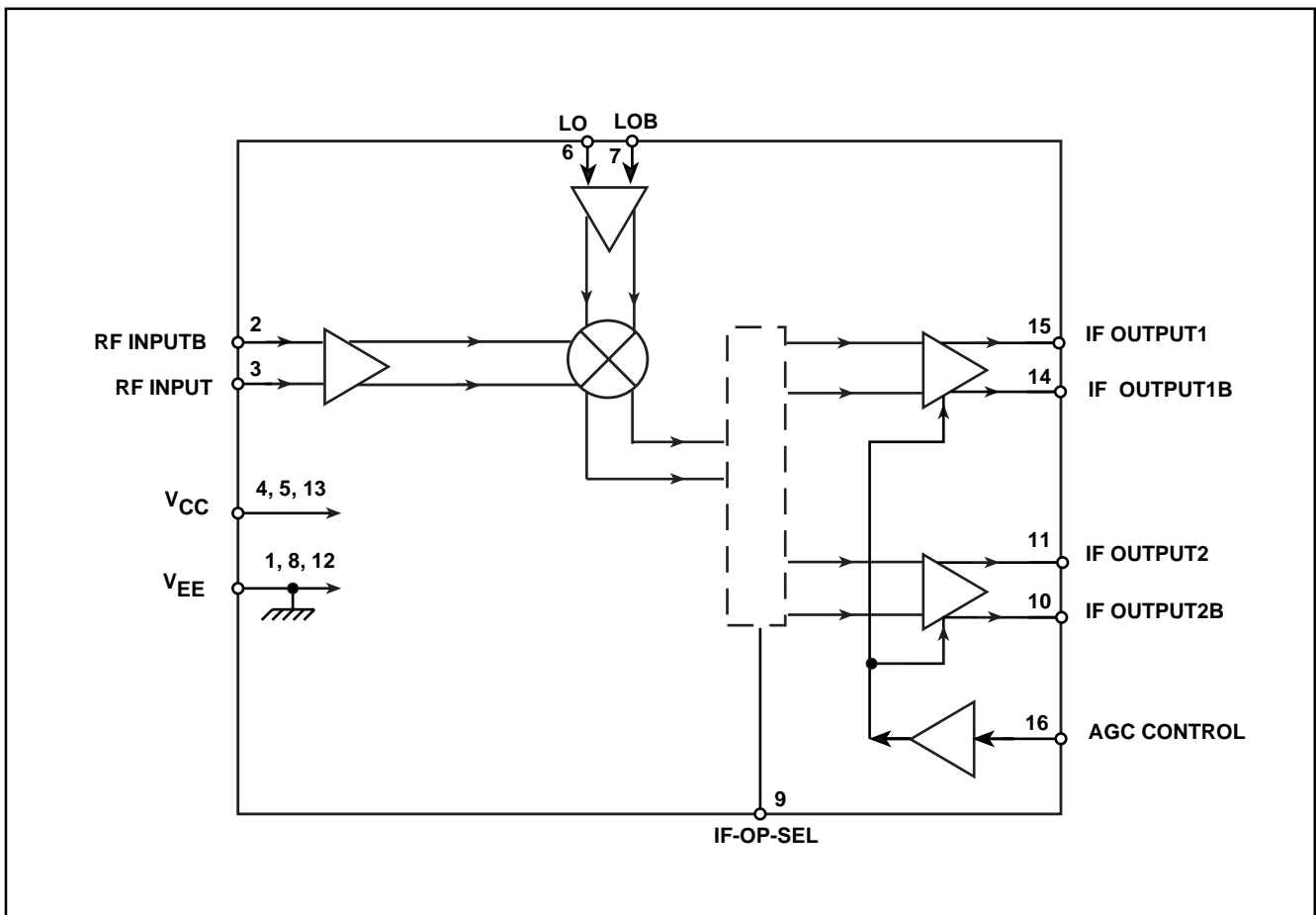


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SL2017 is a downconverter mixer with an output AGC amplifier, which when used with appropriate external varactor tuned oscillator performs the first IF tuning function for a full band satellite receiver system. A block diagram is contained in Fig. 2.

In application the RF input of the device is interfaced through appropriate impedance matching to the first IF signal, which is downlinked from the outdoor unit at typically 950-2150MHz. The RF input preamplifier of the device is designed for low noise figure and for low distortion so eliminating the requirement for RF AGC. The preamplifier also provides gain to the mixer section and back isolation from the local oscillator section.

The output of the preamplifier is fed to the mixer section where the RF signal is mixed with the local oscillator frequency, which is generated by an external oscillator.

Signals from the mixer are fed to the AGC IF amplifier, which gives an overall conversion gain programmable from -10 to +30dB. The output of this stage can be switched to one of two outputs to facilitate IF processing.

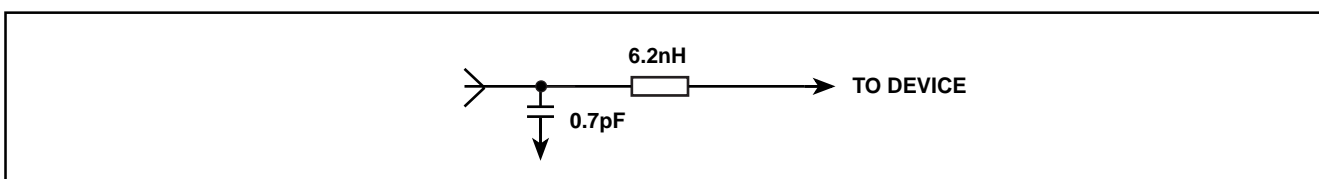


Fig. 3 RF input matching network

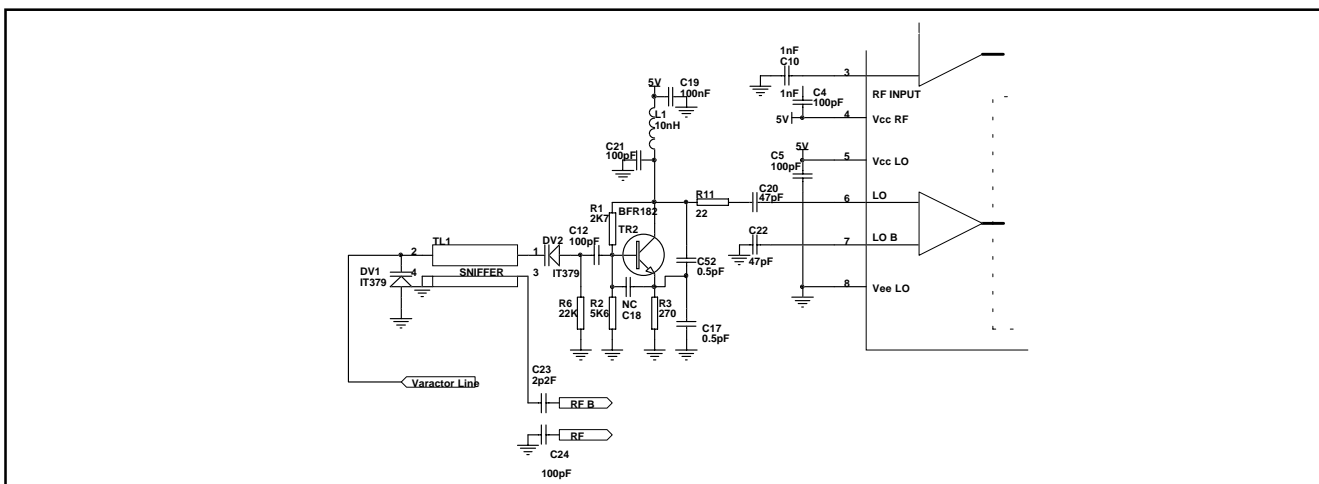


Fig. 4 Typical external VCO application circuit

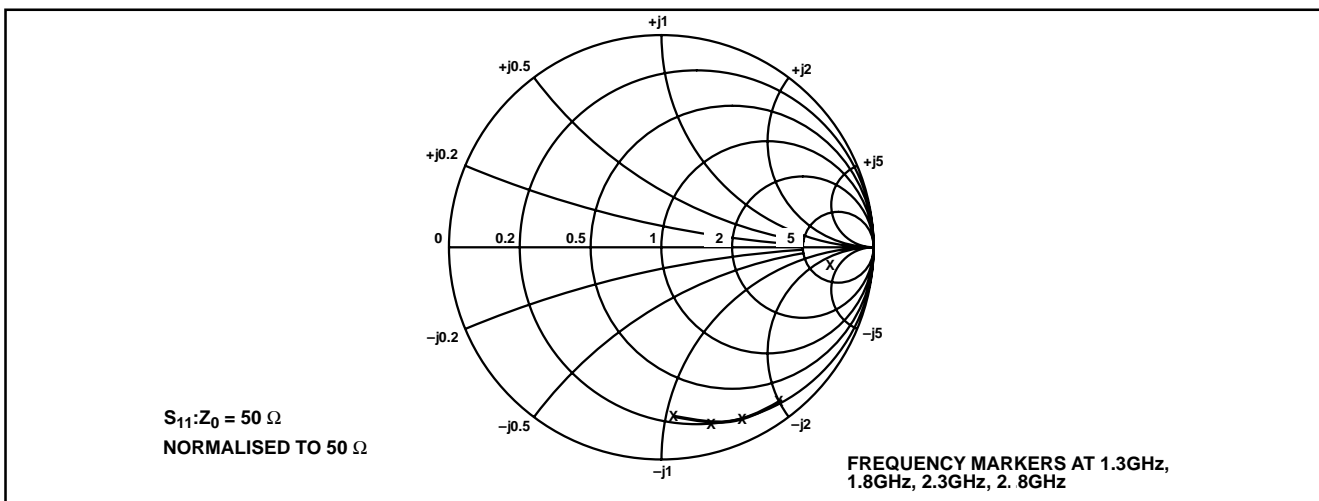


Fig. 5 LO buffer input impedance

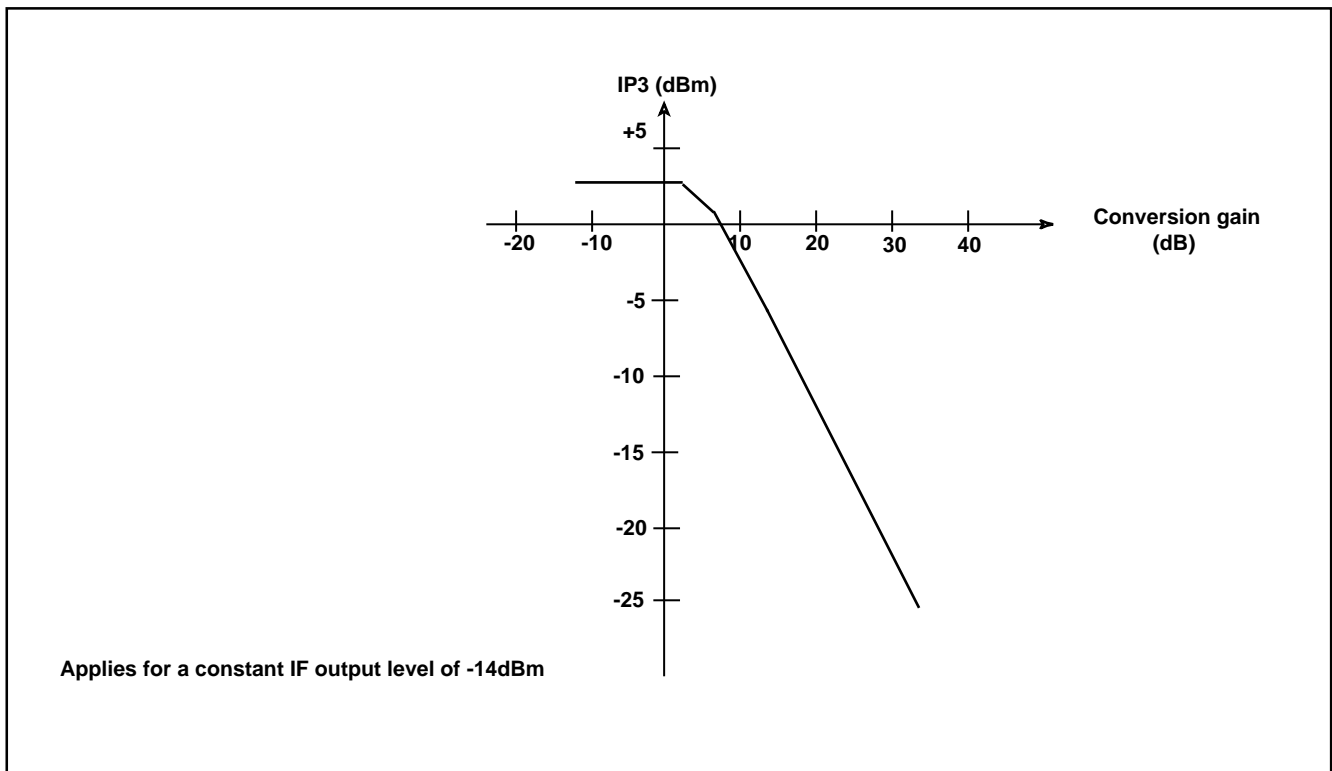


Fig. 6 IP3 variation with gain setting (minimum)

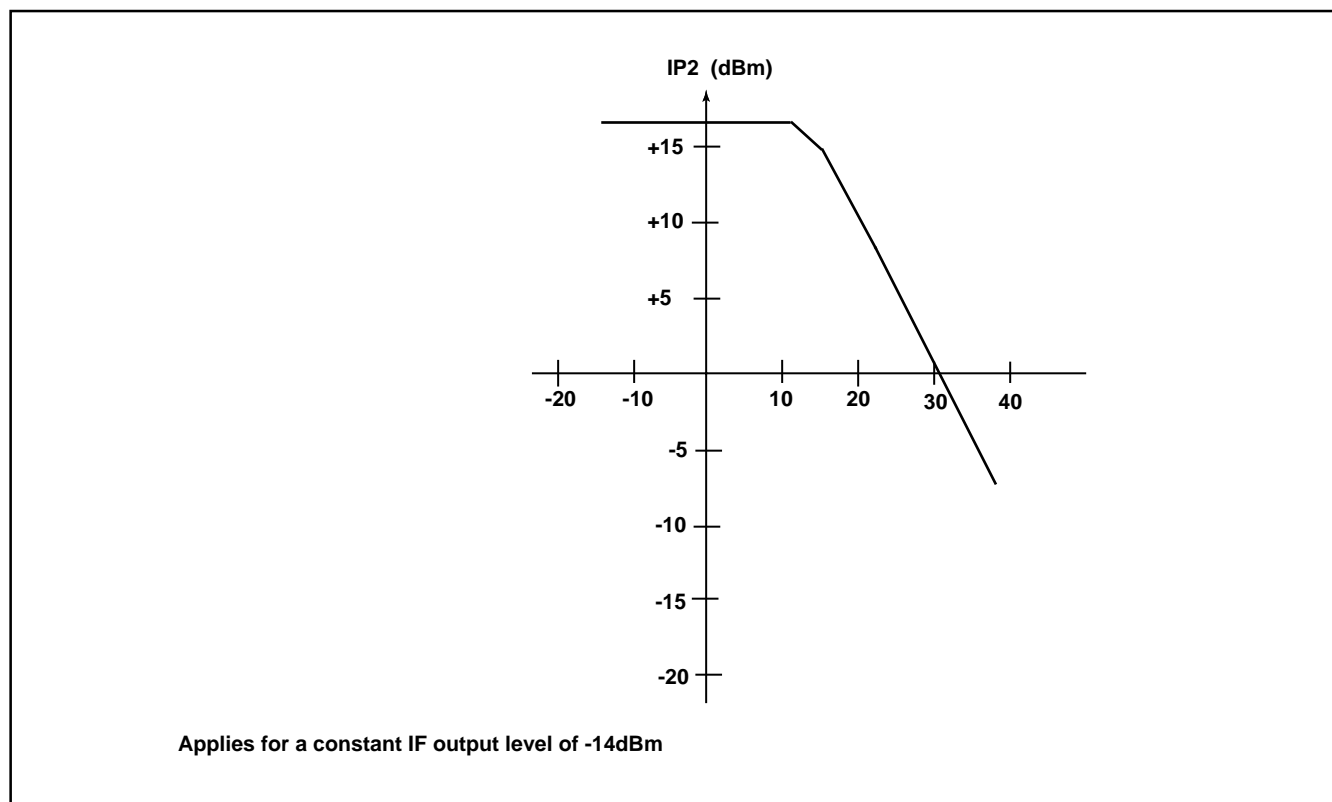


Fig. 7 IP2 variation with gain setting (minimum)

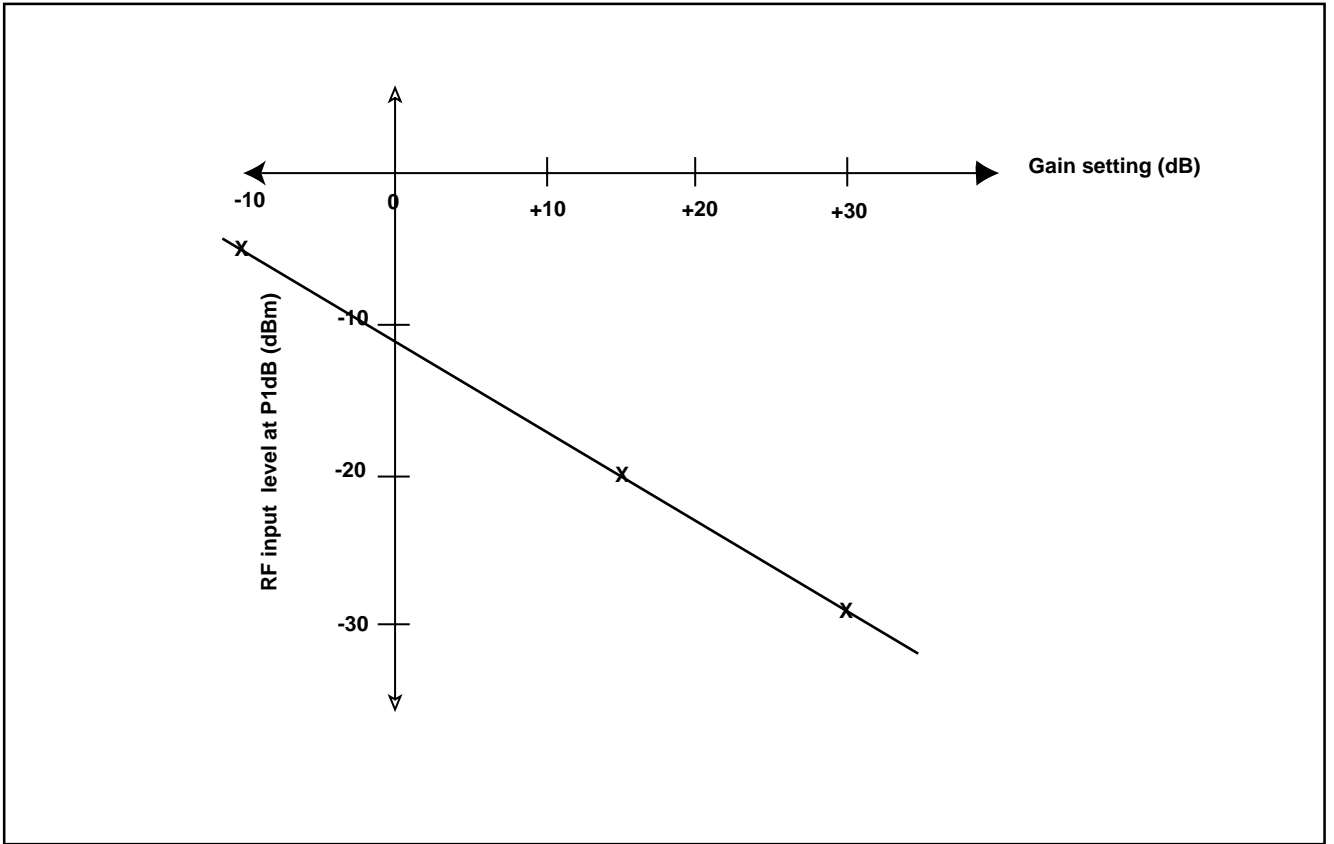


Fig. 8 Variation of 1dB gain compression (P1dB) with gain setting (typical)

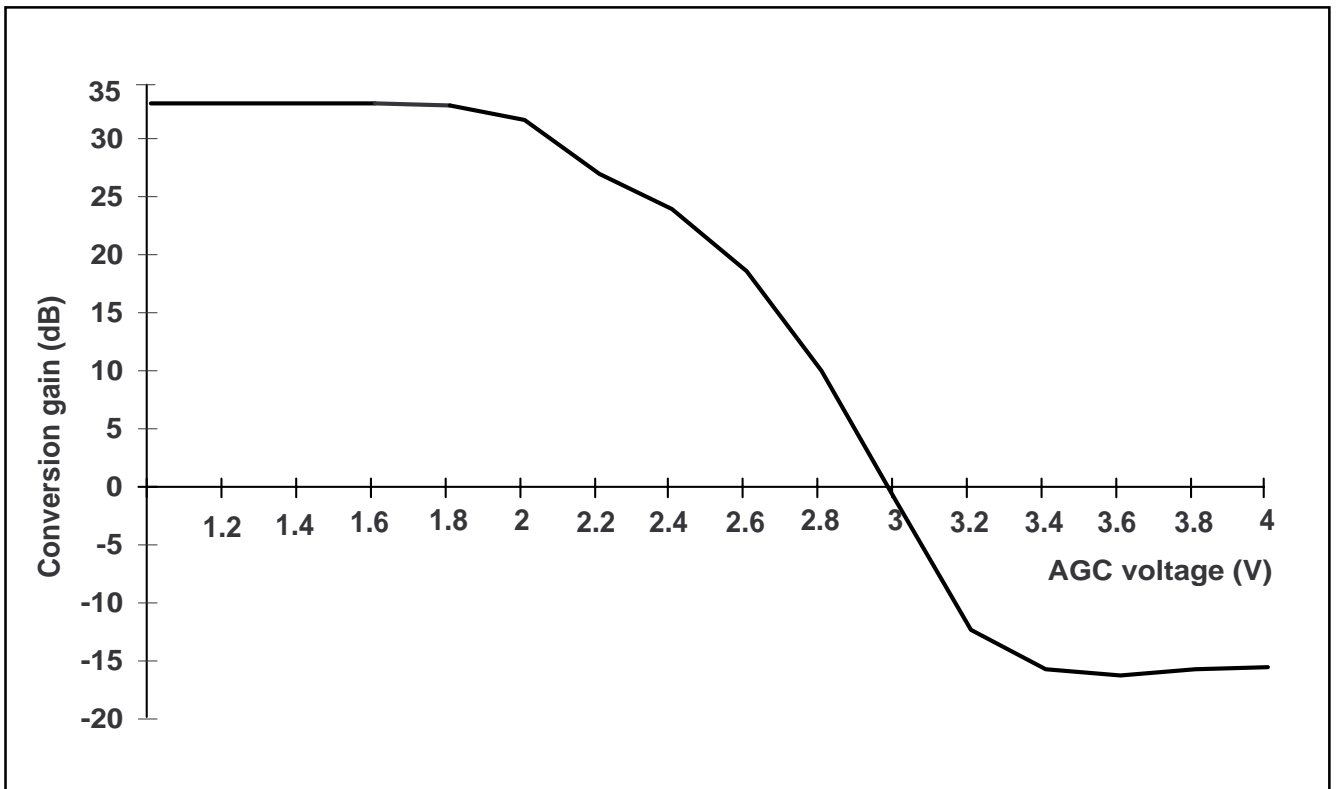


Fig.9 Gain variations with AGC voltage (typical)

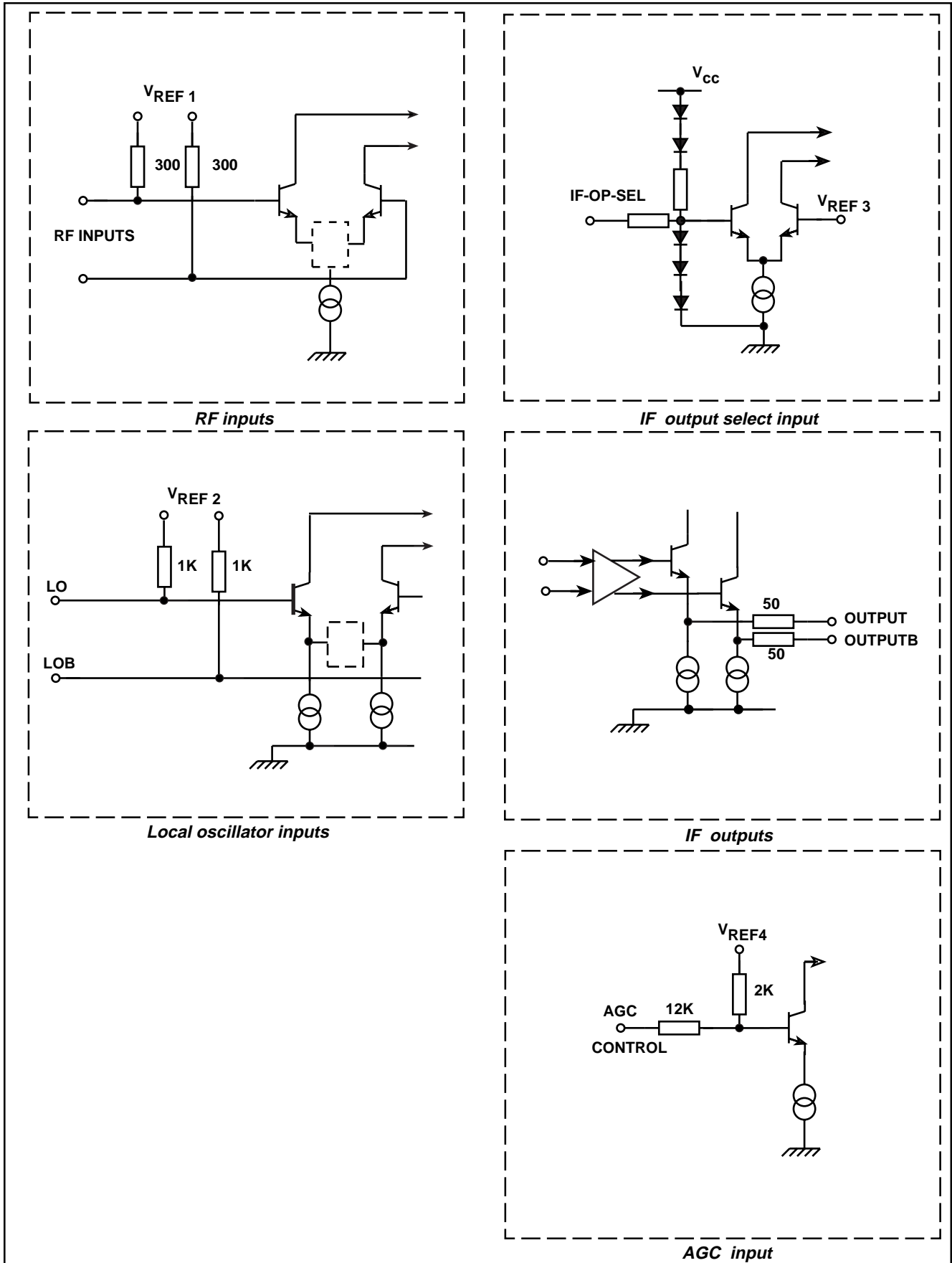


Fig. 10 Input/Output interface circuits

SL2017 Evaluation Board

This board has been created to show the operation of the SL2017 mixer together with the SP5659 low phase noise synthesiser. Schematics for the board are shown in Figs. 11a and 11b.

In a real system, the IF output would be fed to a SAW filter then onto either an FM demodulator such as the SL1466, or an IQ downconverter such as the SL1710 or SL1711. Control of the AGC would be via a loop, which should be set up to ensure that the SL1466, SL1710 or other IF chip receives the correct level for optimum performance.

For full evaluation, 30V and 5V supplies are necessary, together with I²C data, RF signal sources and test equipment.

Supplies

The board must be provided with the following supplies:

- a) 5V for the SL2017 and SP5659 and external oscillator and 30V for the varactor line.

The supply connector is a 3 pin 0.1" pitch pin header. The centre pin of the connector is GND.

I²C Bus connections

- b) The board is provided with an RJ11 I²C bus connector which feeds directly to the SP5659 synthesiser.

This connects to a standard 6-way connector cable which is supplied with the I²C/3-wire bus interface box.

Input and Output connections

The board is provided with the following connectors:

- a) RF I/P SMA connector (SMA1) which is AC coupled to the RF input of the SL2017.
- b) IF OUT 1 (SMA2) and IF OUT 2 (SMA5). These outputs may be selected by switching port P0 on the SP5659.

The standard IF output frequencies used are typically 402.75MHz or 479.5MHz. Either IF output may be connected directly to 50Ω test equipment such as a spectrum analyser.

Details of programming the SL2017 are included below.

Links and Switches

The board is provided with the following:

AGC SELECT switch

This switches between programmable control of the SL2017 AGC, via port P1 of the SP5659, or direct control via the pin TP1, EXTERNAL AGC VOLTAGE.

In normal application, the AGC will be controlled via a loop, such that the IF chip which follows is fed with the desired input level.

Programming of SP5659 Synthesiser

The SP5659 synthesiser is used to set the frequency of the VCO. Since high sided mixing is normally employed in satellite tuners, the VCO should be set to the IF above the wanted input channel.

Example: To mix a wanted channel at 1020.5MHz down to 479.5MHz.

The synthesiser must be programmed to 1020.5MHz + 479.5MHz = 1500MHz.

Send I²C data C2 0B B8 93 40 to the SP5659. See Table 1 for example I²C codes.

C2 is the address byte (byte 1).

0B B8 is the programmable divider information (bytes 2 and 3).

(i.e. 1500MHz / 500kHz = 3000 = 0BB8Hex)

93 is the programmable and reference divider information (byte 4). This will enable the prescaler and program the reference divider to a divide by 16 mode giving a 250kHz phase comparator frequency with a 500kHz step size when a 4MHz crystal is used.

40 is charge pump and port control data (byte 5).

The code 40 will set the charge pump current to 260uA. All ports will be switched off.

If it is required to use the SP5659 (for VCO < 2GHz) with the prescaler disabled it is recommended that data is initially sent to enable the prescaler. This will avoid a potential 'lock out' situation arising when the LO frequency is greater than 2GHz.

SL2017

Required VCO Frequency (MHz)	Byte 1 Address	Byte2 Prog Divider 8 MSB's	Byte 3 Prog Divider 8 LSB's	Byte 4 Prog Divider /Reference Divider	Byte 5 Charge Pump and Port Control
1500	C2	0B	B8	93	40
1600	C2	0C	80	93	40
1700	C2	0D	48	93	40
1800	C2	0E	10	93	40
1900	C2	0E	D8	93	40
2000	C2	0F	A0	93	40
2100	C2	10	68	93	40
2200	C2	11	30	93	40
2300	C2	11	F8	93	40
2400	C2	12	C0	93	40
Bottom of Band	C2	XX	XX	93	11
Top of Band	C2	XX	XX	93	10

Codes above are for Fcomp = 250kHz, prescaler enabled, giving Fstep = 500kHz.

X = Don't care

Table 1. Example I²C Hex codes for SP5659 synthesiser

Switching of SL2017 IF outputs

Port P0 is used to select the IF outputs.

When Port P0 is OFF, IF output 1 is selected.

When Port P0 is ON, IF output 2 is selected.

Switching of SL2017 AGC

Port P1 is used to program the AGC gain.

When Port P1 is OFF, AGC is set to 4V (minimum gain).

When Port P1 is ON, the AGC is set to 1V (maximum gain).

SL2017 Operation

The SL2017 is a downconverter mixer with an AGC amplifier, which when used with appropriate external varactor tuned oscillator performs the first IF tuning function for a full band satellite receiver system.

In application the RF input of the device is interfaced through appropriate impedance matching to the first IF signal, which is down linked from the outdoor unit at typically 950-2150MHz. The RF input preamplifier of the device is designed for low noise figure and for low distortion so eliminating the requirement for RF AGC. The preamplifier also provides gain to the mixer section and back isolation from the local oscillator signal.

The output of the preamplifier is fed to the mixer section where the RF signal is mixed with the local oscillator frequency.

Signals from the mixer are then fed to the AGC IF amplifier, which gives an overall conversion gain programmable from -10 to +30 dB. The output of this stage can be switched to one of two outputs to facilitate IF processing.

The SL2017 will mix an RF input signal from 950MHz - 2150MHz and produce an IF signal typically at 402.75MHz or 479.5MHz.

The device has a number of features, which may be either programmable via a synthesiser and operated as part of a dynamic AGC loop, or hardwired into a fixed mode.

There are a variety of parameters which can be measured using this evaluation board.

Measurement of Phase Noise.

This is best measured by looking at the IF output of the SL2017. The IF should be fed to a spectrum analyser, where it can be interpreted.

There are two common methods of doing this:

- a) using phase noise analysis software (such a HP85671A phase noise program)
- b) direct measurement of the noise floor at the chosen offset frequency, and conversion to a dBc/Hz figure.

Since method a) will depend on the software used, a description of method b) will be given only.

To measure phase noise at 10kHz offset:

- a) tune the centre frequency of the spectrum analyser to the IF - e.g. 479.5MHz
- b) Set the span initially wide (10MHz or greater). Gradually reduce this until it is set to 50kHz or less, taking care to ensure that the centre frequency of the display matches the IF peak.
- c) perform a peak search
- d) set marker delta to 10kHz
- e) set video averaging ON to ensure that a representative measurement of the noise floor at the chosen offset frequency is made.
- f) record the level of noise at the 10kHz offset compared to the peak IF level (in dBc).

Care must be taken to ensure that the LO is stable, since any instability will reduce the averaged peak LO value, thus giving a falsely low phase noise reading.

- g) convert the measured reading to a 1Hz bandwidth.

e.g. A measured phase noise of -50dBc/1kHz bandwidth (RBW of 1kHz) corresponds to -80dBc/Hz.

Since noise floor must be reduced by the ratio of the two bandwidths

i.e. $10 \log 1\text{kHz}/1\text{Hz} = 30\text{dB}$.

Measurement of Conversion Gain (from a 50Ω source)

- a) Connect an RF signal generator to the RF input to the SL2017.
- b) Connect an IF output to a spectrum analyser.
- c) Feed the SL2017 with the appropriate signal level, depending on AGC setting, required output, etc.
- d) Note the relative difference in the input and IF level in dB. This is the conversion gain of the device.

For increased accuracy, the input signal level should also be checked with a spectrum analyser, since any level measurement errors that exist within the analyser will then be relative, rather than literal.

The AGC voltage may be varied and conversion gain measured at different AGC voltages.

SL2017

Measurement of IM3 and IP3

a) Input two signal tones from RF generators. The level of these should be adjusted so that the device sees an input signal level of -19dBm from each tone.

Program the local oscillator so that both tones are mixed down to the IF (approx).

b) Adjust the AGC so that the device gives an overall conversion gain of +5dB.

c) Connect a spectrum analyser to the selected IF output of the device.

d) Measure the relative levels of the down converter signals and the 3rd order products (see diag overleaf).

Two input signals are used:

- f1 = 950MHz
- f2 = 951MHz

The local oscillator flo is tuned to 1430MHz.

This gives the following at the IF output:

$$fa = 1430\text{MHz} - 950\text{MHz} = 480\text{MHz}$$

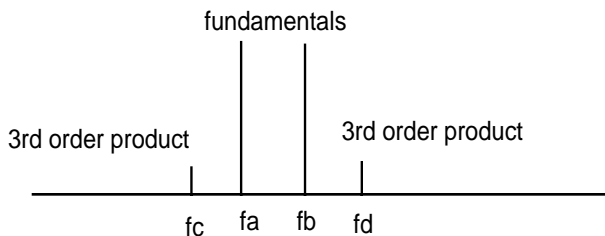
$$fb = 1430\text{MHz} - 951\text{MHz} = 479\text{MHz}$$

Mixing products are also produced in the front end. These are then downconverted by the mixer.

The in-band ones are listed below:

$$fd = flo - (2 \times f1 - f2)$$
$$fc = flo - (2 \times f2 - f1)$$

$$fd = 1430\text{MHz} - (2 \times 950\text{MHz} - 951\text{MHz}) = 481\text{MHz}$$
$$fc = 1430\text{MHz} - (2 \times 951\text{MHz} - 950\text{MHz}) = 478\text{MHz}$$



e) The difference in level in dB between the fundamentals and the 3rd order products is the IM3 of the device.

f) IP3 may be calculated from the above reading as follows:

$$IP3 = \text{RF input level} + \text{IM3}/2.$$

This level is usually referred to the input.

e.g.

Assuming a measured IM3 of 44dB, and with an input level of -19dBm,

$$IP3 = 44/2 + -19\text{dBm} = +3\text{dBm}$$

In a 50Ω system, this may be converted to dBuV by adding 107 to the value calculated since 0dBm = 107dBμV.

$$\text{i.e. } +3\text{dBm} = 110\text{dBuV}.$$

This is known as the input referred IP3 of the device.

If you experience any difficulties with this board, or require further help, please contact Robert Marsh on 01793 518234 or Fred Herman on 01793 518423. The fax number is 01793 518411.

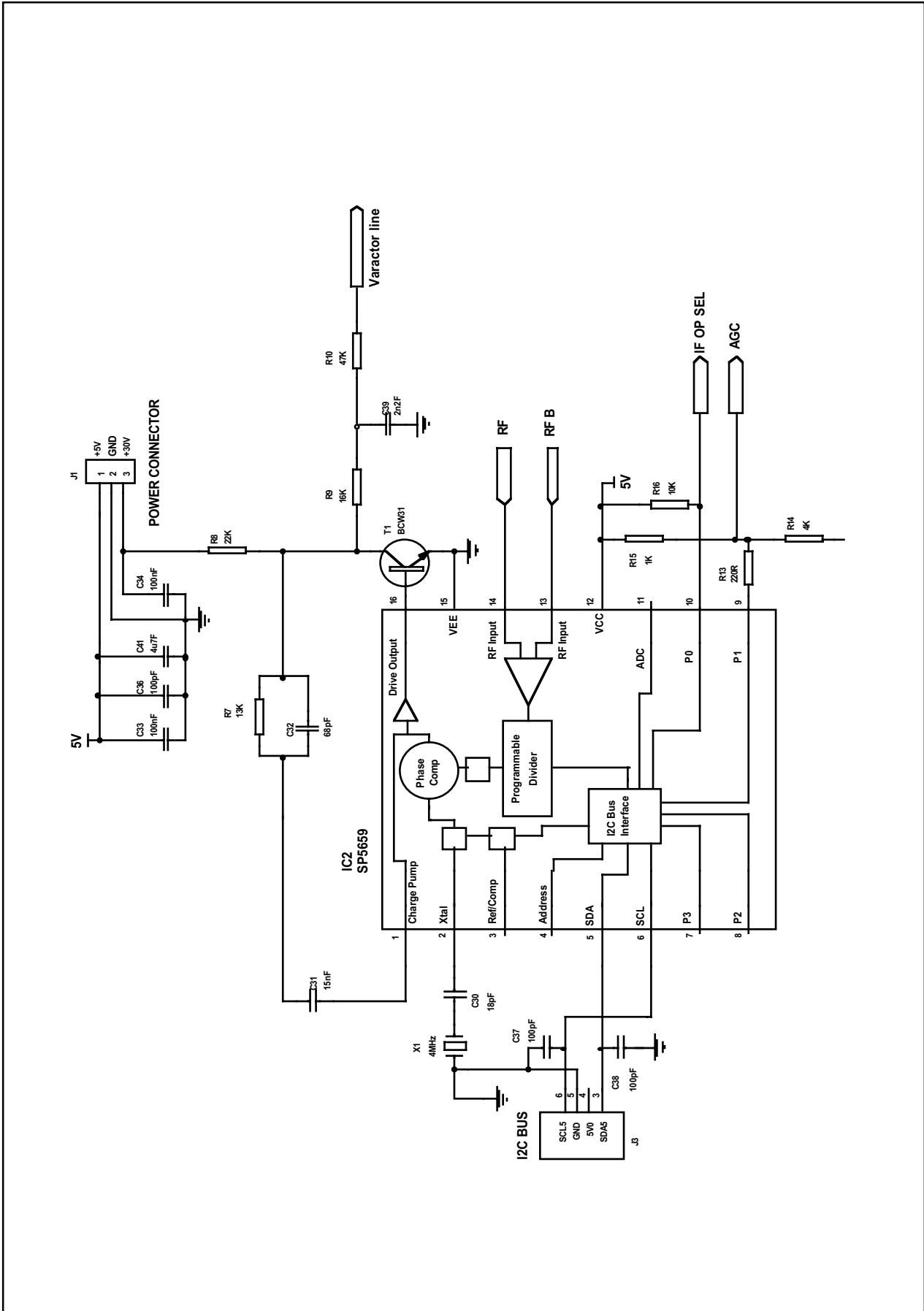


Fig. 11a Evaluation board schematic PLL section

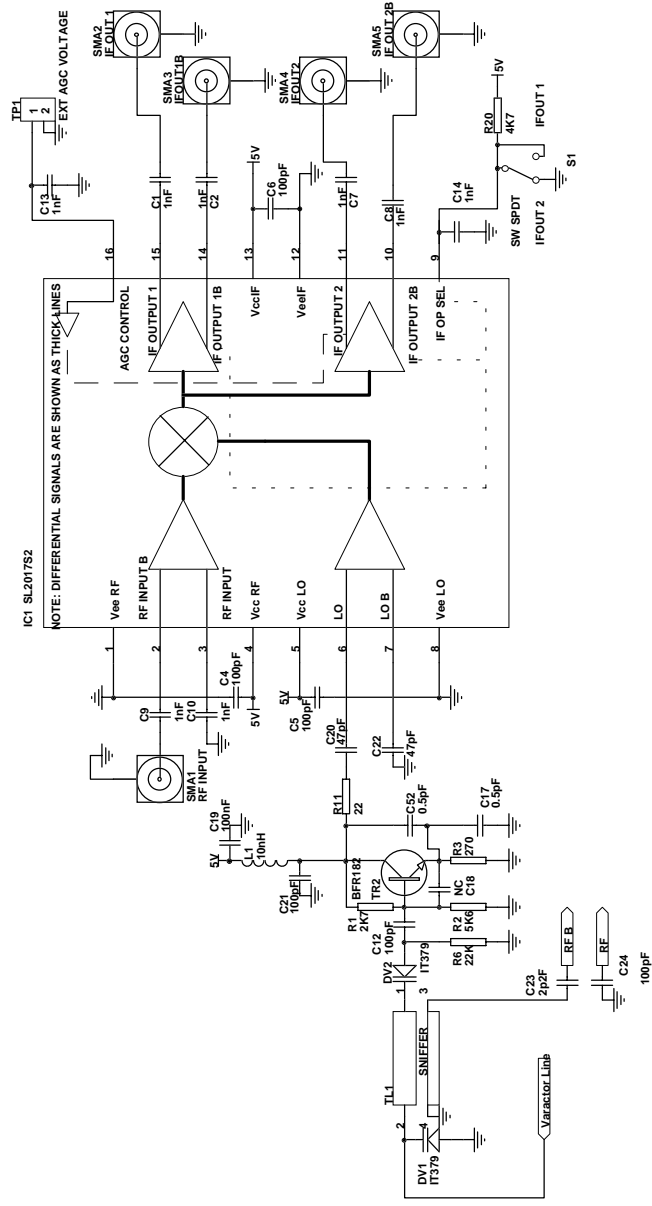


Fig. 11b Evaluation board schematic SL2017 Section

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

$T_{AMB} = -20^{\circ}\text{C}$ to $+80^{\circ}\text{C}$, $V_{CC} = +4.75\text{V}$ to 5.25V .

IF = 403.25MHz or 479.5MHz; IF bandwidth up to 54MHz maximum. RF input frequency = 950MHz - 2150MHz.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Supply Current, I_{CC}	4,5,13		80	115	mA	
RF input Noise figure	2,3		18		dB	@ $T_{amb} = 27^{\circ}\text{C}$. At maximum gain
Variation of Noise Figure with AGC setting				1	dB/dB	
Conversion gain						AGC bandwidth 100kHz
minimum AGC gain			-15	-5	dB	AGC = 4.0V
maximum AGC gain		25	33		dB	AGC = 1.0V
Gain inband ripple		-0.25		+0.25	dB	AGC = self bias (2.4V)
Gain variation across RF input range		-2		+2	dB	Channel bandwidth 27MHz
Gain imbalance between IF outputs	10,11 14,15	-2		+2	dB	
RF input impedance, single ended	2,3		50		Ω	@ $T_{amb} = 27^{\circ}\text{C}$
RF input return loss	2,3	8	12		dB	Input unmatched @ $T_{amb} = 27^{\circ}\text{C}$
RF input IP2	2,3	12	14		dBm	See note 2
RF input IP3	2,3	-1	1		dBm	See note 2
RF input IP3 variation with gain						See Fig. 6
Input referred 1dB gain compression						See Fig. 8
Two tone IM2 distortions with		-31	-33		dBc	See note 2
Two tone IM3 distortions		-36	-40		dBc	See note 2
LO input drive level	6,7	-10		0	dBm	From 1300 - 2700MHz
LO input impedance	6,7				Ω	See Smith chart Fig. 5

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated.

$T_{AMB} = -20^{\circ}\text{C}$ to $+80^{\circ}\text{C}$, $V_{CC} = +4.75\text{V}$ to 5.25V .

IF = 403.25MHz or 479.5MHz; IF bandwidth up to 54MHz maximum. RF input frequency = 950MHz -2150MHz.

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
LO leakage to RF input	2,3,6,7			-20	dBr	Relative to single ended input LO drive level
LO leakage to IF outputs	6,7,10,11 14,15			-10	dBm	Maximum conversion gain
AGC gain control slope variation	16					Monotonic from V_{EE} to V_{CC} . See Fig. 9
AGC control input current	16	-250		250	μA	
Output select low voltage	9			0.7	V	O/P 2 enabled, O/P 1 disabled
Output select high voltage	9	$V_{CC}-0.7$			V	O/P 1 enabled, O/P 2 disabled
Output select low current	9			-50	μA	
Output select high current	9			200	μA	
IF output 1 & 2	10,11, 14,15					Output in enabled and disabled state
Output impedance			50		Ω	Single ended
Return loss		12			dB	
IF output 1 to 2 isolation	10,11 14,15	30			dB	

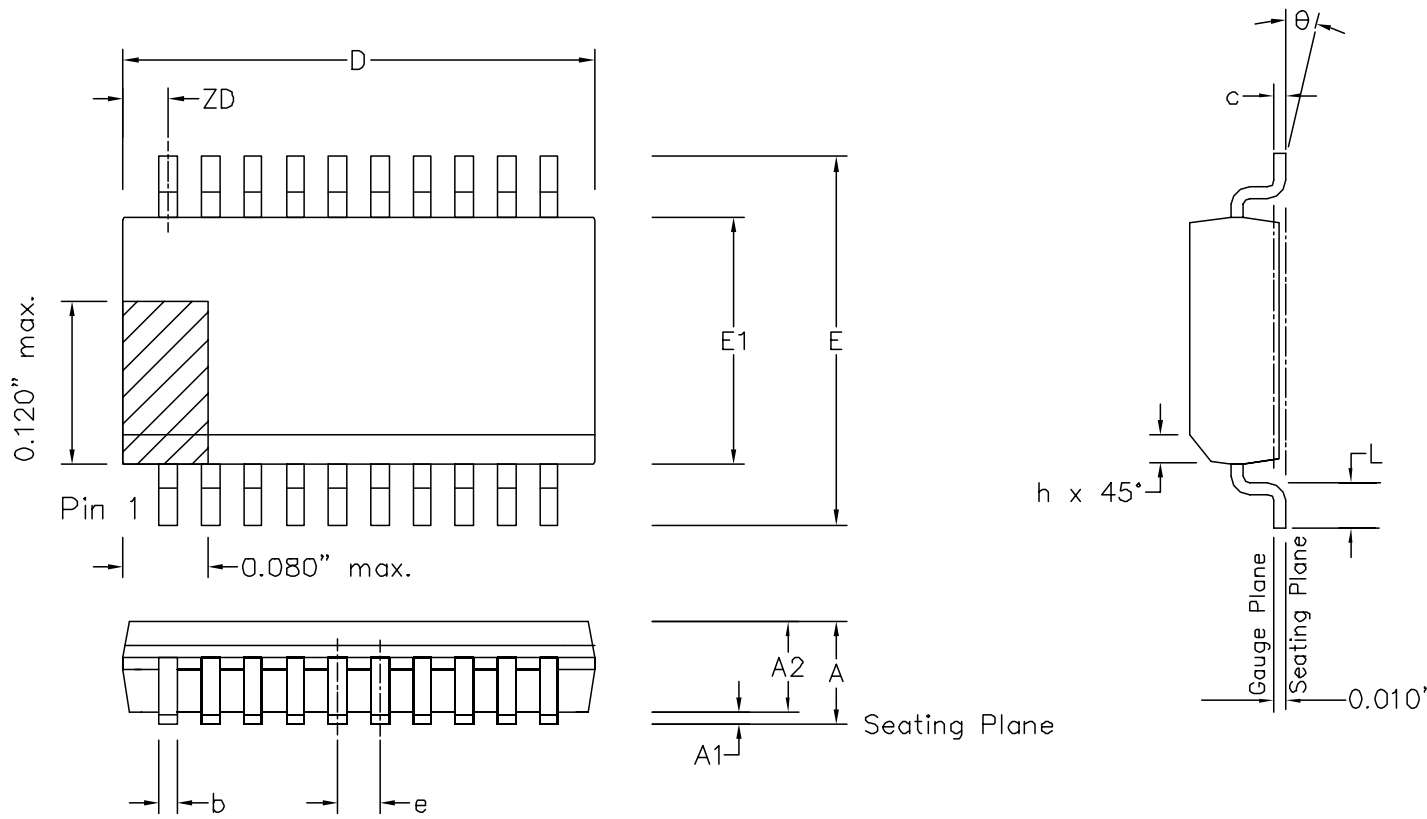
Notes:

1. All dBm units refer to a 50Ω system
2. Applies for any two carriers within band at -19dBm, and with AGC set for +5dB conversion gain.

ABSOLUTE MAXIMUM RATINGSAll voltages are referred to $V_{EE} = 0V$ (pins 1,8,12)

Parameter	Pin	Value		Units	Conditions
		Min	Max		
Supply voltages V_{CC}	4,5,13	-0.3	7	V	Transient
RF input voltage	2,3		2.5	Vp-p	
RF input DC offset	2,3	-0.3	$V_{CC}+0.3$	V	
LO input DC offset	6,7	-0.3	$V_{CC}+0.3$	V	
IF-OP-SEL input DC offset	9	-0.3	$V_{CC}+0.3$		
IF outputs 1 and 2 DC offset	10, 11 14, 15	-0.3	$V_{CC}+0.3$	V	
AGC Control input DC offset	16	-0.3	$V_{CC}+0.3$	V	
Storage temperature		-55	+150	°C	
Junction temperature			+150	°C	
MP16 thermal resistance					
Chip to ambient			111	°C/W	
Chip to case			41	°C/W	
Power consumption at $V_{CC}=5.25V$			580	mW	
ESD protection	ALL	1.75		kV	

Mil std 883 latest revision method
3015 cat 1.



Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	—	0.059	—	1.50
D	0.337	0.344	8.56	8.74
ZD	0.058	REF.	1.47	REF.
E	0.228	0.244	5.79	6.20
E1	0.150	0.157	3.81	3.99
L	0.016	0.050	0.41	1.27
e	0.025	BSC.	0.64	BSC.
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.18	0.25
θ	0°	8°	0°	8°
h	0.010	0.020	0.25	0.50
Pin features				
N	20			
Conforms to JEDEC MO-137AD Iss. A				

This drawing supersedes
 418/ED/51617/002 (Swindon/Roborough)
 TD/D 1029 (Oldham)

- Notes:
1. The chamfer on the body is optional. If it is not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
 2. Controlling dimensions are in inches.
 3. Dimension D do not include mould flash, protrusion or gate burrs. These shall not exceed 0.006" per side.
 4. Dimension E1 do not include inter-lead flash or protrusion. These shall not exceed 0.010" per side.
 5. Dimension b does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.004" total in excess of b dimension.

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ORIGINATING SITE: SWINDON

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DATE	27FEB97	24AUG99			
APPRD.					

MITEL SEMICONDUCTOR

Title:
 Package Outline Drawing for
 20L QSOP-0.150" Body Width(QP)

Drawing Number
 GPD00291



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