

SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2363 is in a 10 lead TO5 encapsulation.

The SL2364 is in a 14 lead DIL plastic encapsulation and a high performance Dilmon encapsulation.

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = 22^\circ\text{C} \pm 2^\circ\text{C}$

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BVCBO	10	20		V	$I_C = 10\mu\text{A}$
LVCEO	6	9		V	$I_C = 5\text{mA}$
BVEBO	2.5	5.0		V	$I_E = 10\mu\text{A}$
BVCIO	16	40		V	$I_C = 10\mu\text{A}$
hFE	50	80			$I_C = 8\text{mA}, V_{CE} = 2\text{V}$
f_T	2.5	5		GHz	$I_C(\text{Tail}) = 8\text{mA}, V_{CE} = 2\text{V}$
ΔV_{BE} (See note 1)		2	5	mV	$I_C(\text{Tail}) = 8\text{mA}, V_{CE} = 2\text{V}$
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/ $^\circ\text{C}$	$I_C(\text{Tail}) = 8\text{mA}, V_{CE} = 2\text{V}$
CCB		0.5	0.8	pF	$I_C(\text{Tail}) = 8\text{mA}, V_{CE} = 2\text{V}$
CCI		1.0	1.5	pF	$V_{CB} = 0$ $V_{CI} = 0$

NOTE 1. ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

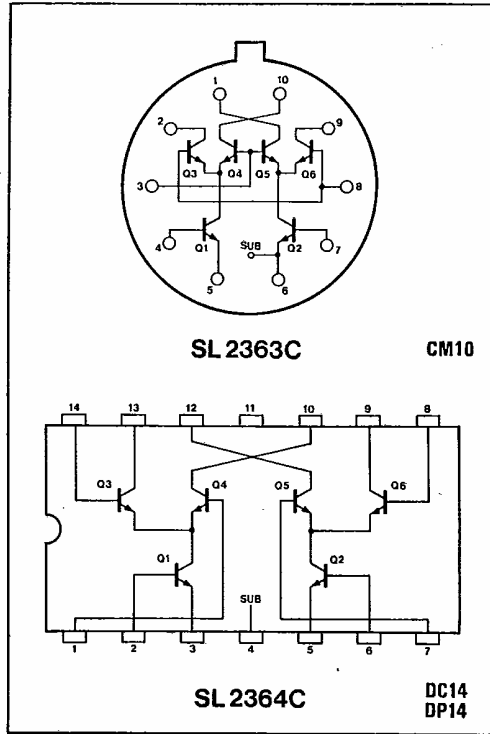


Fig. 1 Pin connections (top view)

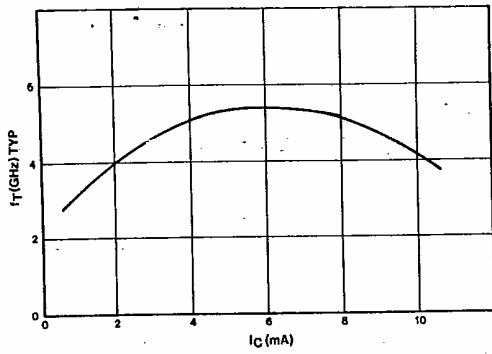


Fig. 2 Collector current

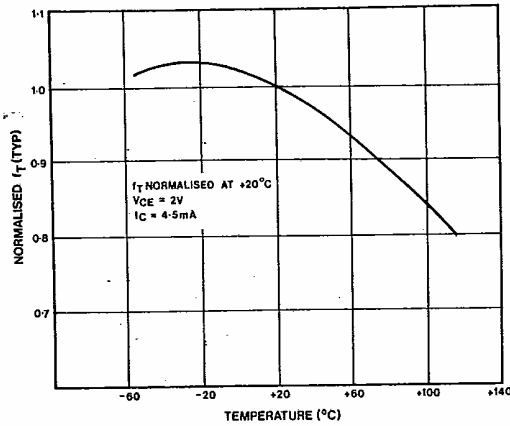


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature -55°C to +150°C

Maximum junction temperature +150°C

Package thermal resistance (°C/W):

Chip to case 65 (CM10)

Chip to ambient 225 (CM10) 175 (DP14)

$V_{CBO} = 10V$, $V_{EBO} = 2.5V$, $V_{CEO} = 6V$, $V_{CIO} = 15V$, I_C (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.